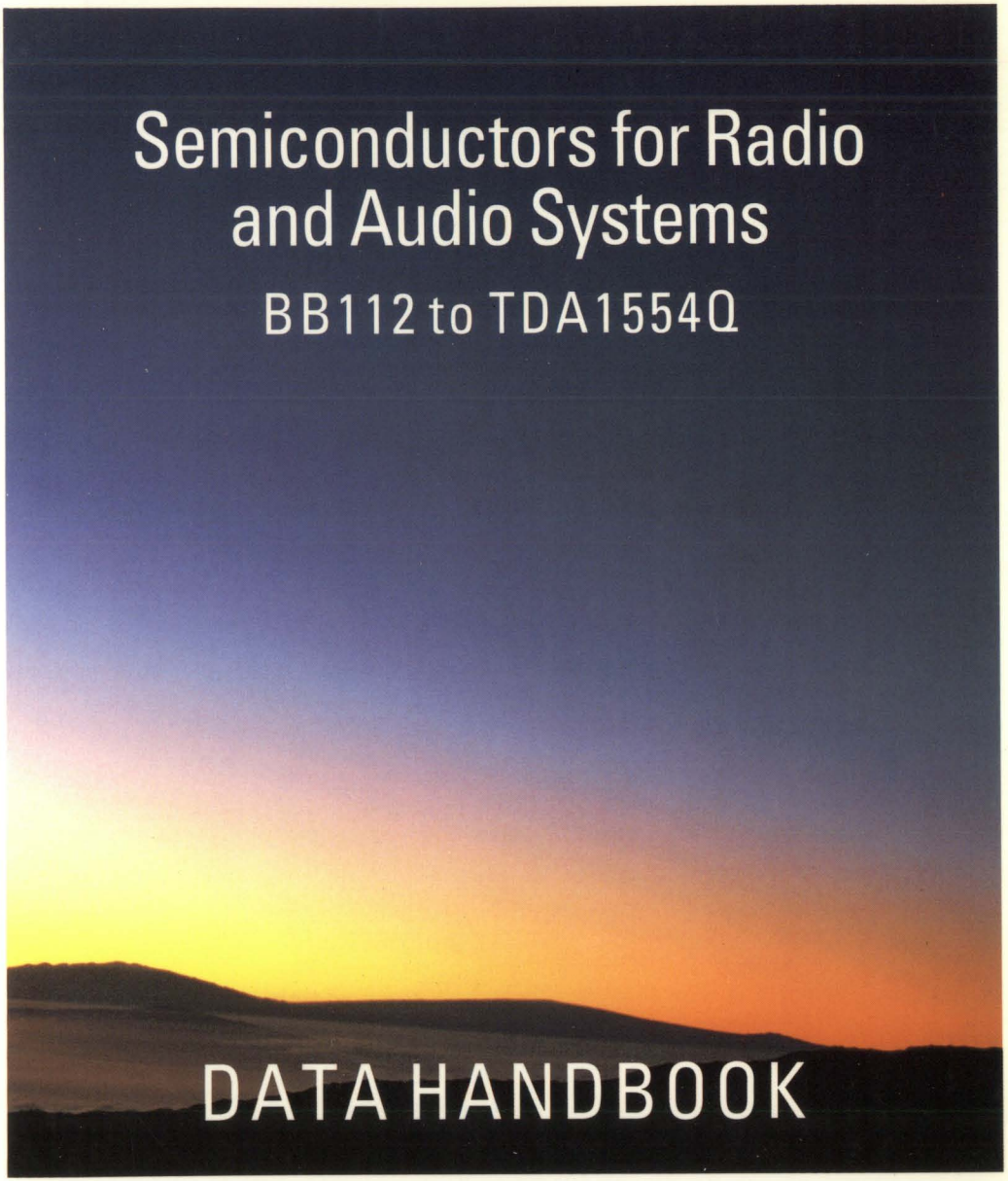
INTEGRATED CIRCUITS

Semiconductors for Radio and Audio Systems

BB112 to TDA1554Q



DATA HANDBOOK

Philips Semiconductors

PHILIPS

BOOK IC01a 1992

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Semiconductors for Radio and Audio Systems

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SEMICONDUCTORS

INTEGRATED CIRCUITS

MAINTAINANCE TYPE LIST

The types listed below are not included in this handbook. Detailed information will be supplied on request.

SAA3028	high performance transcoder (RC5) for infrared rermote control; I²C-bus
SAA7210	decoder for Compact Disc digital audio system
TDA1512A	12 to 20 W hi-fi audio power amplifier
TDA1512AQ	12 to 20 W hi-fi audio power amplifier
TDA1520B	20 W hi-fi audio power amplifier; complete SOAR protection
TDA1520BQ	20 W hi-fi audio power amplifier; complete SOAR protection
TDA1576T	FM/IF amplifier/demodulator circuit

GENERAL

Quality

Pro Electron type numbering system for Discrete Semiconductors

Pro Electron type numbering system for Integrated Circuits

Microcontroller type numbering

Rating systems

Handling MOS devices

QUALITY

Total Quality Management

Philips Semiconductors are a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is:

quality assurance

based on ISO 9000 standards, customer standards such as Ford Q1 and IBM MDQ, and the CECC system of conformity. Our factories are certified to ISO 9000 and CECC by external inspectorates

partnerships with customers

PPM co-operations, design-in agreements, and ship-to-stock, just-in-time and self-qualification programmes

partnerships with suppliers

ship-to-stock, statistical process control and ISO 9000 audits

quality improvement programme

continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- incoming material management through partnerships with suppliers
- in-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control
- acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications
- periodic inspections to monitor and measure the conformance of products.

Product reliability

With the increasing complexity of OEM (original equipment manufacturer) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies have resulted in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer responses

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR DISCRETE SEMICONDUCTORS

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

A germanium or other material with a band gap of 0.6 to 1 eV

B silicon or other material with a band gap of 1 to 1.3 eV

C gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more

R compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements. In the following list low power types are defined by $R_{th\ j\text{-}mb} > 15$ K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

A diode; signal, low power

B diode; variable capacitance

C transistor; low power, audio frequency

D transistor; power, audio frequency

E diode; tunnel

F transistor; low power, high frequency

G multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter, see under '*Serial number*'

H diode; magnetic sensitive

L transistor; power, high frequency

N photocoupler

P radiation detector; e.g. high sensitivity photo-transistor; with special third letter

Q radiation generator; e.g. LED, laser; with special third letter

R control or switching device; e.g. thyristor, low power; with special third letter

S transistor; low power, switching

T control and switching device; e.g. thyristor, power; with special third letter

U transistor; power, switching

W surface acoustic wave device

X diode; multiplier, e.g. varactor, step recovery

Y diode; rectifying, booster

Z diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER/SPECIAL THIRD LETTER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.(1) The letter has no fixed meaning, except in the following cases:

A for triacs, after second letter 'R' or 'T'

F for emitters and receivers in fibre-optic communication, after second letter 'G', 'P' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

L for lasers in non-fibre-optic applications, after second letter 'G' or 'Q'. When the second letter is 'G', the first letter should be defined in accordance with the material of the main optical device.

O for opto-triacs, after second letter 'R'

T for 3-state bicolour LEDs, after second letter 'Q'

W for transient voltage suppressor diodes, after second letter 'Z'.

EXAMPLES OF BASIC TYPE NUMBERS

AA112: germanium, low power signal diode (consumer type)

ACY32: germanium, low power AF transistor (industrial type)

BD232: silicon, power AF transistor (consumer type)

CQY17: GaAs, light-emitting diode (industrial type)

RPY84: CdS, photo-conductive cell (industrial type).

Version letter(s)

One or two letters may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type. The letters never have a fixed meaning, except that the letter 'R' indicates reverse polarity and the letter 'W' indicates a surface mounted device (SMD).

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

Suffix

Sub-classification can be used for devices supplied in a wide range of variants, called associated types. The following sub-coding suffixes are in use:

VOLTAGE REFERENCE AND VOLTAGE REGULATOR DIODES

One letter and one number, preceded by a hyphen (-). The letter, if required, indicates the nominal tolerance of the Zener voltage.

A 1%
B 2%
C 5%
D 10%
E 20%

In the case of a 3% tolerance, the letter 'F' is used.

The number denotes the typical operating (Zener) voltage, related to the nominal current rating for the entire range. The letter 'V' is used in place of the decimal point.

Example: BZY74-C6V3 or -C10.

TRANSIENT VOLTAGE SUPPRESSOR DIODES

One number, preceded by a hyphen (-). The number indicates the maximum recommended continuous reversed (stand-off) voltage, V_R. The letter 'V' is used in place of the decimal point.

Example: BZW70-9V1 or –39.

The letter 'B' may be used immediately after the last number, to indicate a bidirectional suppressor diode.

Example: BZW10-15B.

CONVENTIONAL AND CONTROLLED AVALANCHE RECTIFIER DIODES AND THYRISTORS

One number, preceded by a hyphen (-). The number indicates the rated maximum repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever is the lower. Reversed polarity with respect to the case is indicated by the letter 'R' immediately after the number.

Example: BYT-100 or -100R.

RADIATION DETECTORS

One number, preceded by a hyphen (-). The number indicates the depletion layer in micrometres (μm). The resolution is indicated by a version letter.

Example: BPX10-2A.

ARRAY OF RADIATION DETECTORS AND GENERATORS

One number, preceded by a hyphen (-). The number indicates the number of basic devices assembled into the array.

Examples: BPW50-6, BPW50-9, BPW50-12.

HIGH FREQUENCY POWER TRANSISTORS

One number, preceded by a hyphen (-). The number indicates the supply voltage.

Example: BLU80-24.

PRO ELECTRON TYPE NUMBERING SYSTEM FOR INTEGRATED CIRCUITS

Basic type number

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

FIRST AND SECOND LETTERS

Digital family circuits

The first two letters identify the family.(1)

Solitary circuits

The first letter divides solitary circuits into:

S solitary digital circuits
T analog circuits

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

U mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(1)

Microprocessors

The first two letters identify microprocessors and related circuits:

MA microcomputer or central processing unit
MB slice processor (functional slice of microprocessor)
MD related memories
ME other related circuits such as interfaces, clocks, peripheral controllers, etc.

Charge-transfer devices and switched capacitors

The first two letters identify:

NH hybrid circuits
NL logic circuits
NM memories
NS analog signal processing using switched capacitors
NT analog signal processing using charge-transfer devices
NX imaging devices
NY other related circuits

THIRD LETTER

The third letter indicates the operating ambient temperature range:

A temperature range not specified below
B 0 to + 70 °C
C −55 to +125 °C
D −25 to + 70 °C
E −25 to + 85 °C
F −40 to + 85 °C
G −55 to + 85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

Serial number

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

Version letter

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C cylindrical
D ceramic dual in-line (CERDIL, CERDIP)
F flat pack (two leads)
G flat pack (four leads)
H quad flat pack (QFP)
L chip on tape (foil)
P plastic dual in-line (DIL)
Q quad in-line (QUIL)
T mini pack (SOL, SO, VSO)
U uncased chip

Two-letter suffix

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

FIRST LETTER (GENERAL SHAPE)

C cylindrical
D dual in-line (DIL)
E power DIL (with external heatsink)
F flat pack (leads on two sides)
G flat pack (leads on four sides)
H quad flat pack (QFP)

(1) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

K diamond (TO-3 family)
M multiple in-line (except dual, triple and quad)
Q quad in-line (QUIL)
R power QUIL (with external heatsink)
S single in-line (SIL)
T triple in-line
W leaded chip carrier (LCC)
X leadless chip carrier (LLCC)
Y pin grid array (PGA)

SECOND LETTER (MATERIAL)

C metal-ceramic
G glass-ceramic
M metal
P plastic

Examples

PCF1105WP: digital IC; PC family; operating temperature range –40 to +85 °C; serial number 1105; plastic leaded chip carrier.

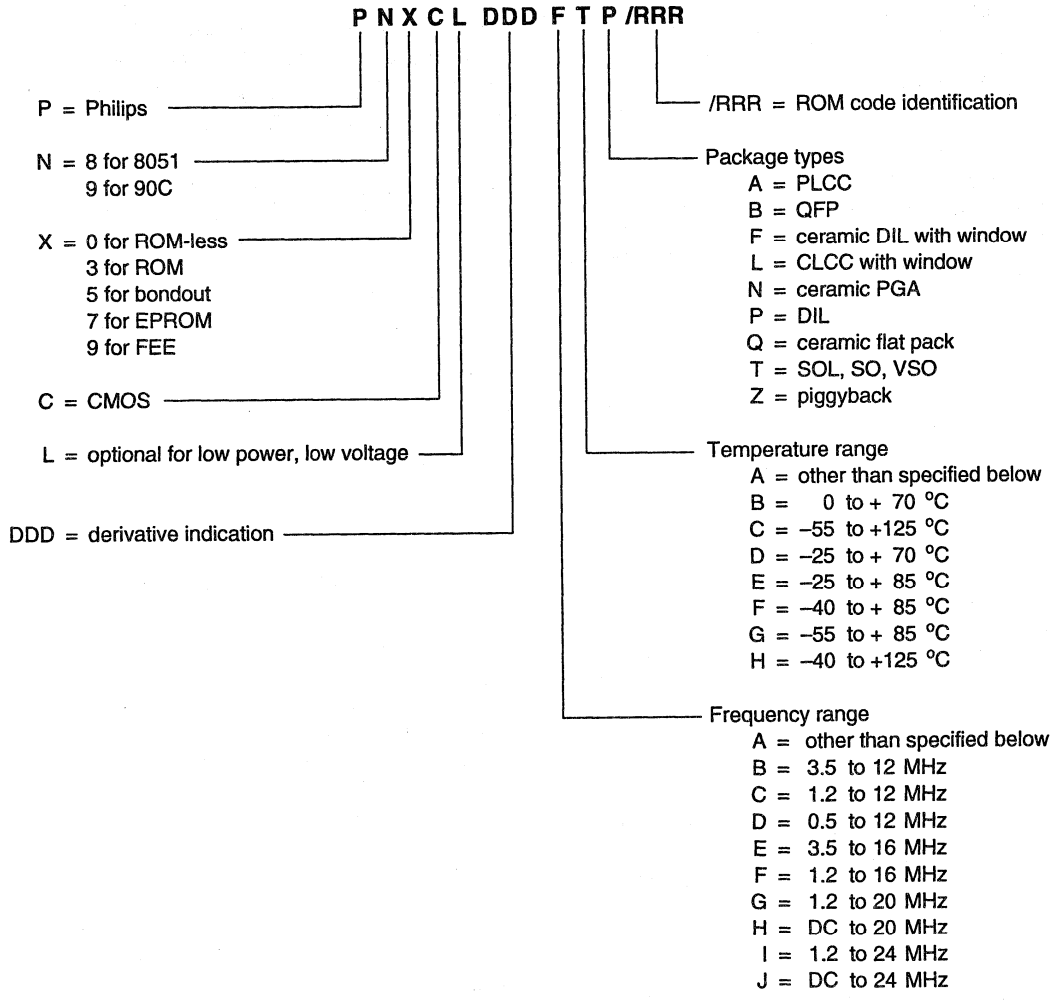
GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range –55 to +125 °C; serial number 2000.

MICROCONTROLLER TYPE NUMBERING

8051 and 90C derivatives



RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage

variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

Work station

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- persons at a work bench should be earthed via a wrist strap and a resistor
- all mains-powered electrical equipment should be connected via an earth leakage switch
- equipment cases should be earthed
- relative humidity should be maintained between 50 and 65%
- an ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

Assembly

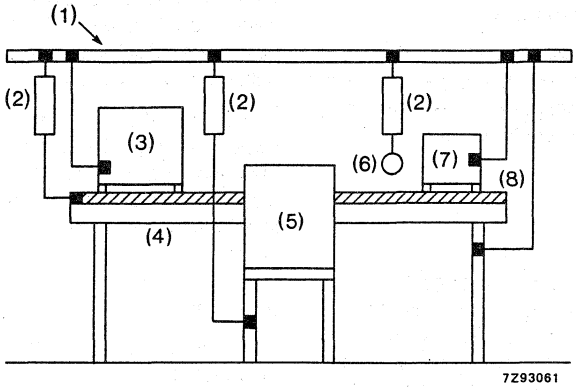
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.

Fig.1 Protected work station.

DEVICE DATA

SILICON PLANAR VARIABLE CAPACITANCE DIODE

The BB112 is a single 9 V variable capacitance diode in a plastic encapsulation for application in tuning circuits in a.m. receivers. The diodes are supplied in matched sets of three items.

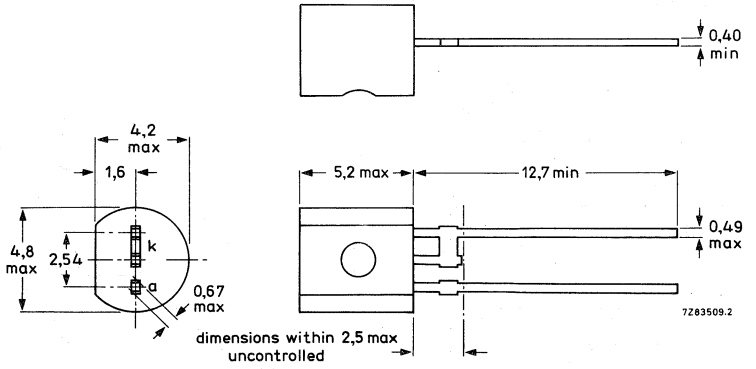
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	12 V
Operating junction temperature	T_j	max.	85 °C
Forward current	I_F	max.	50 mA
Reverse current at T_{amb} = 25 °C V_R = 12 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz V_R = 1 V V_R = 8,5 V	C_d C_d		440 to 540 pF 17 to 29 pF
Series resistance at f = 500 kHz V_R = 1 V	r_s	<	1,5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-69



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	12 V
Forward current (d.c.)	I_F	max.	50 mA
Operating junction temperature	T_j	max.	85 °C
Storage temperature	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Reverse current			
V_R = 12 V	I_R	<	50 nA
V_R = 12 V; T_{amb} = 85 °C	I_R	<	300 nA
Diode capacitance at f = 1 MHz			
V_R = 1 V	C_d		440 to 540 pF
V_R = 8,5 V	C_d		17 to 29 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\,(V_R = 1\ V)}{C_d\,(V_R = 8{,}5\ V)}$	>	18
Series resistance at f = 500 kHz			
V_R = 1 V	r_s	<	1,5 Ω
Temperature coefficient of the diode capacitance at f = 1 MHz; T_{amb} = −40 to + 85 °C; V_R = 1 V	η	typ.	0,05 %/K

Matching properties

D.C. capacitance ratio for a set of 3 diodes; V_P = 1 to 9 V	ΔC	⩽	3 %

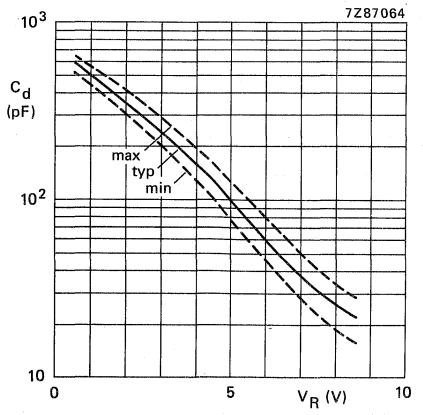


Fig. 2 Diode capacitance at f = 1 MHz as a function of the reverse voltage.

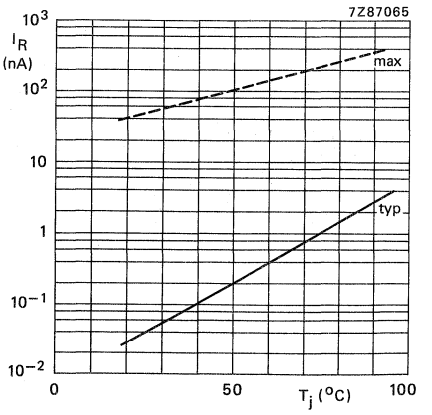


Fig. 3 Reverse current as a function of junction temperature at V_R = 12 V.

VARIABLE CAPACITANCE DIODE

A single variable capacitance diode, in a plastic envelope. The diode is for tuning of long, medium and short wavebands. Also suitable for frequency synthesizer applications.

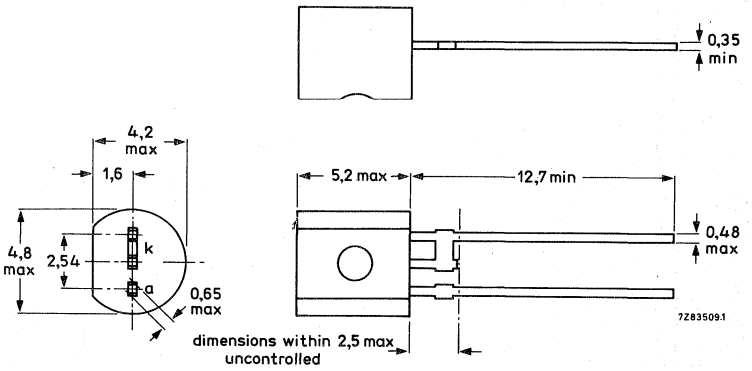
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	30 V
Reverse current at V_R = 30 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz; V_R = 28 V	C_d		12 to 21 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	>	23
Series resistance f = 1 MHz; V_R = 1 V	r_s	<	2 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOD-69 (TO-92 variant).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	30	V
Reverse voltage (peak value)	V_{RM}	max.	32	V
Forward current (d.c.)	I_F	max.	50	mA
Storage temperature	T_{stg}	−55 to +	125	°C
Operation junction temperature	T_j	max.	85	°C

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Reverse current				
V_R = 30 V	I_R	<	50	nA
V_R = 30 V; T_{amb} = 85 °C	I_R	<	300	nA
Diode capacitance at f = 1 MHz				
V_R = 1 V	C_d	450 to	550	pF
V_R = 28 V	C_d	12 to	21	pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 1\ V)}{C_d\ (V_R = 28\ V)}$	>	23	
Series resistance				
at f = 1 MHz and V_R = 1 V	r_s	<	2	Ω
Temperature coefficient of the diode capacitance at f = 1 MHz; T_{amb} = −20 °C to + 85 °C				
V_R = 1 V	η	typ.	0,05	%/°C
Capacitance matching				
Relative capacitance difference between two diodes at V_R = 1 to 28 V	$\frac{\Delta C}{C}$	<	3	%

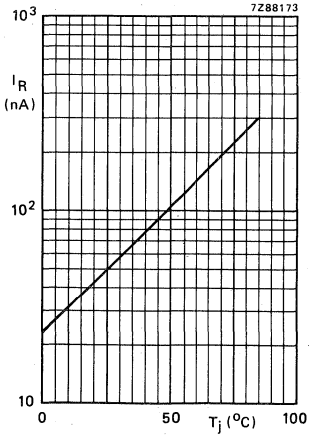


Fig. 2 Maximum values. Reverse current as a function of the junction temperature. V_R = 30 V.

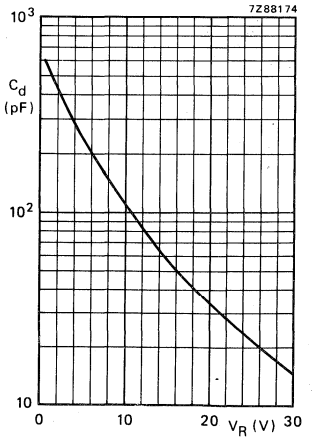


Fig. 3 Typical diode capacitance as a function of reverse voltage; f = 1 MHz.

SILICON PLANAR
VARIABLE CAPACITANCE DOUBLE DIODES

The BB204B and BB204G are double diodes with common cathode in a plastic TO-92 variant, primarily intended for electronic tuning in band II (f.m.). They are recommended for stages where large signals occur (e.g. oscillator circuits).

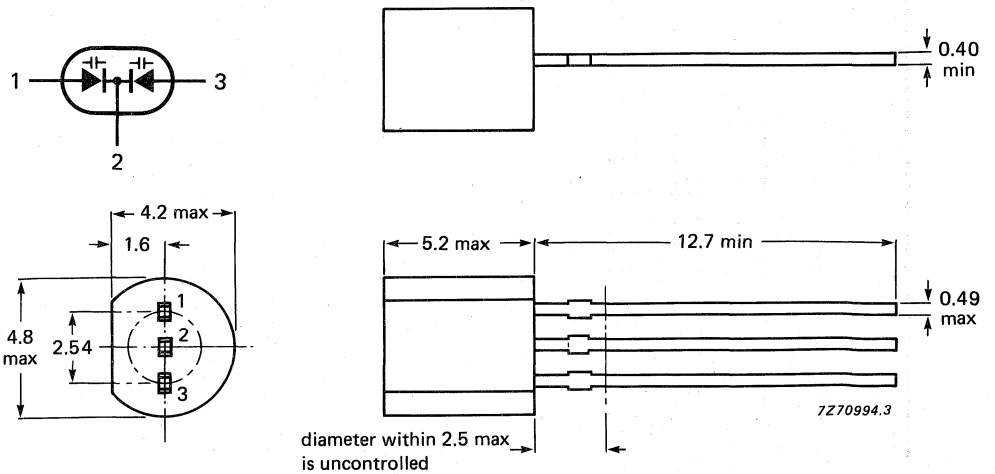
QUICK REFERENCE DATA

For each diode:				
Continuous reverse voltage	V_R	max.	30	V
Junction temperature	T_j	max.	100	°C
Reverse current at V_R = 30 V	I_R	<	50	nA
			BB204G | BB204B	
Diode capacitance at f = 1 MHz				
V_R = 3 V	C_d		34 – 39 | 37 – 42	pF
V_R = 8 V	C_d		22 – 27 | 24 – 29	pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 3\ V)}{C_d\ (V_R = 30\ V)}$		2,5 to 2,8	
Series resistance at f = 100 MHz V_R is that value at which C_d = 38 pF	r_D	typ. <	0,2 0,4	Ω Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

For each diode:

Continuous reverse voltage	V_R	max.	30	V
Forward current (d.c.)	I_F	max.	100	mA
Storage temperature	T_{stg}		−55 to + 100	°C
Junction temperature	T_j	max.	100	°C

CHARACTERISTICS

For each diode:

T_j = 25 °C

Reverse current at V_R = 30 V	I_R	<	50		nA
Diode capacitance at f = 1 MHz			BB204G	BB204B	
V_R = 3 V	C_d		34 – 39	37 – 42	pF
V_R = 8 V	C_d		22 – 27	24 – 29	pF
V_R = 30 V	C_d	typ.	14		pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 3\ V)}{C_d\ (V_R = 30\ V)}$		2,5 to 2,8		
Series resistance at f = 100 MHz V_R is that value at which C_d = 38 pF	r_D	typ. <	0,2 0,4		Ω Ω

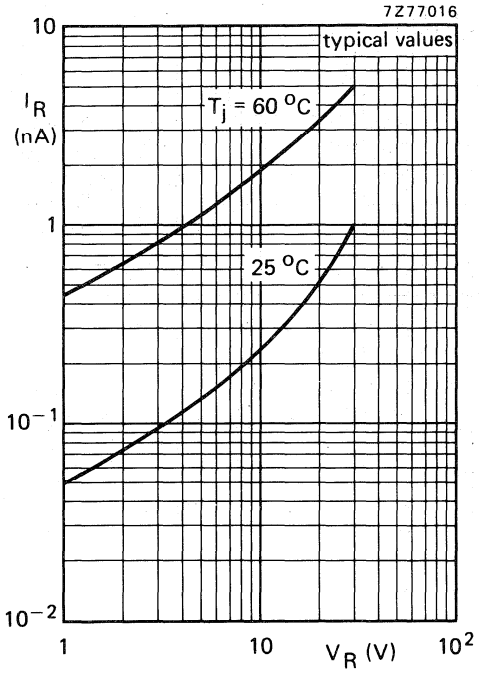

7Z77016
typical values
T_j = 60 °C
25 °C
I_R (nA)
10
1
10^{-1}
10^{-2}
1
10
V_R (V)
10^2

Fig. 2.

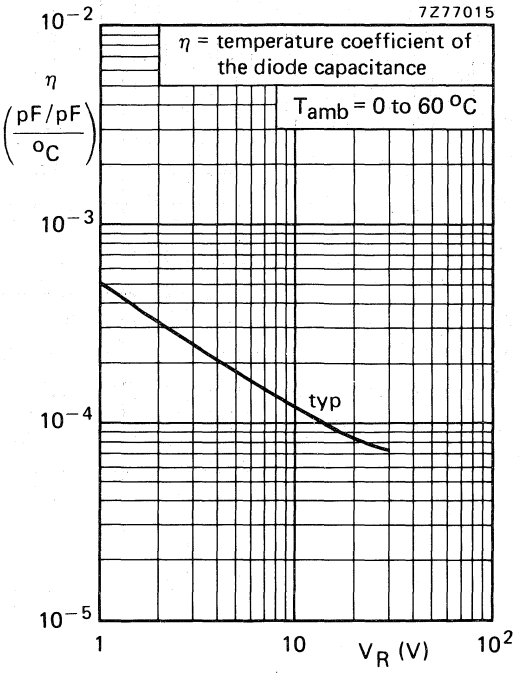

7Z77015
η = temperature coefficient of the diode capacitance
T_{amb} = 0 to 60 °C
η $\left(\frac{pF/pF}{°C}\right)$
10^{-2}
10^{-3}
10^{-4}
10^{-5}
typ
1
10
V_R (V)
10^2

Fig. 3.

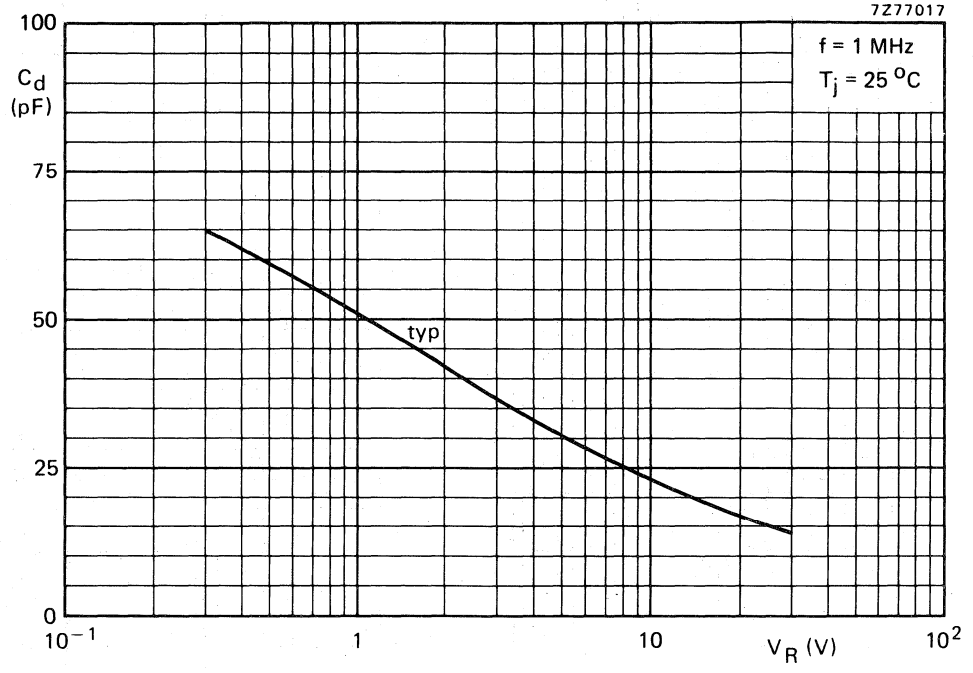

7Z77017
f = 1 MHz
T_j = 25 °C
C_d (pF)
100
75
50
25
0
typ
10^{-1}
1
10
10^2
V_R (V)

Fig. 4.

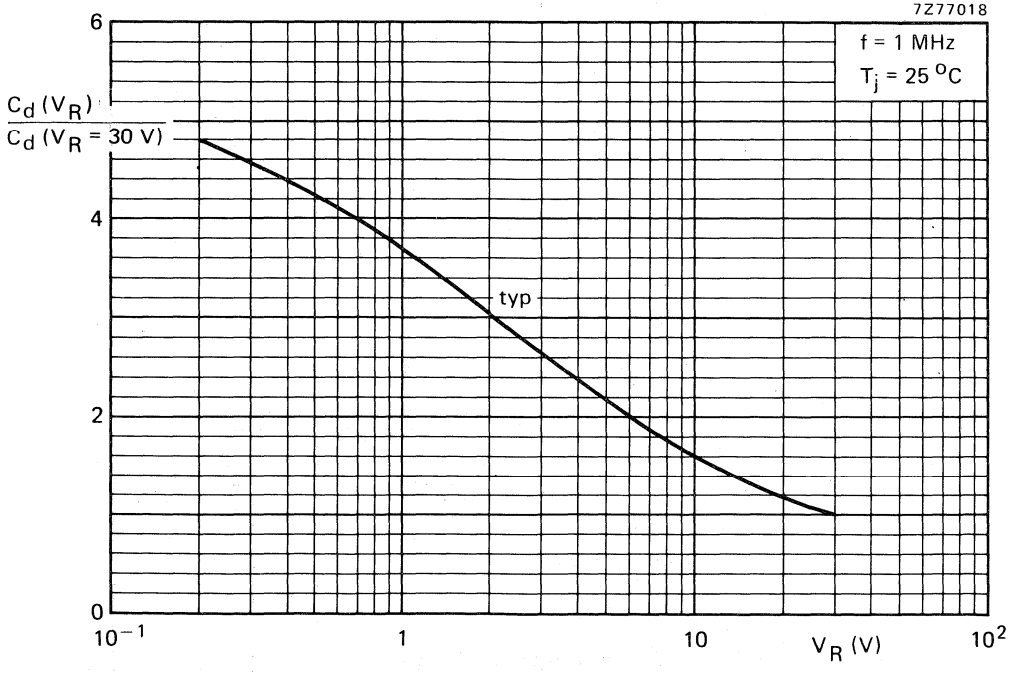

7Z77018
f = 1 MHz
T_j = 25 °C
$\frac{C_d (V_R)}{C_d (V_R = 30\ V)}$
6
4
2
0
typ
10^{-1}
1
10
10^2
V_R (V)

Fig. 5.

A.M. VARIABLE CAPACITANCE DOUBLE DIODES

The BB212 is a double 9V variable capacitance diode with common cathode in a plastic TO-92 variant.

A special feature is the low tuning voltage which makes the device particularly suited to car and domestic receivers in the L.W., M.W. and S.W. bands.

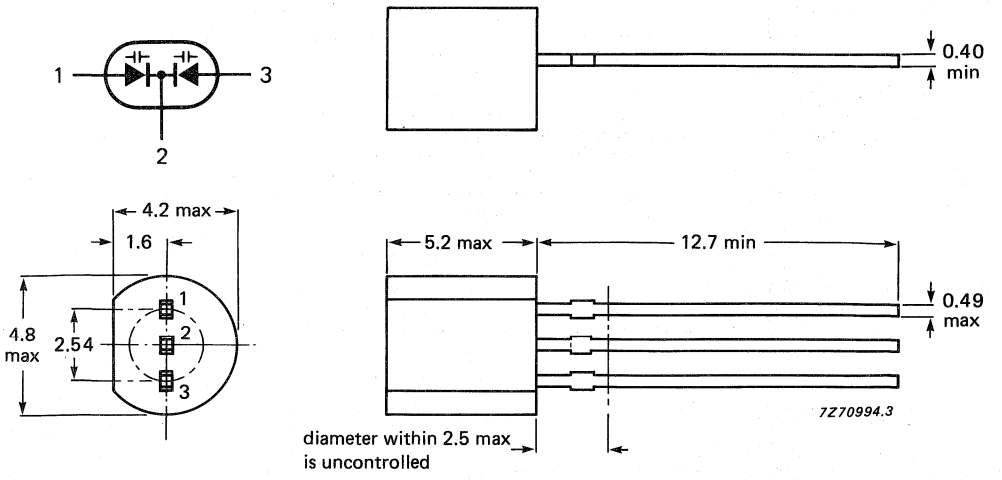
QUICK REFERENCE DATA

For each diode:			
Continuous reverse voltage	V_R	max.	12 V
Operating junction temperature	T_j	max.	85 °C
Reverse current at T_j = 25 °C V_R = 10 V	I_R	<	50 nA
Diode capacitance at f = 1 MHz			
V_R = 0,5 V	C_d		500 to 620 pF
V_R = 8,0 V	C_d	<	22 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 0{,}5\ V)}{C_d\ (V_R = 8{,}0\ V)}$	>	22,5
Series resistance at f = 500 kHz V_R is that value at which C_d = 500 pF	r_s	<	2,5 Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



The anode of the diode with the higher capacitance C_1 at V_R = 3 V, i.e. a more positive mismatch, is identified by a white dot.

RATINGS (for each diode)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	12 V
Forward current (d.c.)	I_F	max.	100 mA
Storage temperature	T_{stg}		−55 to + 100 °C
Operating junction temperature	T_j	max.	85 °C

CHARACTERISTICS (for each diode)

T_j = 25 °C unless otherwise specified

Reverse current			
V_R = 10 V	I_R	<	50 nA
V_R = 10 V; T_{amb} = 60 °C	I_R	<	200 nA
Diode capacitance at f = 1 MHz			
V_R = 0,5 V	C_d		500 to 620 pF
V_R = 3,0 V	C_d		140 to 280 pF
V_R = 5,5 V	C_d		40 to 90 pF
V_R = 8,0 V	C_d	<	22 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 0{,}5\ V)}{C_d\ (V_R = 8{,}0\ V)}$	>	22,5
Series resistance at f = 500 MHz			
V_R is that value at which C_d = 500 pF	r_s	<	2,5 Ω
Temperature coefficient of the diode capacitance at f = 1 MHz; T_{amb} = 25 °C to 60 °C			
V_R = 0,5 V	η	typ.	0,054 %/K
V_R = 8,0 V	η	typ.	0,050 %/K

MATCHING PROPERTIES

The capacitance of the two diodes in their common envelope may differ within certain limits. The total, relative capacitance difference between the two diodes in one envelope may be found in Fig. 2. The anode a1 or a2 with the higher capacitance at V_R = 3 V, is identified by a white dot.

BASIC TOLERANCE

The relative deviation of the capacitance value at V_R = 0,5 V is maximum 3,5%.

$$k = \left| \frac{C_1\ (0{,}5\ V) - C_2\ (0{,}5\ V)}{C_2\ (0{,}5\ V)} \right| = < 3{,}5\%.$$

ADDITIONAL TOLERANCE

In the range of V_R = 0,5 to 8 V the following additional tolerances are valid.

$$S = \left| \left(\frac{C_1}{C_2}\right)_{V_R} - \left(\frac{C_1}{C_2}\right)_{0{,}5\ V} \right|$$

$S < 2\%$ for V_R = 0,5 to 3 V
$S < 4\%$ for V_R = 3 to 5,5 V
$S < 6\%$ for V_R = 5,5 to 8 V

} see Fig. 2

C_1 is the capacitance of a_1 when $a_1 > a_2$
C_1 is the capacitance of a_2 when $a_2 > a_1$

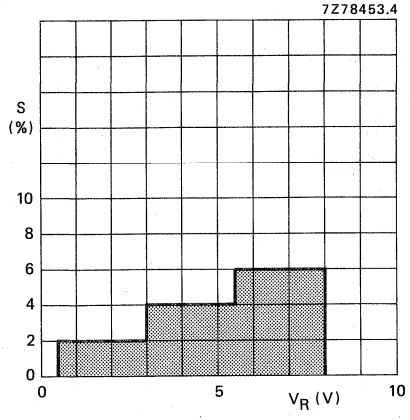


Fig. 2 The shaded area represents the maximum tolerance of the two diodes in one envelope as a function of the reverse voltage.

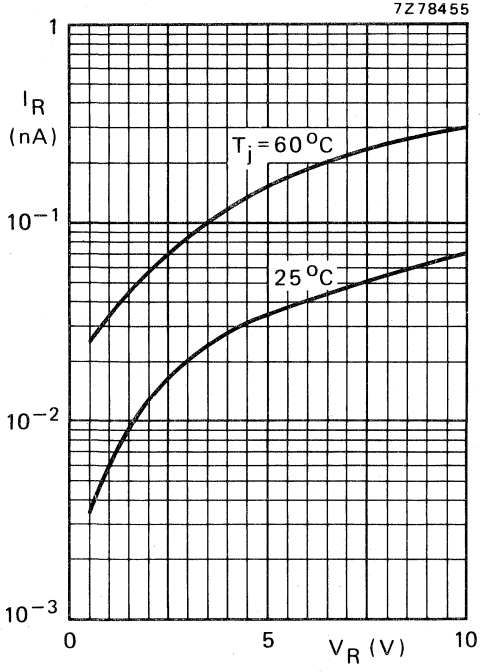


Fig. 3 Typical values.

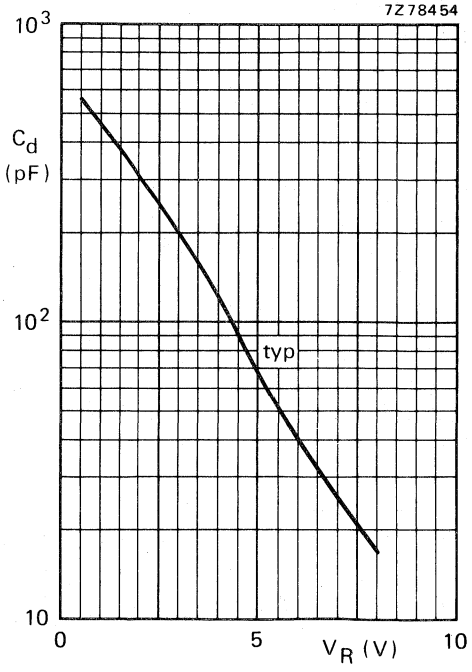


Fig. 4 f = 1 MHz.

VHF VARIABLE CAPACITANCE DOUBLE DIODE

The BB804 is a variable capacitance double diode in planar technology with common cathode in a plastic SOT23 envelope. It is intended for FM tuning especially for car radios.

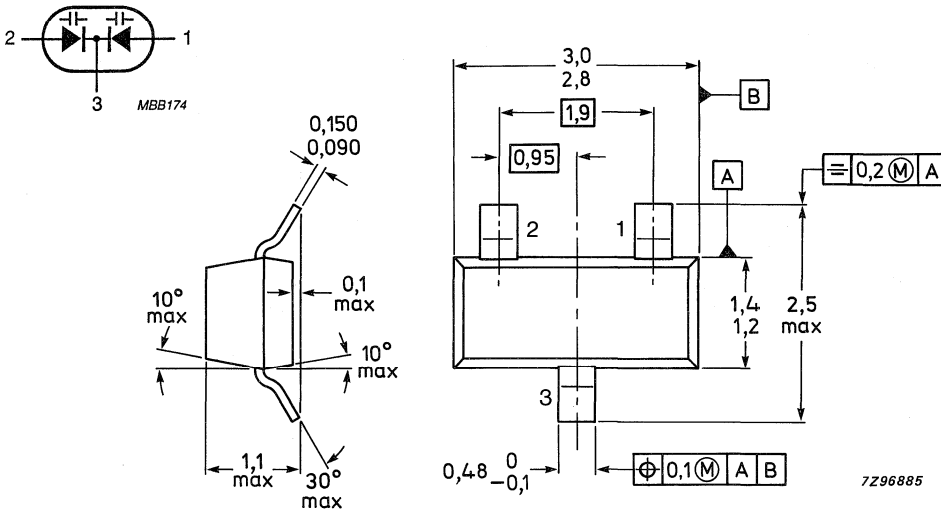
QUICK REFERENCE DATA

Continuous reverse voltage	V_R	max.	18 V
Repetitive peak reverse voltage	V_{RRM}	max.	20 V
Forward current (DC)	I_F	max.	50 mA
Operating junction temperature	T_j	max.	100 °C
Reverse current	I_R	max.	20 nA
Diode capacitance at f = 1 MHz V_R = 2 V	C_d		42 to 47.5 pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 2\ V)}{C_d\ (V_R = 8\ V)}$		1.65 to 1.75
Series resistance at f = 100 MHz V_R is that value at which C_d = 38 pF	r_s	typ.	0.20 Ω

MECHANICAL DATA

Dimensions in mm

Marking SF x (x = 0 - 4)



TOP VIEW

Fig.1 SOT23.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Continuous reverse voltage	V_R	max.	18	V
Forward current (DC)	I_F	max.	50	mA
Repetitive peak reverse voltage	V_{RRM}	max.	20	V
Storage temperature range	T_{stg}		−55 to + 100	°C
Operating junction temperature	T_j	max.	100	°C

THERMAL RESISTANCE

From junction to ambient mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Reverse current				
V_R = 16 V	I_R	<	20	nA
V_R = 16 V; T_{amb} = 60 °C	I_R	<	200	nA
Diode capacitance at f = 1.0 MHz				
V_R = 2 V				
red 0	C_d		42 to 43.5	pF
yellow 1	C_d		43 to 44.5	pF
white 2	C_d		44 to 45.5	pF
green 3	C_d		45 to 46.5	pF
blue 4	C_d		46 to 47.5	pF
Capacitance ratio at f = 1 MHz	$\frac{C_d\ (V_R = 2\ V)}{C_d\ (V_R = 8\ V)}$		1.65 to 1.75	
Series resistance at f = 100 MHz, V_R is that value at which C_d = 38 pF	r_s	typ.	0.20	Ω

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

QUICK REFERENCE DATA

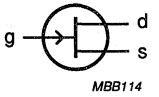
Drain-source voltage	$\pm V_{DS}$			max. 30		V
Gate-source voltage (open drain)	$-V_{GSO}$			max. 30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}			max. 300		mW
		BF245A/0	A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 0,5	2,0	6	12	mA
		< 2,1	6,5	15	25	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0,25 to 8,0		V
Feedback capacitance at f = 1 MHz V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}			typ. 1,1		pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\|y_{fs}\|$			3,0 to 6,5		mS

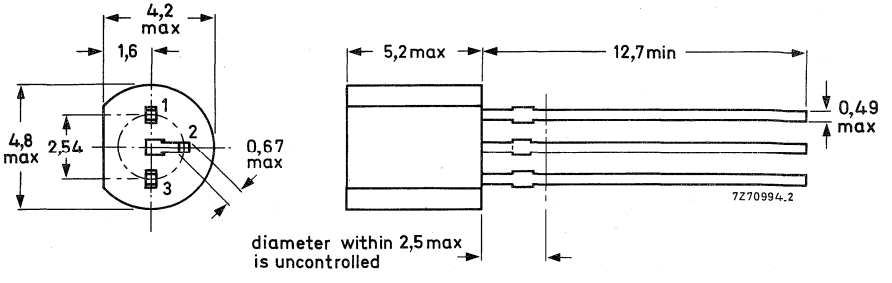
MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.

Pinning:
1 = drain
2 = source
3 = gate





Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Drain current	I_D	max.	25	mA
Gate current	I_G	max.	10	mA
Power dissipation				
up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
up to T_{amb} = 90 °C	P_{tot}	max.	300	mW 1)
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	200	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5	μA
Drain current 2)					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS} 3)	> 2	6,0	12	mA
		< 6,5	15,0	25	mA
Gate-source breakdown voltage					
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30	V
Gate-source voltage					
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$ 3)	> 0,4	1,6	3,2	V
		< 2,2	3,8	7,5	V

1) Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

2) Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

3) BF245A/0: I_{DSS} = 0,5 to 2,1 mA; $-V_{GS}$ = 0,2 to 1,0 V
BF245A/1: I_{DSS} = 1,9 to 3,0 mA; $-V_{GS}$ = 0,4 to 1,0 V
BF245A/2: I_{DSS} = 3,0 to 4,5 mA; $-V_{GS}$ = 0,7 to 1,4 V
BF245A/3: I_{DSS} = 4,5 to 6,5 mA; $-V_{GS}$ = 1,1 to 2,2 V.

Gate-source cut-off voltage				
I_D = 10 nA; V_{DS} = 15 V		$-V_{(P)GS}$	0,25 to 8,0	V
y-parameters at T_{amb} = 25 °C (common source)				
V_{DS} = 15 V; V_{GS} = 0				
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5	mS
	Output admittance	$\|y_{os}\|$	typ. 25	μS
f = 200 MHz	Input conductance	g_{is}	typ. 250	μS
	Reverse transfer admittance	$\|y_{rs}\|$	typ. 1,4	mS
	Transfer admittance	$\|y_{fs}\|$	typ. 6	mS
	Output conductance	g_{os}	typ. 40	μS
V_{DS} = 20 V; $-V_{GS}$ = 1 V				
f = 1 MHz	Input capacitance	C_{is}	typ. 4,0	pF
	Feedback capacitance	C_{rs}	typ. 1,1	pF
	Output capacitance	C_{os}	typ. 1,6	pF
Cut-off frequency *				
V_{DS} = 15 V; V_{GS} = 0		f_{gfs}	typ. 700	MHz
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)				
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise		F	typ. 1,5	dB

* The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

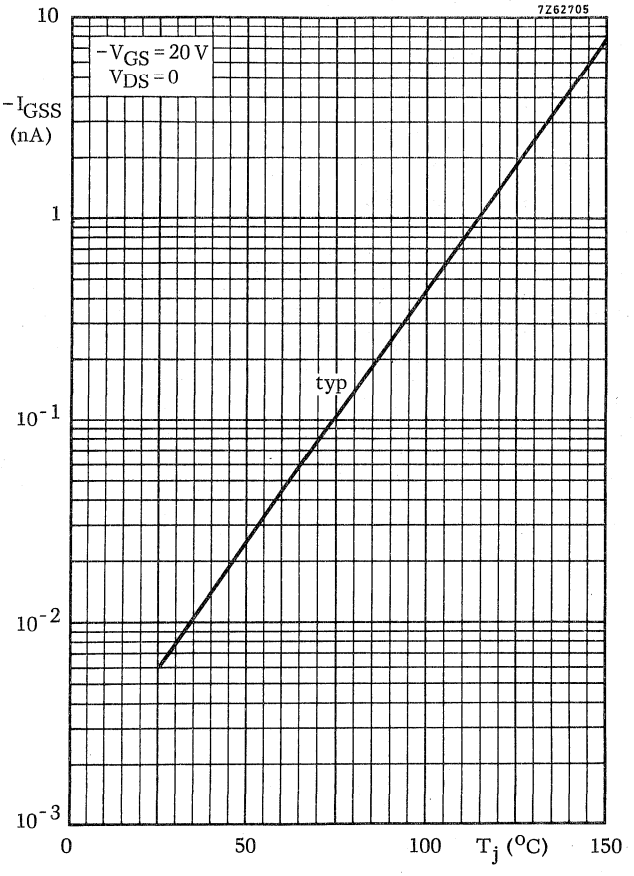

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

Fig. 2

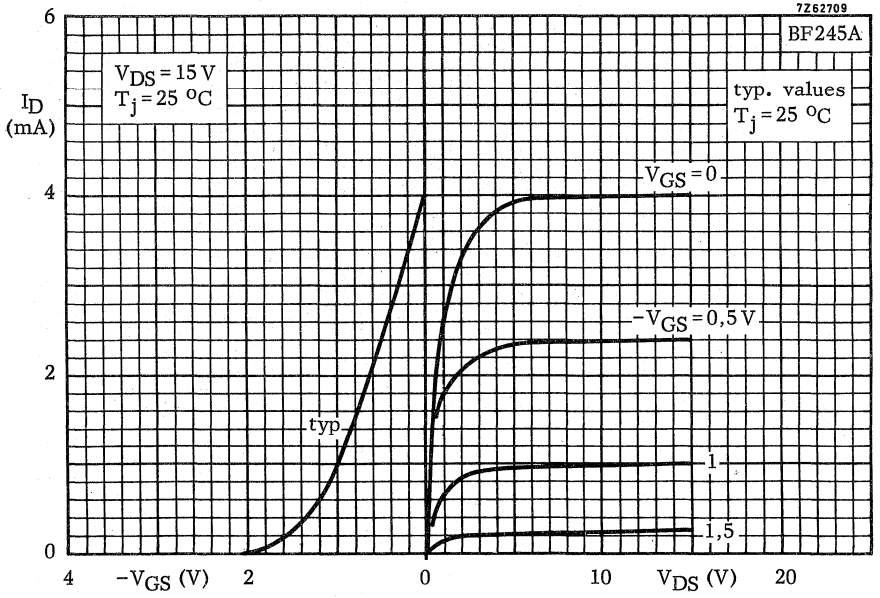

7Z62709
BF245A
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 3

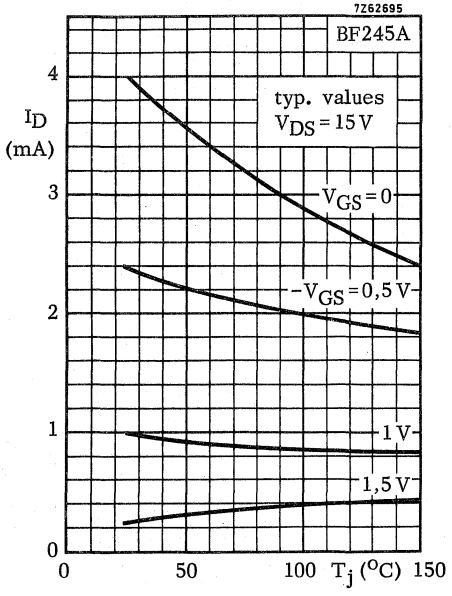

7Z62695
BF245A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
4
3
2
1
0
0
50
100
T_j (°C)
150

Fig. 4

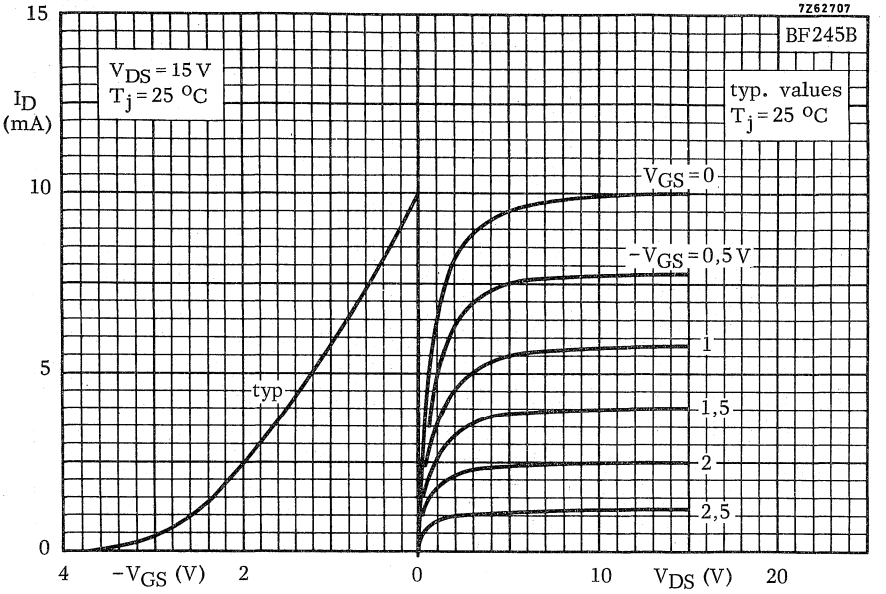

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

Fig. 5

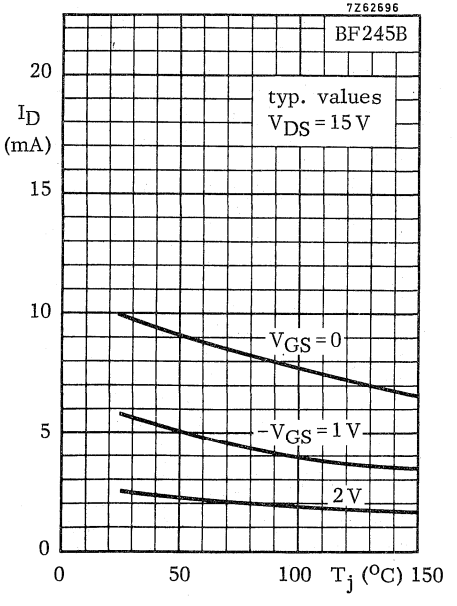

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

Fig. 6

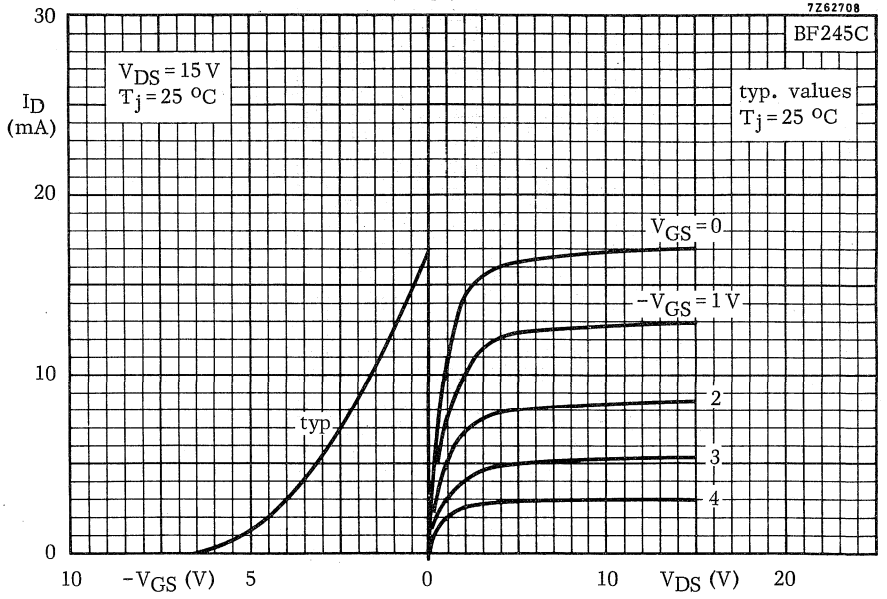

7Z62708
BF245C
typ. values
T_j = 25 °C
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
30
20
10
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

Fig. 7

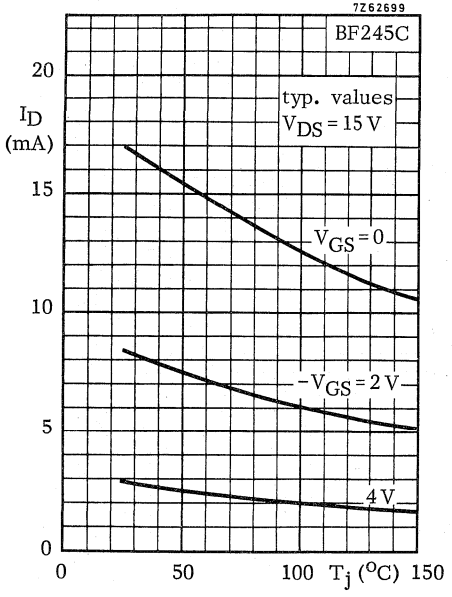

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

Fig. 8

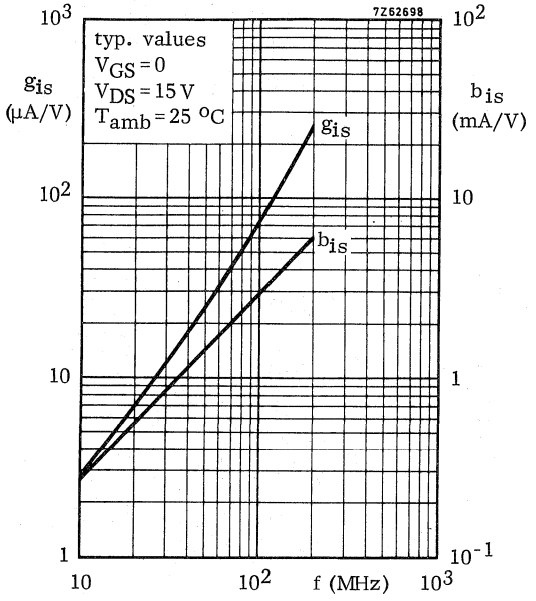

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
g_{is}
b_{is}
g_{is} (μA/V)
b_{is} (mA/V)
10^3
10^2
10
1
10^2
10
1
10^{-1}
f (MHz)

Fig. 9

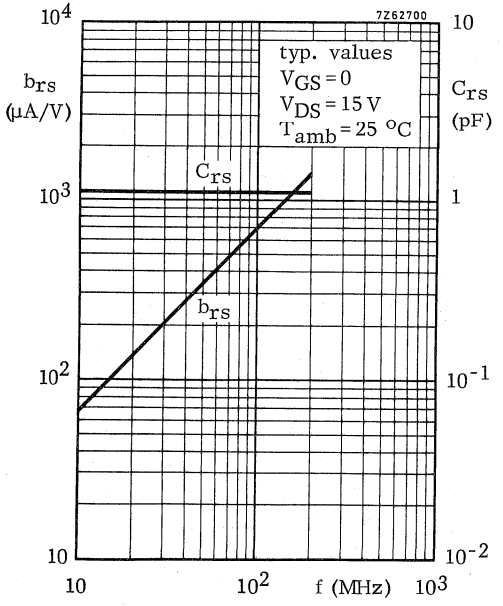

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
C_{rs}
b_{rs}
b_{rs} (μA/V)
C_{rs} (pF)
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
f (MHz)

Fig. 10

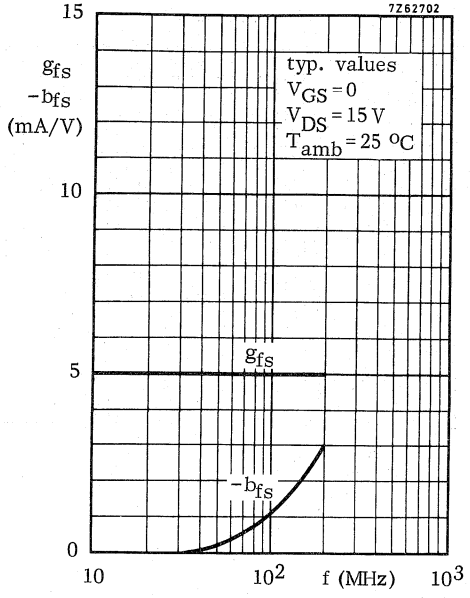

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

Fig. 11

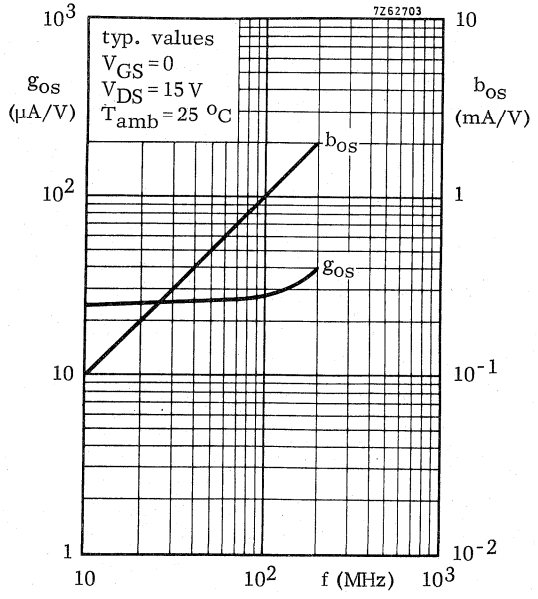

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
b_{os}
(mA/V)
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

Fig. 12

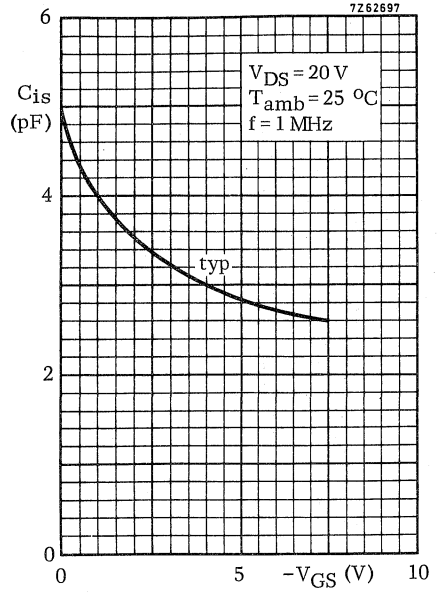


Fig. 13

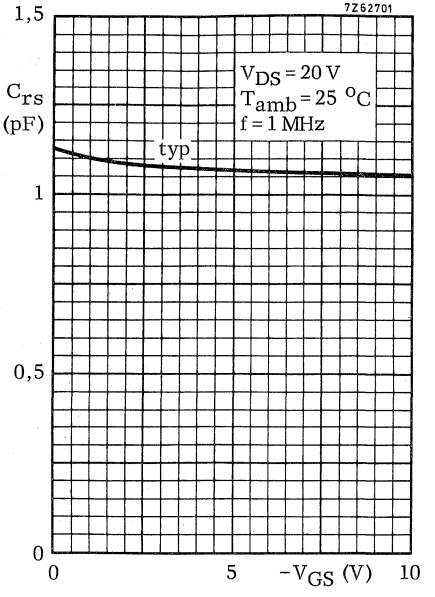


Fig. 14

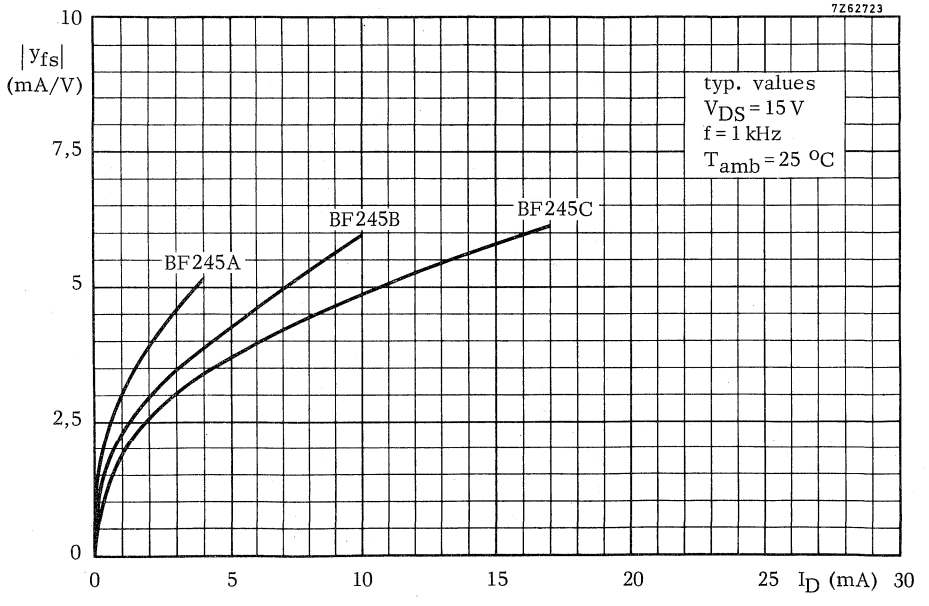


Fig. 15

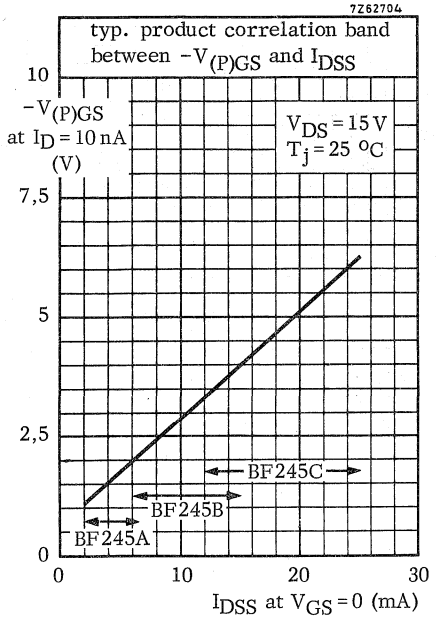


Fig. 16

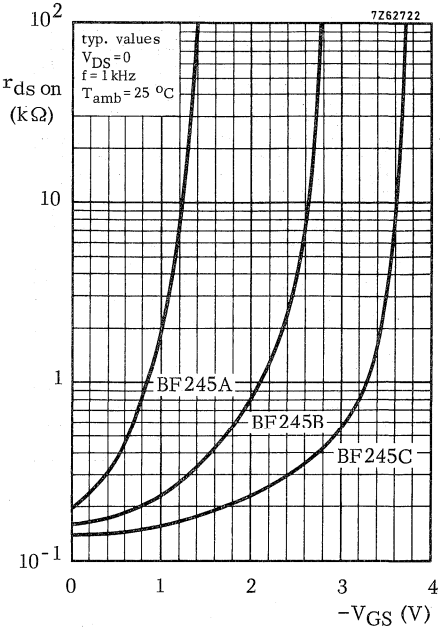


Fig. 17

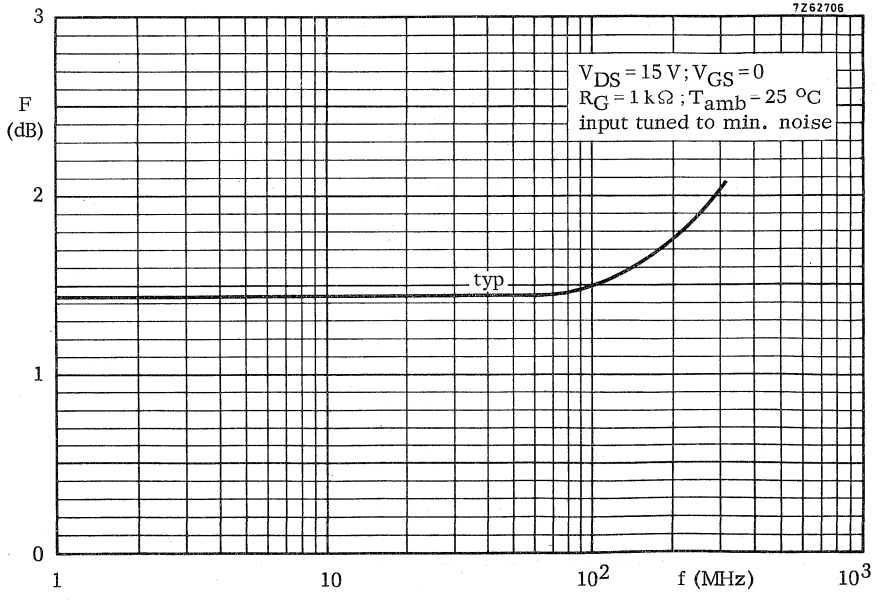


Fig. 18

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for VHF and UHF amplifiers, mixers and general purpose switching.

QUICK REFERENCE DATA

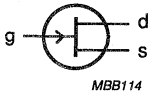
Drain-source voltage	$\pm V_{DS}$	max.			25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.			250	mW
			A	B	C	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$				0.6 to 14.5	V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.			3.5	pF
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	min.			8	mS

MECHANICAL DATA

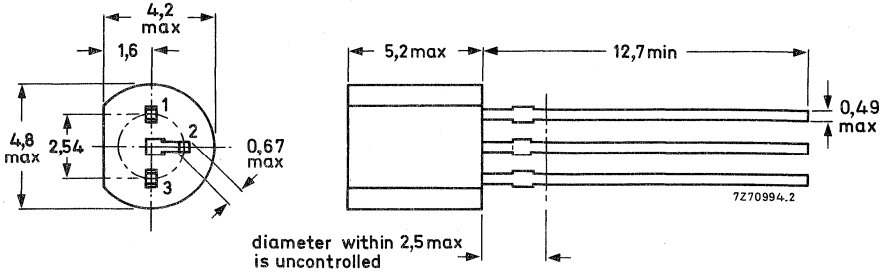
Dimensions in mm

Fig. 1 TO-92 variant.

Pinning (BF246):
1 = drain
2 = gate
3 = source



Pinning (BF247):
1 = drain
2 = source
3 = gate



Note: Drain and source are interchangeable

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate current	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

CHARACTERISTICS

T_{amb} = 25 °C

			A	B	C	
Gate cut-off current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	5	5	5	nA
Drain current* V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	min.	30	60	110	mA
		max.	80	140	250	mA
Gate-source breakdown voltage $-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	min.	25	25	25	V
Gate-source voltage I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	min.	1.5	3.0	5.5	V
		max.	4.0	7.0	12.0	V
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$			0.6 to 14.5		V
Transfer admittance (common source) I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert y_{fs} \rvert$	min.			8	mS
		typ.			17	mS
Capacitances at f = 1 MHz I_D = 10 mA; V_{DS} = 15 V						
feed-back capacitance	C_{rs}	typ.			3.5	pF
input capacitance	C_{is}	typ.			11	pF
output capacitance	C_{os}	typ.			5	pF
Cut-off frequency** V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.			450	MHz

* Measured under pulse conditions; t_p = 300 μs; $\delta \leqslant 0.02$.
** The frequency at which g_{fs} is 0.7 of its value at 1 kHz.

N-channel silicon junction field-effect transistor

BF545A; BF545B; BF545C

FEATURES

- Low leakage level (typ. 500 fA)
- High gain
- Low cut-off voltage (max. 2.2 V for BF545A).

DESCRIPTION

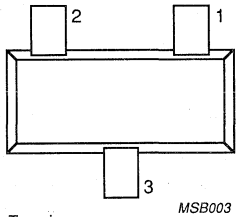
N-channel symmetrical silicon junction FETs in a surface-mountable SOT23 envelope. These devices are specially designed for use as impedance converters in (for example) electret microphones and infra-red detectors, and as VHF amplifiers in oscillators and mixers.

PINNING

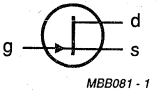
PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0			
	BF545A		2	6.5	mA
	BF545B		6	15	mA
	BF545C		12	25	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 1 μA	0.4	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	6.5	mS



Top view



Marking codes:
BF545A: M65.
BF545B: M66.
BF545C: M67.

Fig.1 Simplified outline (SOT23) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	30	V
$-V_{GSO}$	gate-source voltage		–	30	V
$-V_{GDO}$	gate-drain voltage		–	30	V
I_G	DC forward gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500 K/W

Note

1. Mounted on an FR-4 printboard.

STATIC CHARACTERISTICS

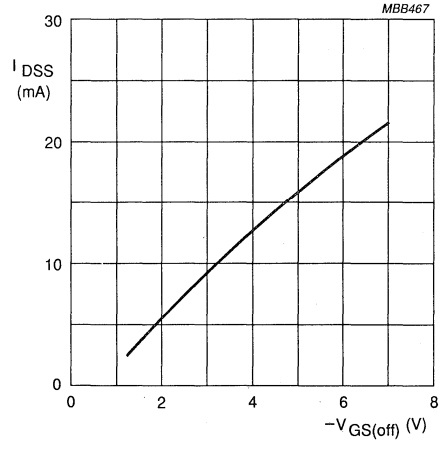
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{DS}$ = 0; $-V_{GS}$ = 20 V	–	0.5	1000	pA
		$-V_{DS}$ = 0; $-V_{GS}$ = 20 V; T_j = 125 °C	–	–	100	nA
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF545A		2	–	6.5	mA
	BF545B		6	–	15	mA
	BF545C		12	–	25	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	V_{DS} = 0; $-I_G$ = 1 µA	30	–	–	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 15 V; I_D = 200 µA				
	BF545A		0.4	–	2.2	V
	BF545B		1.6	–	3.8	V
	BF545C		3.2	–	7.8	V
		V_{DS} = 15 V; I_D = 1 µA	0.4	–	7.8	V
Y_{fs}	common source transfer admittance	V_{DS} = 15 V; V_{GS} = 0	3	–	6.5	mS
Y_{os}	common source output admittance	V_{DS} = 15 V; V_{GS} = 0	–	40	–	µS

DYNAMIC CHARACTERISTICS

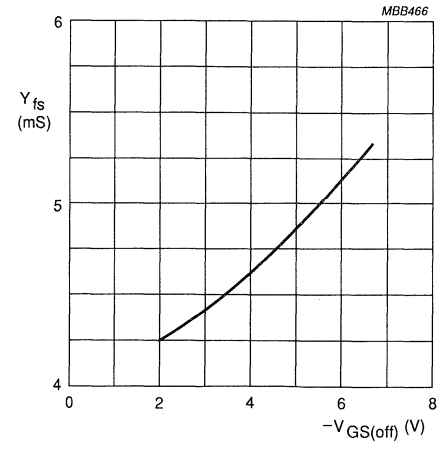
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
C_{is}	input capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	1.7	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	3	pF
C_{rs}	feedback capacitance	V_{DS} = 15 V; $-V_{GS}$ = 10 V; f = 1 MHz	0.8	pF
		V_{DS} = 15 V; $-V_{GS}$ = 0; f = 1 MHz	0.9	pF
g_{is}	common source input conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	15	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	300	µS
g_{fs}	common source transfer conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	2	mS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	1.8	mS
$-g_{rs}$	common source feedback conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	6	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	40	µS
g_{os}	common source output conductance	V_{DS} = 10 V; I_D = 1 mA; f = 100 MHz	30	µS
		V_{DS} = 10 V; I_D = 1 mA; f = 450 MHz	60	µS



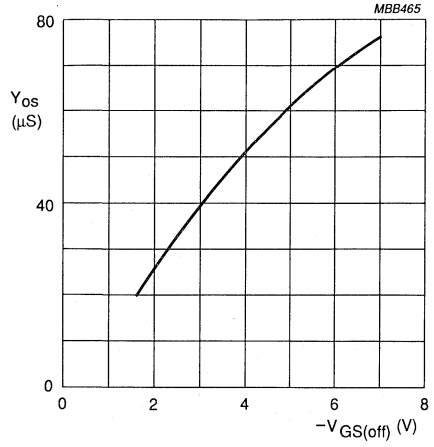
V_{DS} = 15 V; T_j = 25 °C.

Fig.2 Drain current as a function of gate-source cut-off voltage.



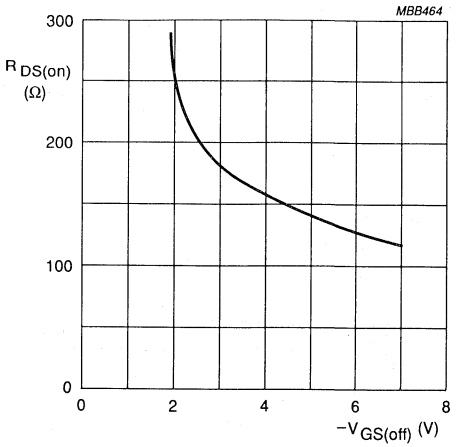
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.3 Common source transfer admittance as a function of gate-source cut-off voltage.



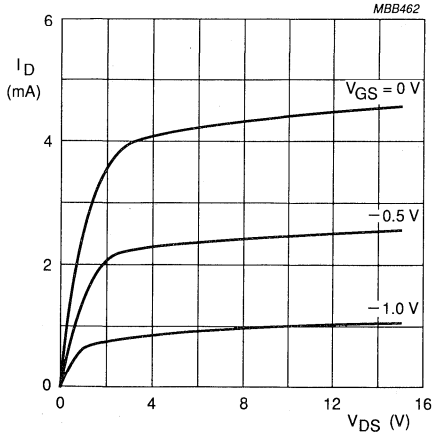
V_{DS} = 15 V; V_{GS} = 0; T_j = 25 °C.

Fig.4 Common source output admittance as a function of gate-source cut-off voltage.



V_{DS} = 100 mV; V_{GS} = 0; T_j = 25 °C.

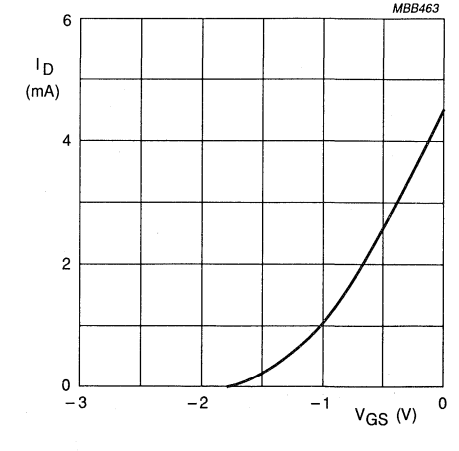
Fig.5 Drain-source on-resistance as a function of gate-source cut-off voltage.



BF545A

T_j = 25 °C.

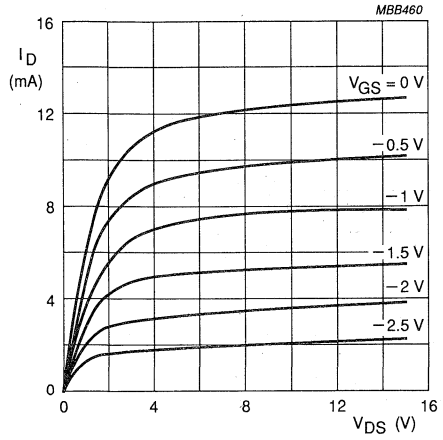
Fig.6 Typical output characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

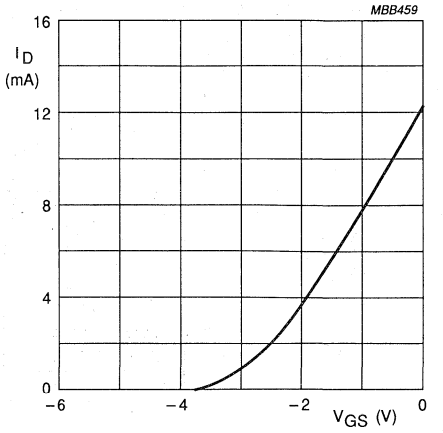
Fig.7 Typical input characteristics.



BF545B

T_j = 25 °C.

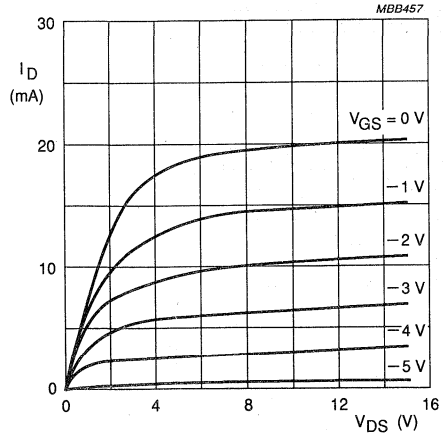
Fig.8 Typical output characteristics.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

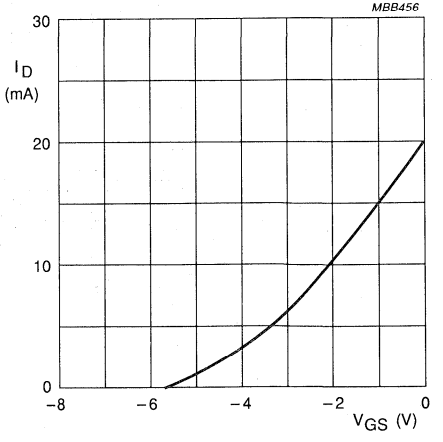
Fig.9 Typical input characteristics.



BF545C

T_j = 25 °C.

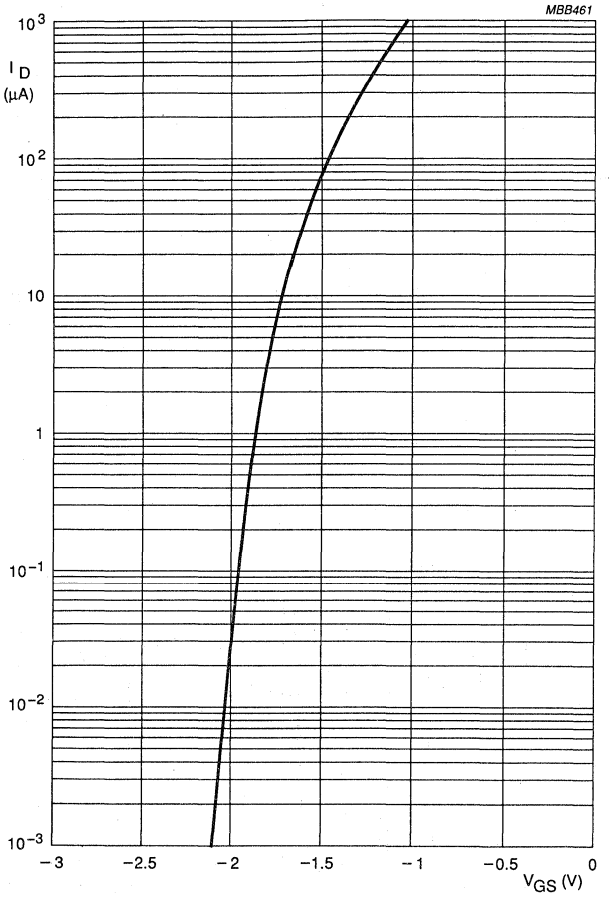
Fig.10 Typical output characteristics.



BF545C

V_{DS} = 15 V; T_j = 25 °C.

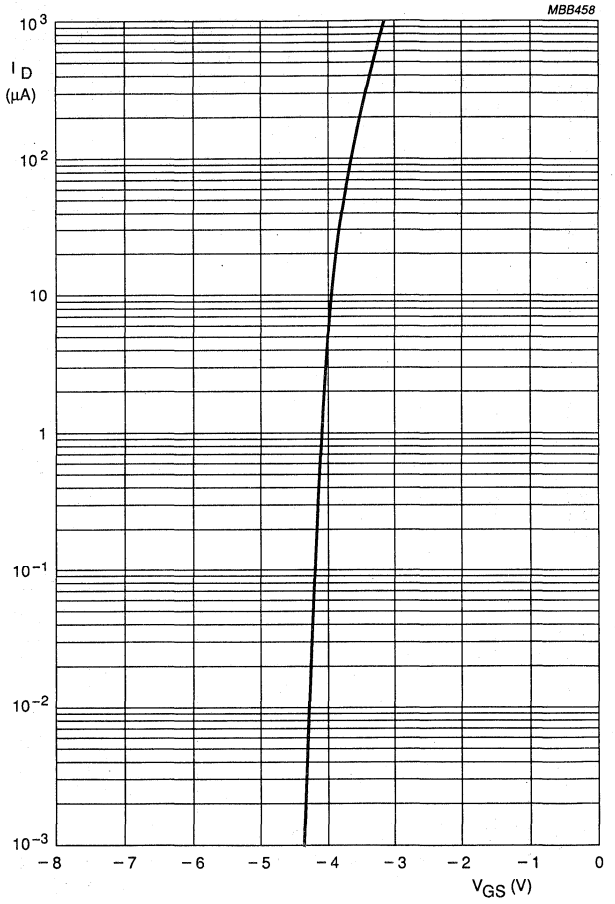
Fig.11 Typical input characteristics.



BF545A

V_{DS} = 15 V; T_j = 25 °C.

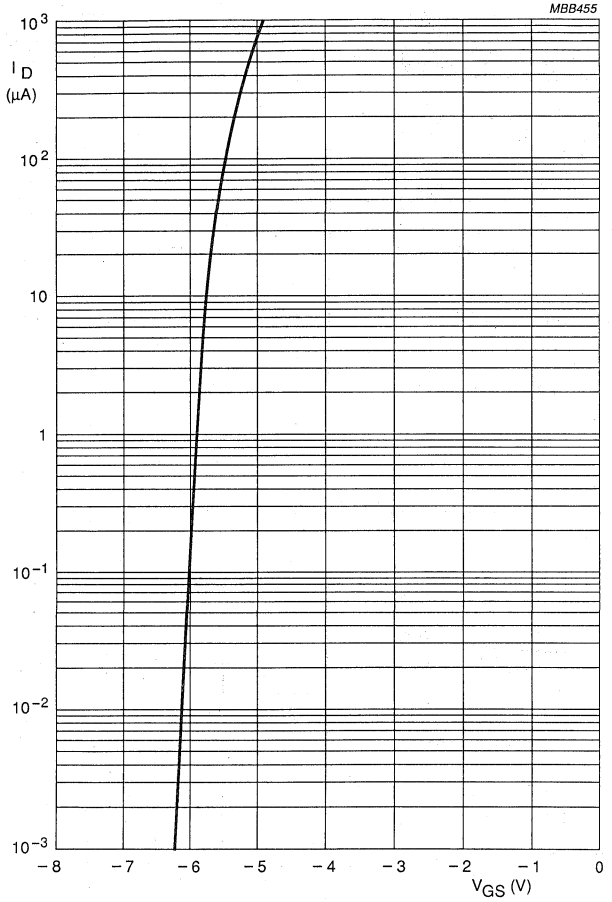
Fig.12 Drain current as a function of gate-source voltage; typical values.



BF545B

V_{DS} = 15 V; T_j = 25 °C.

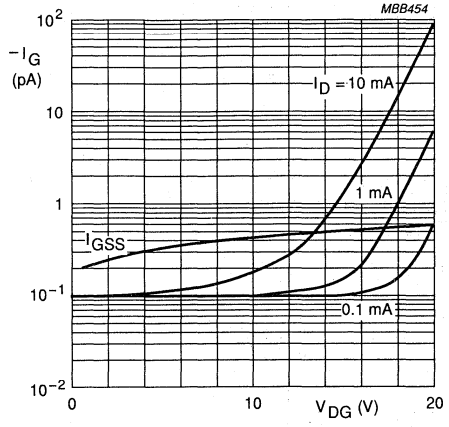
Fig.13 Drain current as a function of gate-source voltage; typical values.



BF545C

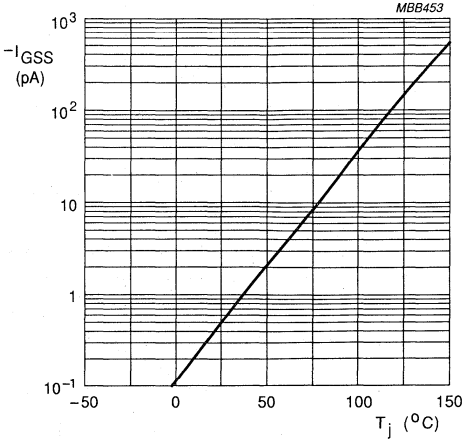
V_{DS} = 15 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage; typical values.



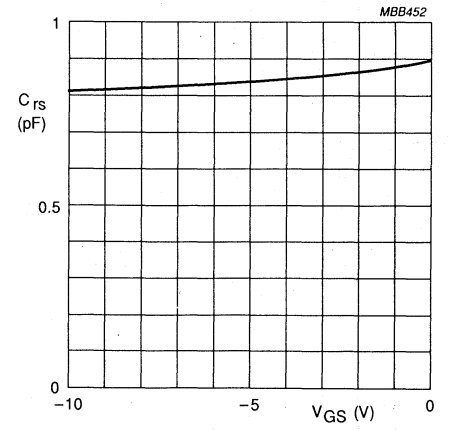
I_D = 10 mA (BF545B and C only); T_j = 25 °C.

Fig.15 Gate current as a function of drain-gate voltage, typical values.



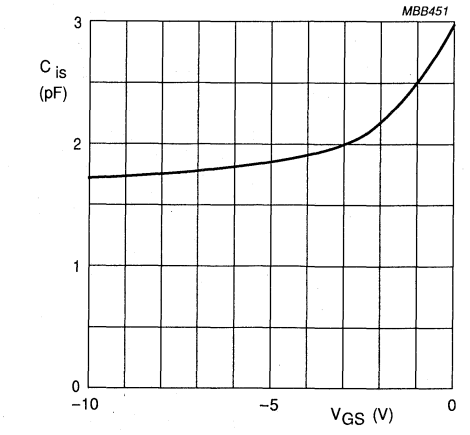
V_{DS} = 0; $-V_{GS}$ = 20 V.

Fig.16 Gate current as a function of junction temperature, typical values.



V_{DS} = 15 V; T_j = 25 °C.

Fig.17 Typical feedback capacitance.



V_{DS} = 15 V; T_j = 25 °C.

Fig.18 Typical input capacitance.

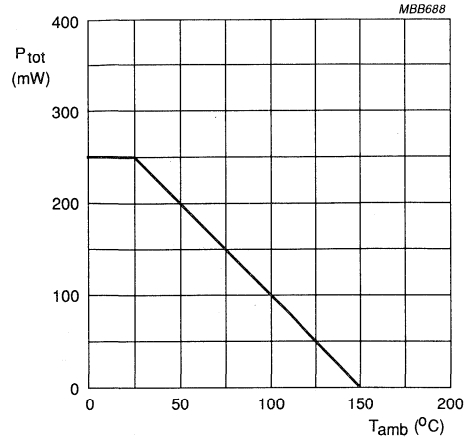
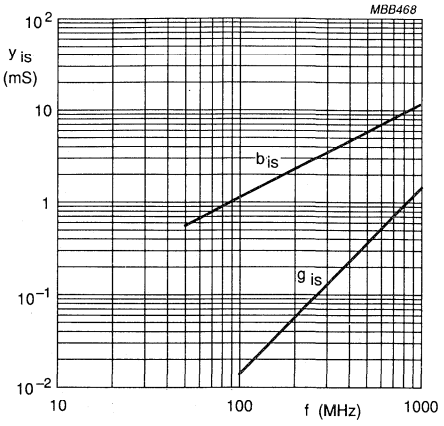
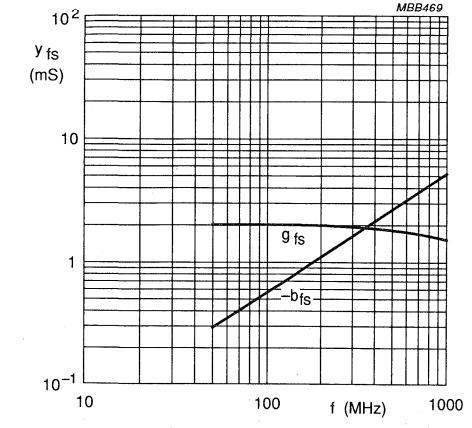


Fig.19 Power derating curve.



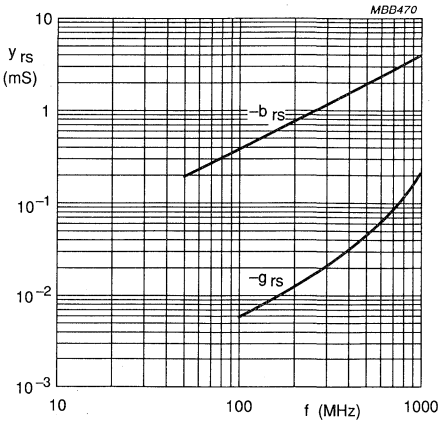
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.20 Common source input conductance.



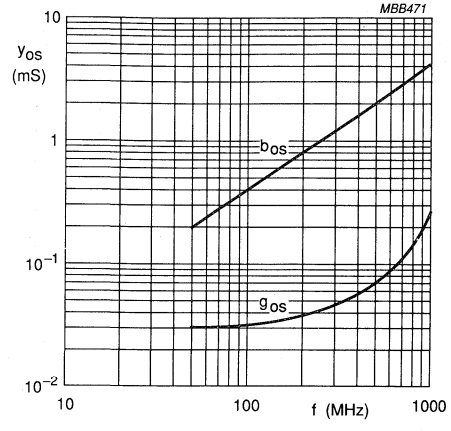
V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.21 Common source transfer conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.22 Common source feedback conductance.



V_{DS} = 10 V; I_D = 1 mA; T_{amb} = 25 °C.

Fig.23 Common source output conductance.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected. This MOS-FET tetrode is intended for use in v.h.f. applications, such as v.h.f. television tuners, FM tuners with a 12 volt supply voltage. The device is also suitable for use in professional communication equipment.

The device is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	40 mA
Total power dissipation up to T_{amb} = 60 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	150 °C
Transfer admittance at f = 1 kHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs}\rvert$	typ.	25 mS
Input capacitance at gate 1; f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	$C_{ig1\text{-}s}$	typ.	4 pF
Feedback capacitance at f = 1 MHz I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	30 fF
Noise figure at G_S = 2 mS I_D = 15 mA; V_{DS} = 10 V; + $V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	1.2 dB

MECHANICAL DATA

Fig.1 SOT143.

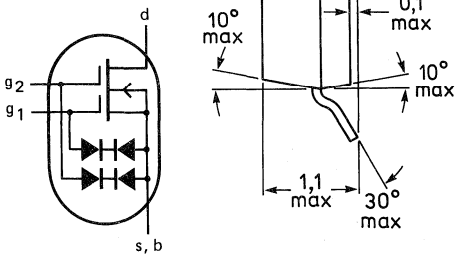
Dimensions in mm

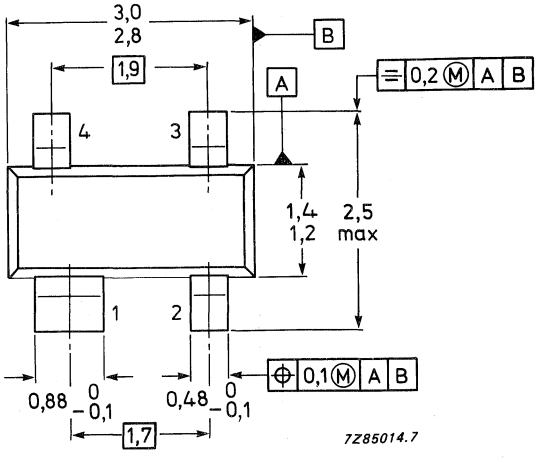
Marking code:

BF992 = M92

Pinning:

1 = source
2 = drain
3 = gate 2
4 = gate 1





TOP VIEW

See also *Soldering recommendations.*

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (DC or average)	I_D	max.	40	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 60 °C (note 1)	P_{tot}	max.	200	mW
Storage temperature range	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air (note 1)	$R_{th\ j-a}$	=	460	K/W

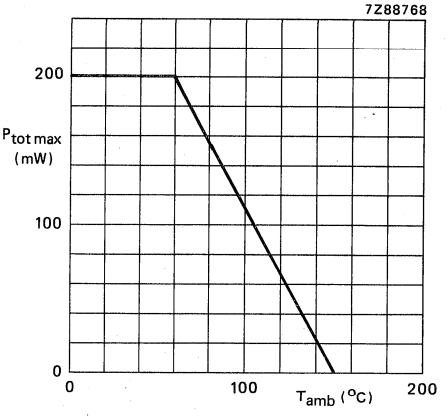


Fig.2 Power derating curve.

Note

1. Device mounted on a ceramic substrate of 8 mm x 10 mm x 0.7 mm.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S}$ = 7 V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	max.	25 nA
$\pm V_{G2-S}$ = 7 V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	max.	25 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS}$ = 10 mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		8 to 20 V
$\pm I_{G2-SS}$ = 10 mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		8 to 20 V
Gate-source cut-off voltages			
I_D = 20 μA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$		0.2 to 1.3 V
I_D = 20 μA; V_{DS} = 10 V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$		0.2 to 1.1 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 15 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	min. typ.	20 mS 25 mS
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	4 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1.7 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ. max.	30 fF 40 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	2 pF
Noise figure at f = 200 MHz; G_S = 2 mS	F	typ.	1.2 dB

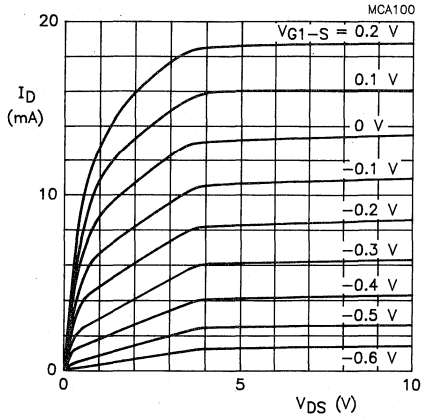


Fig.2 Output characteristics.

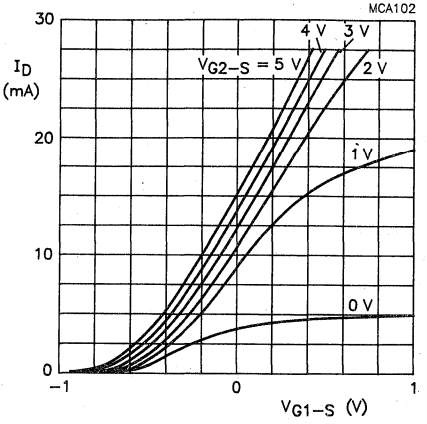


Fig.3 Transfer characteristics.

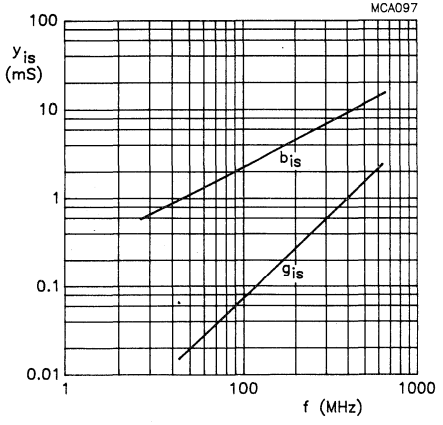


Fig.4 Input admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

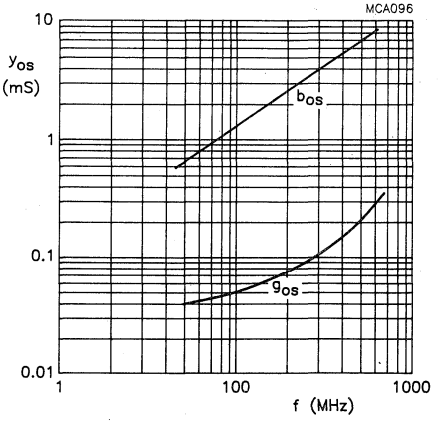


Fig.5 Output admittance as a function of frequency; V_{DS} = 10 V; V_{G2-S} = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

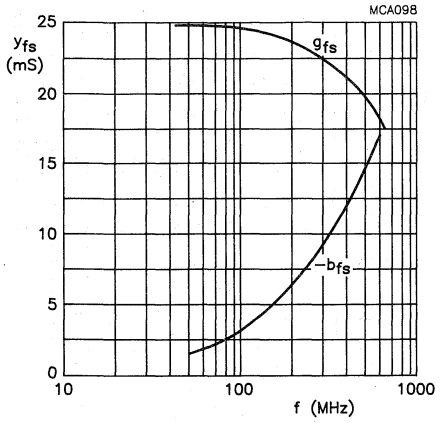


Fig.6 Transfer admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

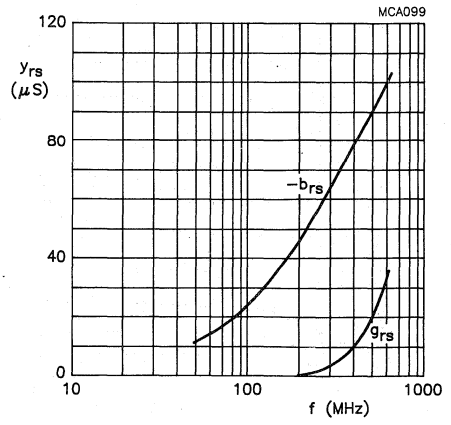


Fig.7 Feedback admittance as a function of frequency; V_{DS} = 10 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; T_{amb} = 25 °C; typical values.

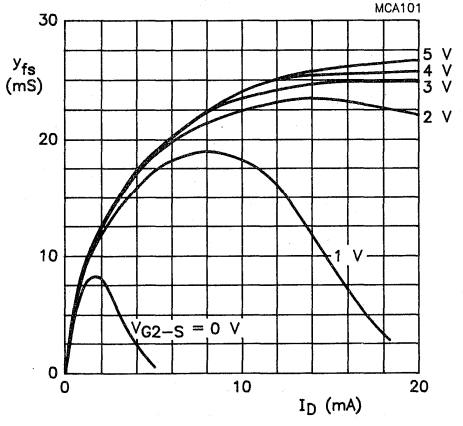


Fig.8 Transfer admittance as a function of drain current.

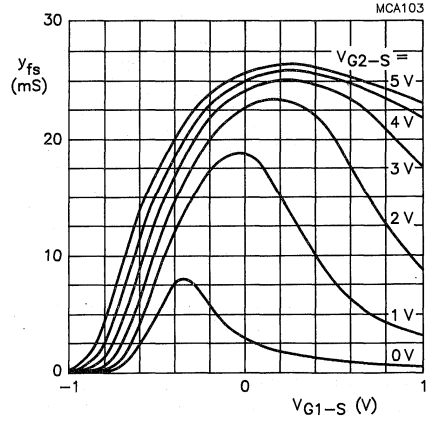


Fig.9 Transfer admittance as a function of gate 2 source voltage.

Data sheet	
status	Preliminary specification
date of issue	April 1991

BF998

Silicon n-channel dual gate MOS-FET

FEATURES

- Short channel transistor with high ratio $|Y_{fs}|/C_{is}$.
- Low noise gain controlled amplifier to 1 GHz.

DESCRIPTION

Depletion type field-effect transistor in a plastic SOT143 microminiature envelope with source and substrate interconnected, intended for VHF and UHF applications, such as television tuners, with 12 V supply voltage and professional communication equipment. This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	-	12	V
I_D	drain current	-	30	mA
P_{tot}	total power dissipation	-	200	mW
T_j	junction temperature	-	150	°C
$\|Y_{fs}\|$	transfer admittance	24	-	mS
C_{ig1-s}	input capacitance at gate 1	2.1	-	pF
C_{rs}	feedback capacitance	25	-	fF
F	noise figure at 800 MHz	1	-	dB

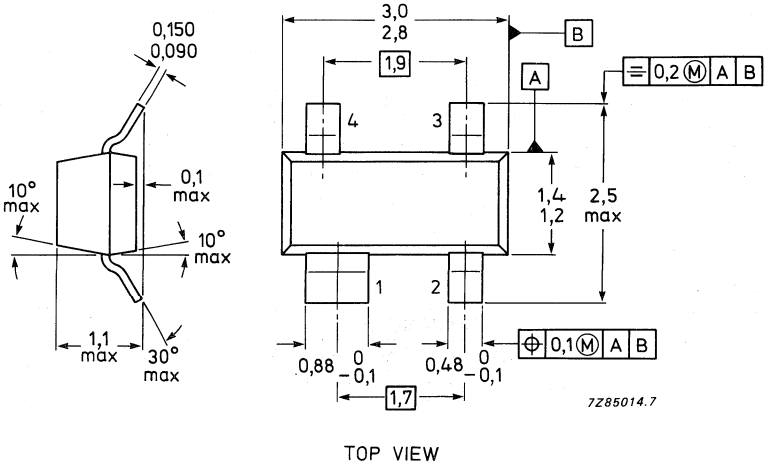
Silicon n-channel dual gate MOS-FET BF998

MECHANICAL DATA

Dimensions in mm

Marking code

BF998 = MOp



TOP VIEW

See also soldering recommendations.

Fig.1 SOT143.

PIN CONFIGURATION

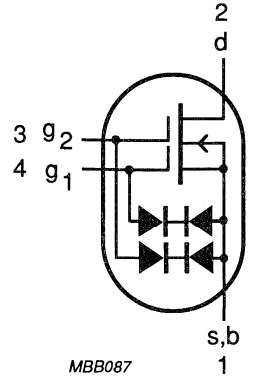


Fig.2 Pin configuration.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		-	12	V
I_D	drain current (DC or average)		-	30	mA
$\pm I_{G1-S}$	gate 1-source current		-	10	mA
$\pm I_{G2-S}$	gate 2-source current		-	10	mA
P_{tot}	total power dissipation	T_{amb} = 60 °C (note 1)	-	200	mW
P_{tot}	total power dissipation	T_{amb} = 50 °C (note 2)	-	200	mW
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient in free air (note 1)	460	K/W
$R_{th\ j-a}$	from junction to ambient in free air (note 2)	500	K/W

Notes

1. Device mounted on a ceramic substrate, 8 mm x 10 mm x 0.7 mm.
2. Device mounted on printed circuit board.

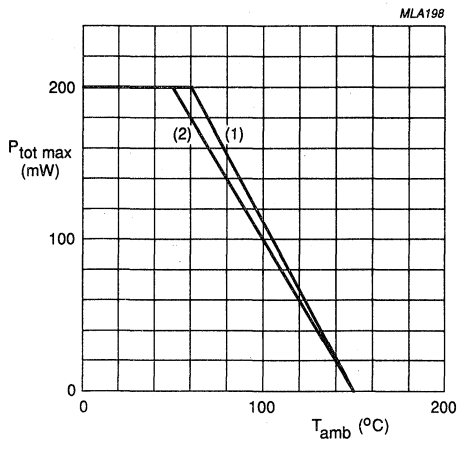


Fig.3 Power derating curve;
(1) ceramic substrate;
(2) printed-circuit board.

Silicon n-channel dual gate MOS-FET BF998

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1-SS}$	gate 1 cut-off current	$\pm V_{G1-S}$ = 5 V $V_{G2S} = V_{DS}$ = 0	-	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$\pm V_{G2-S}$ = 5 V $V_{G1S} = V_{DS}$ = 0	-	50	nA
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$\pm I_{G1-SS}$ = 10 mA $V_{G2-S} = V_{DS}$ = 0	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$\pm I_{G2-SS}$ = 10 mA $V_{G1-S} = V_{DS}$ = 0	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V $+V_{G2-S}$ = 4 V	-	2.5	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	I_D = 20 µA V_{DS} = 8 V V_{G1-S} = 0	-	2.0	V
I_{DSS}	drain current (measured under pulse condition)	V_{DS} = 8 V V_{G1-S} = 0 $+V_{G2-S}$ = 4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source) I_D = 10 mA; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs} \rvert$	transfer admittance	f = 1 kHz	21	24	-	mS
C_{ig1-s}	input capacitance at gate 1	f = 1 MHz	-	2.1	2.5	pF
C_{os}	output capacitance	f = 1 MHz	-	1.05	-	pF
C_{rs}	feedback capacitance	f = 1 MHz	-	25	-	fF
C_{ig2-s}	input capacitance at gate 2	f = 1 MHz	-	1.2	-	pF
F	noise figure	f = 200 MHz G_s = 2 mS $B_s = B_{sopt}$	-	0.6	-	dB
F	noise figure	f = 800 MHz G_s = 3.3 mS $B_s = B_{sopt}$	-	1	-	dB

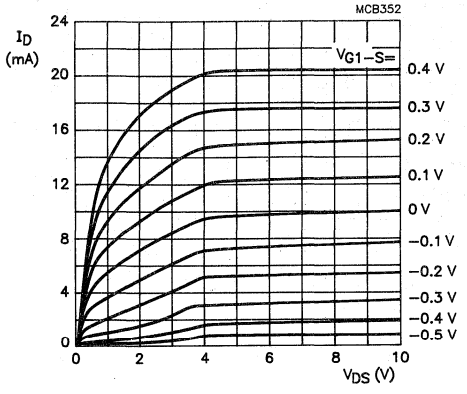


Fig.4 Output characteristics; V_{G2-S} = 4 V; T_{amb} = 25 °C.

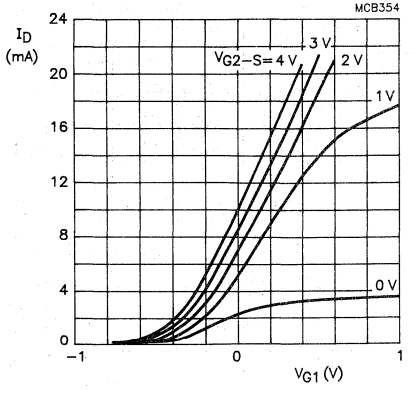


Fig.5 Transfer characteristics; V_{DS} = 8 V; T_{amb} = 25 °C.

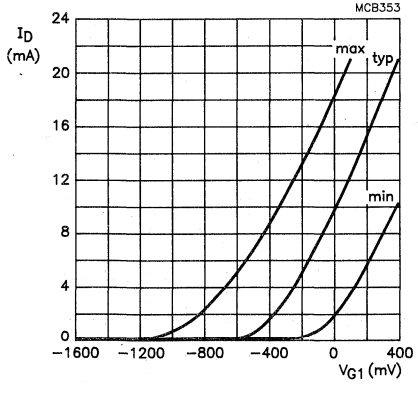


Fig.6 Drain current as a function of gate 1 voltage; V_{DS} = 8 V; V_{G2-S} = 4 V; T_{amb} = 25 °C.

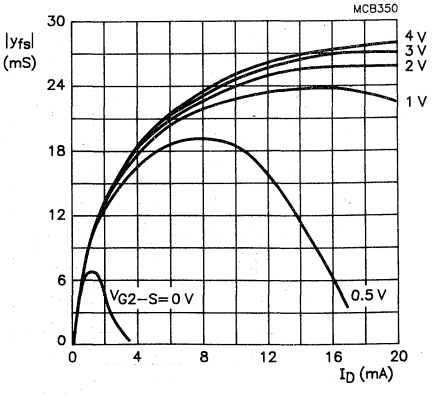


Fig.7 Transfer admittance as a function of drain current; V_{DS} = 8 V; T_{amb} = 25 °C.

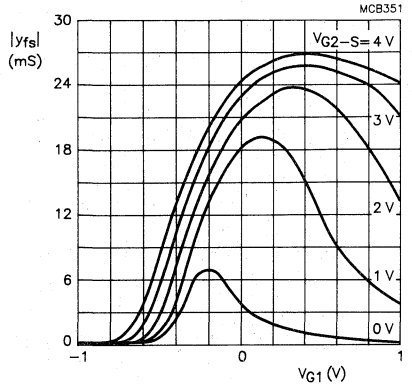


Fig.8 Transfer admittance as a function of gate 1 voltage; V_{DS} = 8 V; T_{amb} = 25 °C.

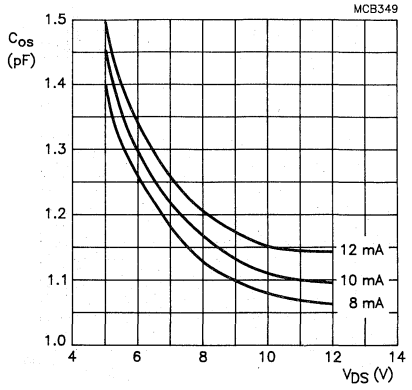


Fig.9 Output capacitance as a function of drain-source voltage; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

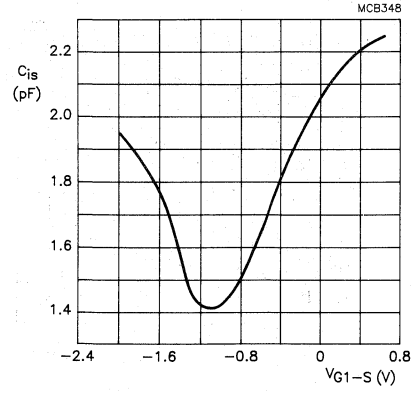


Fig.10 Gate 1 input capacitance as a function of gate 1-source voltage; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; f = 1 MHz; T_{amb} = 25 °C.

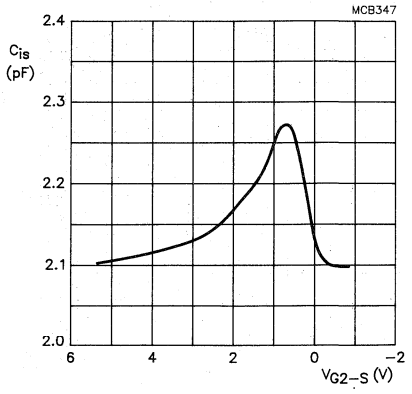


Fig.11 Gate 1 input capacitance as a function of gate 2-source voltage; V_{DS} = 8 V; $V_{G1\text{-}S}$ = 0; f = 1 MHz; T_{amb} = 25 °C.

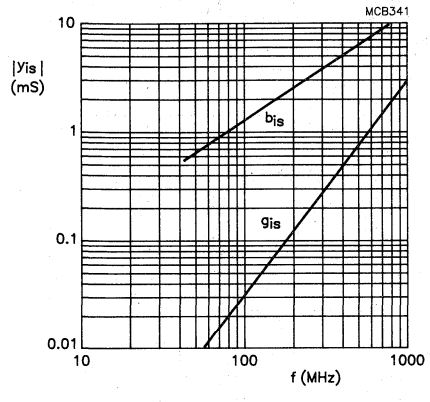


Fig.12 Input admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

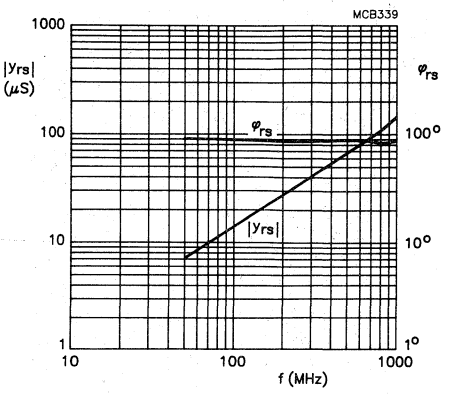


Fig.13 Feedback admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

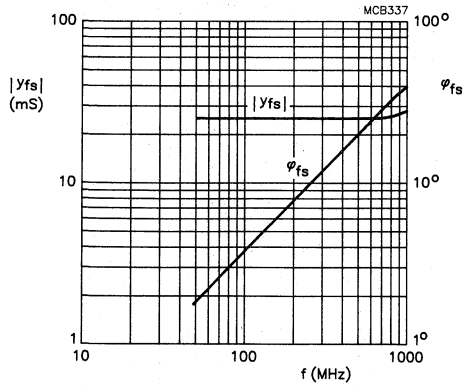


Fig.14 Transfer admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.

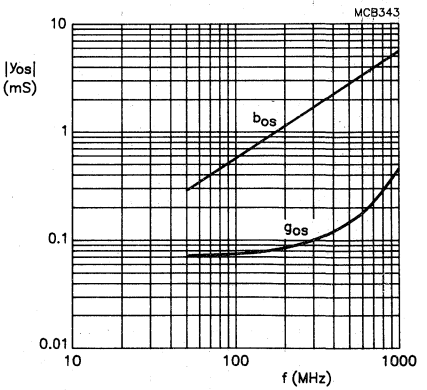
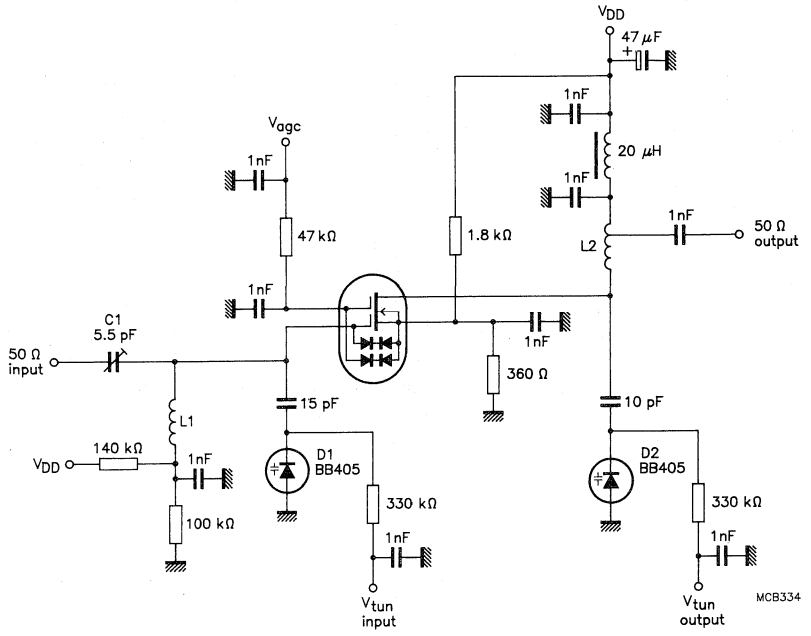
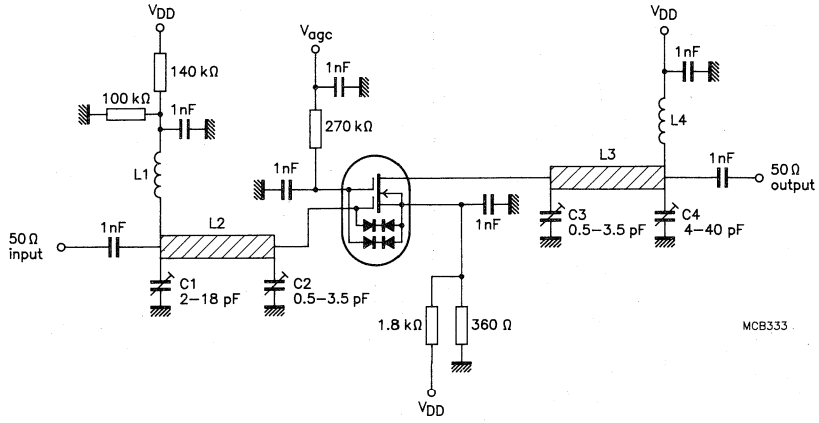


Fig.15 Output admittance as a function of frequency; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V; I_D = 10 mA; T_{amb} = 25 °C.



L1 = 45 nH, 4 turns, internal diameter 4 mm, 0.8 mm copper wire.
L2 = 160 nH, 3 turns, internal diameter 8 mm, 0.8 mm copper wire.
Tapped at approximately half a turn from the cold side, to adjust G_L = 0.5 mS.
C1 adjusted for G_S = 2 mS.

Fig.16 Gain control test circuit at f = 200 MHz; V_{DD} = 12 V; G_S = 2 mS; G_L = 0.5 mS.



L1 = L4 = 11 turns, internal diameter 3 mm, 0.5 mm copper wire, without spacing; ≈200 nH.
L2 = 2 cm, silvered 0.8 mm copper wire, 4 mm above ground plane.
L3 = 2 cm, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.17 Gain control test circuit at f = 800 MHz; V_{DD} = 12 V; G_S = 3.3 mS; G_L = 1 mS.

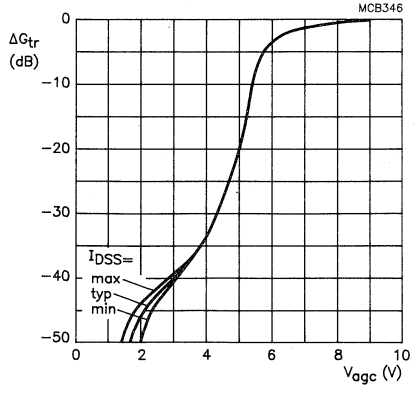


Fig.18 Automatic gain control characteristics measured in circuit of Fig.16; V_{DD} = 12 V; f = 200 MHz; T_{amb} = 25 °C.

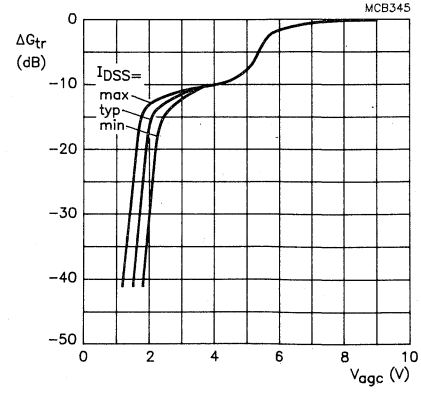


Fig.19 Automatic gain control characteristics measured in circuit of Fig.17; V_{DD} = 12 V; f = 800 MHz; T_{amb} = 25 °C.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	October 1990

J108/J109/J110
N-channel junction FETs

FEATURES

- High speed switching
- Interchangeability of drain and source connections
- Low $R_{DS(on)}$ at zero gate voltage (< 8 Ω for J108)

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT54 envelope. They are intended for use in applications such as analog switches, choppers and commutators.

PINNING - SOT54

PIN	DESCRIPTION
1	gate
2	source
3	drain

Note

1. Drain and source are interchangeable.

PIN CONFIGURATION

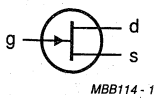


Fig 1. Symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		-	25	V
$-V_{GSO}$	gate-source voltage		-	25	V
$-V_{GDO}$	gate-drain voltage		-	25	V
I_G	forward gate current	DC	-	50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 50$ °C	-	400	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		-	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	250	K/W

STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
$-I_{GSS}$	reverse gate current	$-V_{GS}$ = 15 V V_{DS} = 0		-	3	nA
I_{DSX}	drain-source cut-off current	$-V_{GS}$ = 10 V V_{DS} = 5 V		-	3	nA
I_{DSS}	drain current	V_{GS} = 0 V_{DS} = 15 V	J108 J109 J110	80 40 10	- - -	mA
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 µA V_{DS} = 0		-	25	V
$-V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 µA V_{DS} = 5 V	J108 J109 J110	3 2 0.5	10 6 4	V
$R_{DS(on)}$	drain-source on-resistance	V_{GS} = 0 V V_{DS} = 0.1 V	J108 J109 J110	- - -	8 12 18	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	15	30	pF
C_{is}	input capacitance	V_{DS} = 0 $-V_{GS}$ = 0 f = 1 MHz T_{amb} = 25 °C	50	85	pF
C_{rs}	feedback capacitance	V_{DS} = 0 $-V_{GS}$ = 10 V f = 1 MHz	8	15	pF
Switching times (see Fig.2)					
t_d	delay time	note 1	2	-	ns
t_{on}	turn-on time	note 1	4	-	ns
t_s	storage time	note 1	4	-	ns
t_{off}	turn-off time	note 1	6	-	ns

Notes

1. Test conditions for switching times are as follows:
   V_{DD} = 1.5 V, V_{GS} = 0 to $-V_{GS(off)}$ (all types);
   $-V_{GS(off)}$ = 12 V, R_L = 100 Ω (J108);
   $-V_{GS(off)}$ = 7 V, R_L = 100 Ω (J109);
   $-V_{GS(off)}$ = 5 V, R_L = 100 Ω (J110).

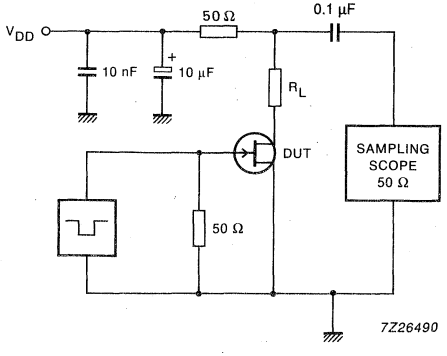


Fig.2 Switching circuit.

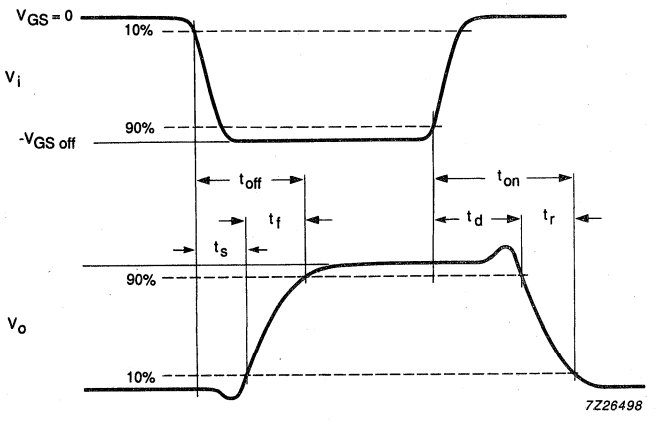


Fig.3 Input and output waveforms.

N-channel silicon field-effect transistors

J308/309/310

FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a TO-92 envelope. They are intended for use in the AM input stage in car radios and in UHF/VHF amplifiers, oscillators and mixers.

PIN CONFIGURATION

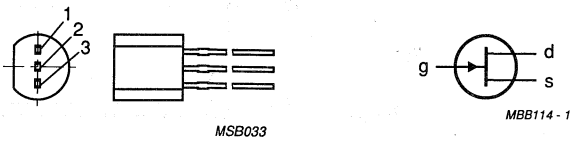


Fig.1 Simplified outline and symbol.

PINNING - TO-92

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	J308		12	60	mA
	J309		12	30	mA
	J310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA			
	J308		1	6.5	V
	J309		1	4	V
	J310		2	6.5	V
Y_{fs}	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 50 °C	–	400	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	250	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm, mounting pad for the drain lead minimum 10 mm².

STATIC CHARACTERISTICS

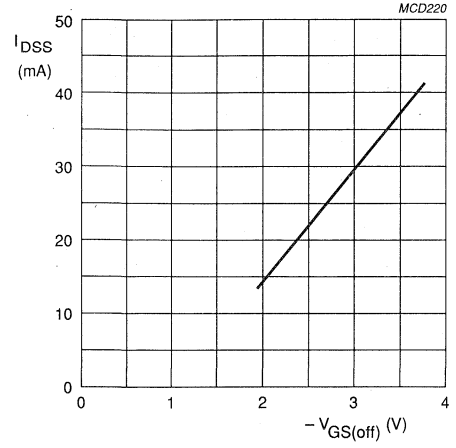
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	J308		12	–	60	mA
	J309		12	–	30	mA
	J310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	J308		1	–	6.5	V
	J309		1	–	4	V
	J310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\|Y_{os}\|$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

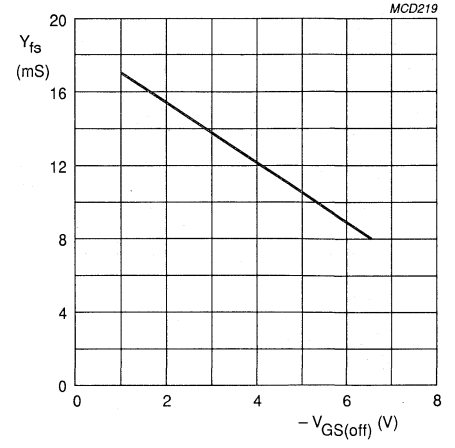
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\bar{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

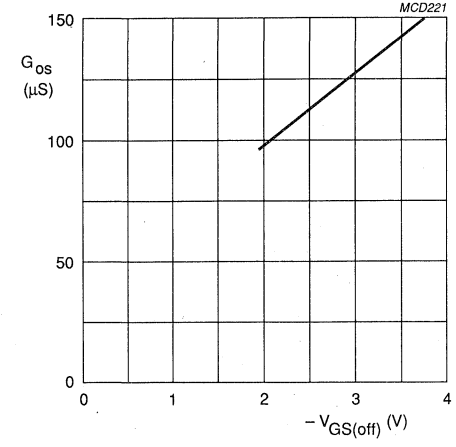
Fig.2 Drain current as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

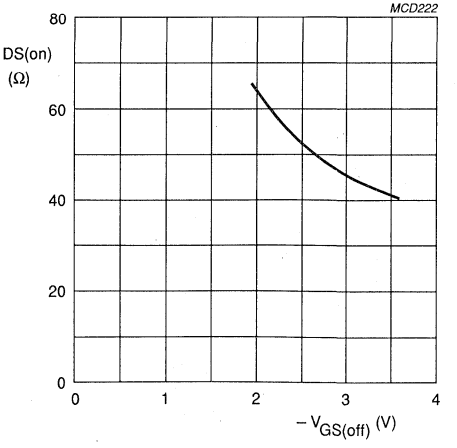
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

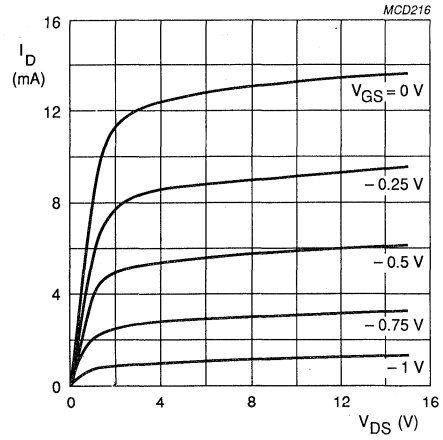
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



J308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

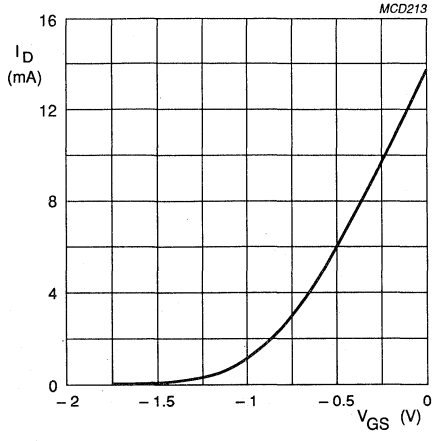
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



J308.

T_j = 25 °C.

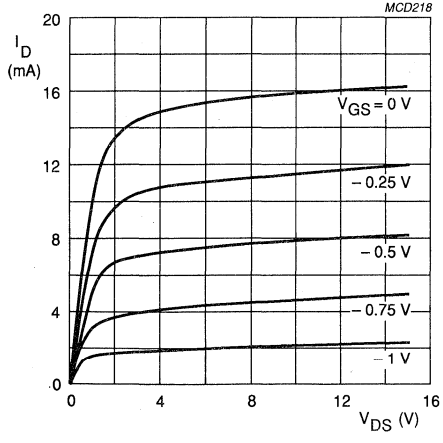
Fig.6 Output characteristics, typical values.



J308.

V_{DS} = 10 V; T_j = 25 °C.

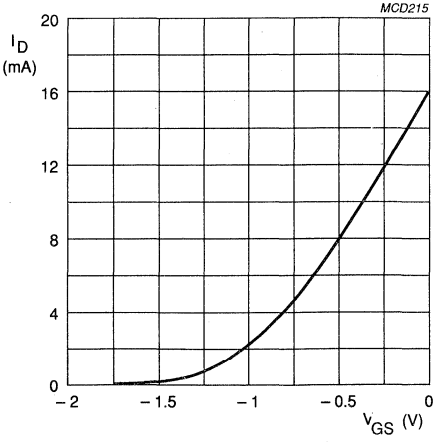
Fig.7 Input characteristics, typical values.



J309.

T_j = 25 °C.

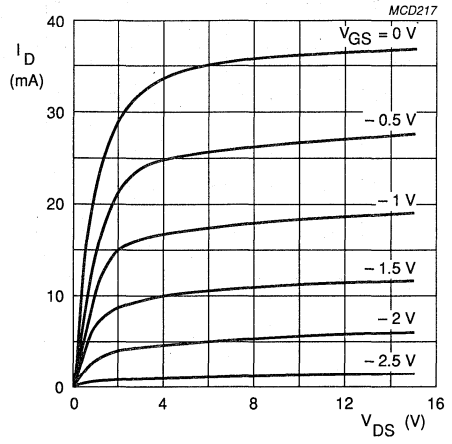
Fig.8 Output characteristics, typical values.



J309.

V_{DS} = 10 V; T_j = 25 °C.

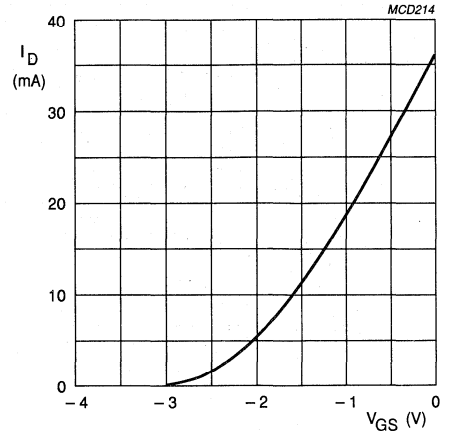
Fig.9 Input characteristics, typical values.



J310.

T_j = 25 °C.

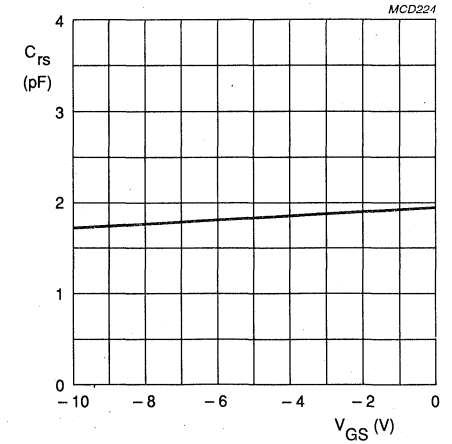
Fig.10 Output characteristics, typical values.



J310.

V_{DS} = 10 V; T_j = 25 °C.

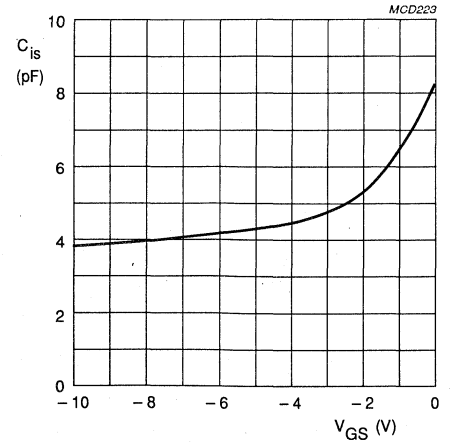
Fig.11 Input characteristics, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

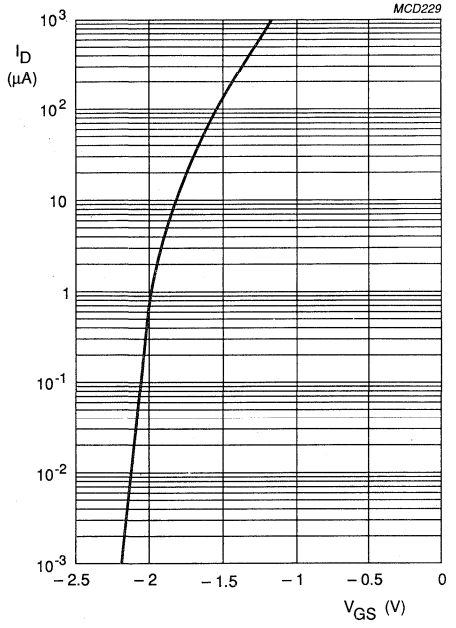
Fig.12 Feedback capacitance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

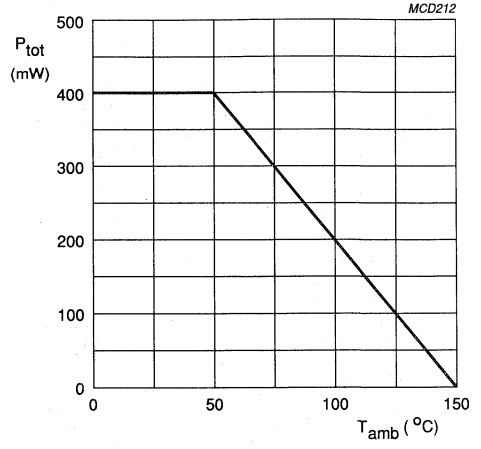
Fig.13 Input capacitance, typical values.



J308, 309 & 310.

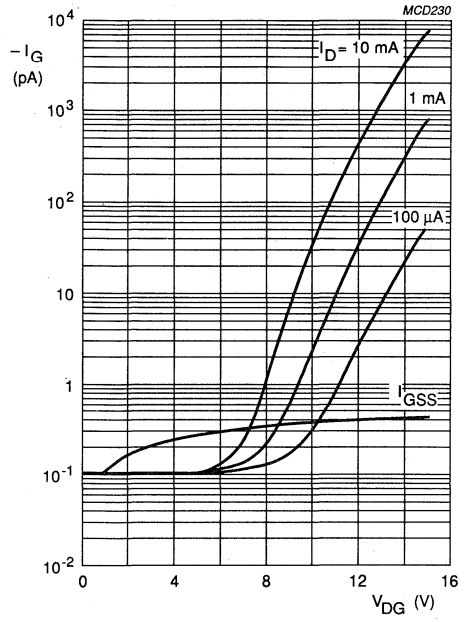
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



J308, 309 & 310.

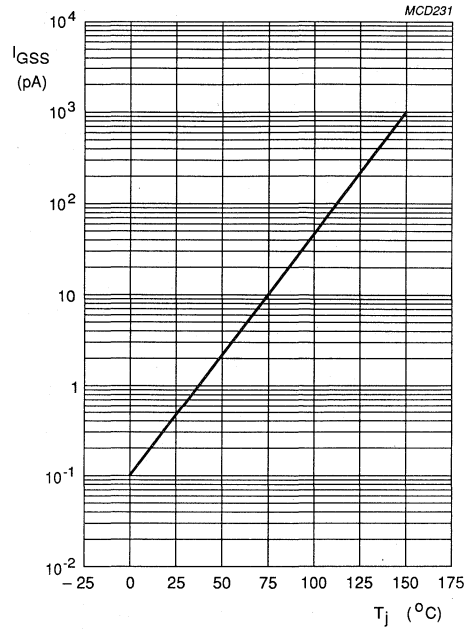
Fig.15 Power derating curve.



J308, 309 & 310.

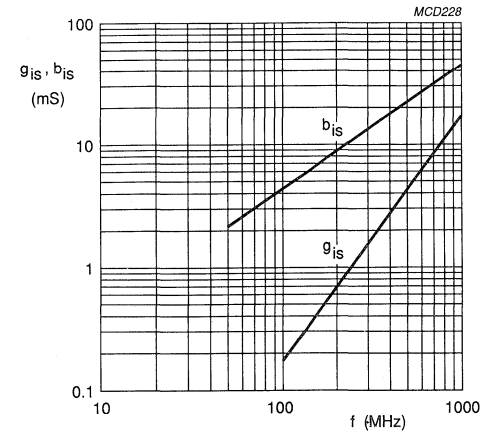
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



J308, 309 & 310.

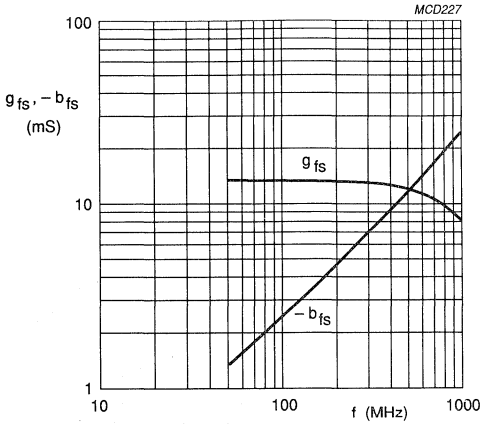
Fig.17 Gate current as a function of junction temperature, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

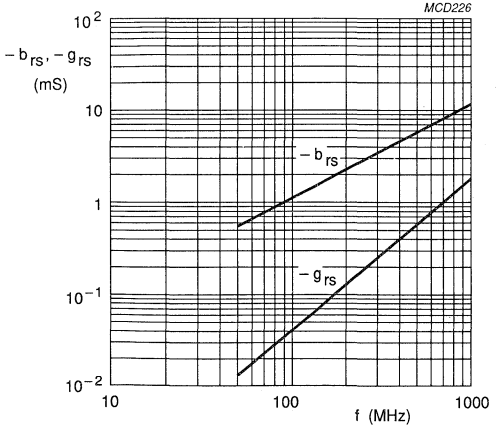
Fig.18 Input admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

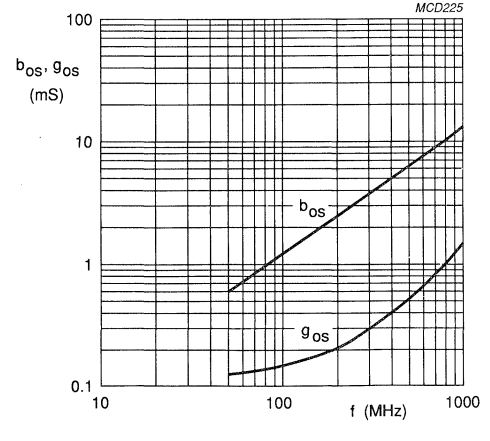
Fig.19 Forward admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



J308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

N-channel silicon field-effect transistors

PMBFJ308/309/310

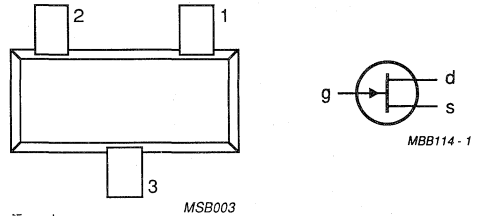
FEATURES

- Low noise
- Interchangeability of drain and source connections
- High gain.

DESCRIPTION

Silicon symmetrical n-channel junction FETs in a SOT23 envelope. They are intended for use in VHF amplifiers, the AM input stage of car radios, oscillators and mixers.

PIN CONFIGURATION



Marking codes:
PMBFJ308: M08.
PMBFJ309: M09.
PMBFJ310: M10.

Top view

Fig.1 Simplified outline and symbol.

PINNING - SOT23

PIN	DESCRIPTION
1	source
2	drain
3	gate

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0			
	PMBFJ308		12	60	mA
	PMBFJ309		12	30	mA
	PMBFJ310		24	60	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 µA			
	PMBFJ308		1	6.5	V
	PMBFJ309		1	4	V
	PMBFJ310		2	6.5	V
$\|Y_{fs}\|$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{DS}$	drain-source voltage		–	25	V
$-V_{GSO}$	gate-source voltage		–	25	V
$-V_{GDO}$	gate-drain voltage		–	25	V
I_G	forward gate current	DC value	–	50	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

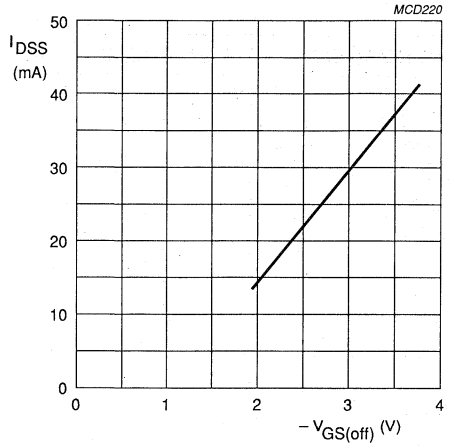
T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)GSS}$	gate-source breakdown voltage	$-I_G$ = 1 μA V_{DS} = 0	–	–	25	V
I_{DSS}	drain current	V_{DS} = 10 V; V_{GS} = 0				
	PMBFJ308		12	–	60	mA
	PMBFJ309		12	–	30	mA
	PMBFJ310		24	–	60	mA
$-I_{GSS}$	reverse gate leakage current	$-V_{GS}$ = 15 V; V_{DS} = 0	–	–	1	nA
V_{GSS}	gate-source forward voltage	V_{DS} = 0; I_G = 1 mA	–	–	1	V
$-V_{GS(off)}$	gate-source cut-off voltage	V_{DS} = 10 V; I_D = 1 μA				
	PMBFJ308		1	–	6.5	V
	PMBFJ309		1	–	4	V
	PMBFJ310		2	–	6.5	V
$R_{DS(on)}$	drain-source on-resistance	V_{DS} = 100 mV; V_{GS} = 0	–	50	–	Ω
$\lvert Y_{fs} \rvert$	common-source transfer admittance	V_{DS} = 10 V; I_D = 10 mA	10	–	–	mS
$\lvert Y_{os} \rvert$	common-source output admittance	V_{DS} = 10 V; I_D = 10 mA	–	–	250	μS

DYNAMIC CHARACTERISTICS

T_j = 25 °C.

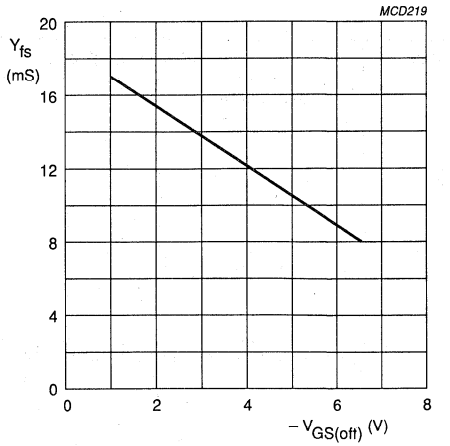
SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 10 V; $-V_{GS}$ = 10 V; f = 1 MHz	3	5	pF
		V_{DS} = 10 V; $-V_{GS}$ = 0; T_{amb} = 25 °C	6	–	pF
C_{rs}	feedback capacitance	V_{DS} = 0; $-V_{GS}$ = 10 V; f = 1 MHz	1.3	2.5	pF
g_{is}	common-source input conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	200	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	3	–	mS
g_{fs}	common-source transfer conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	13	–	mS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	12	–	mS
$-g_{rs}$	common-source feedback conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	30	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	450	–	µS
g_{os}	common-source output conductance	V_{DS} = 10 V; I_D = 10 mA; f = 100 MHz	150	–	µS
		V_{DS} = 10 V; I_D = 10 mA; f = 450 MHz	400	–	µS
$\overline{e}_n$	equivalent input noise voltage	V_{DS} = 10 V; I_D = 10 mA; f = 100 Hz	6	–	$\frac{nV}{\sqrt{Hz}}$



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

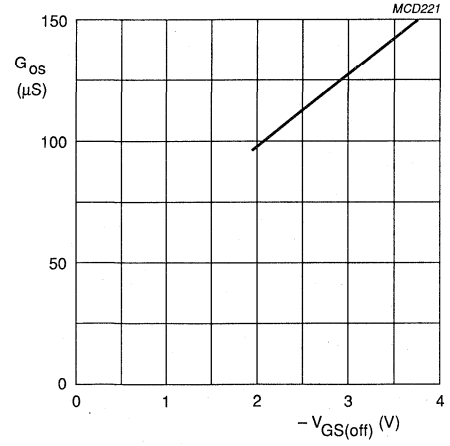
Fig.2 Drain current as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

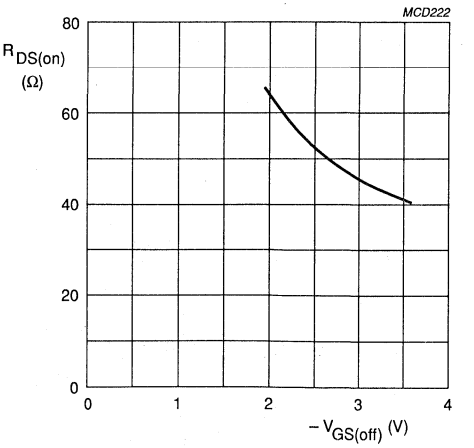
Fig.3 Common-source transfer admittance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_j = 25 °C.

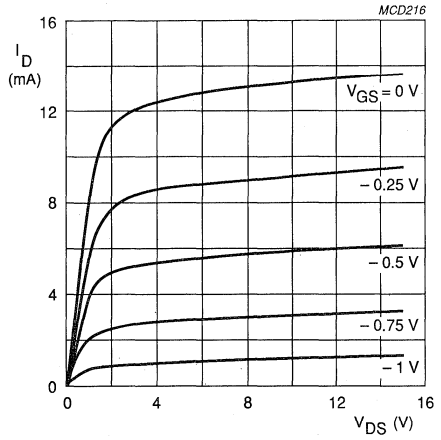
Fig.4 Common-source output conductance as a function of gate-source cut-off voltage.



PMBFJ308, 309 & 310.

V_{DS} = 0.1 V; V_{GS} = 0; T_j = 25 °C.

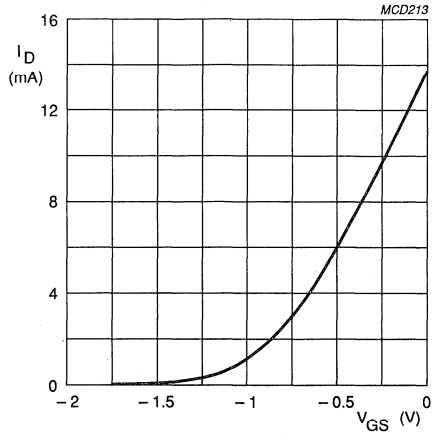
Fig.5 Drain-source on resistance as a function of gate-source cut-off voltage.



PMBFJ308.

T_j = 25 °C.

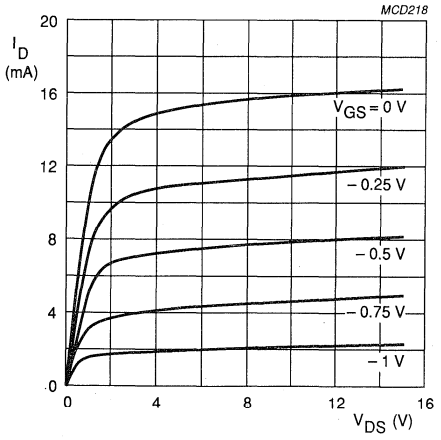
Fig.6 Output characteristics, typical values.



PMBFJ308.

V_{DS} = 10 V; T_j = 25 °C.

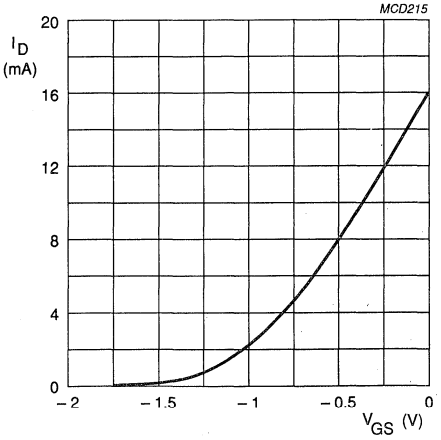
Fig.7 Input characteristics, typical values.



PMBFJ309.

T_j = 25 °C.

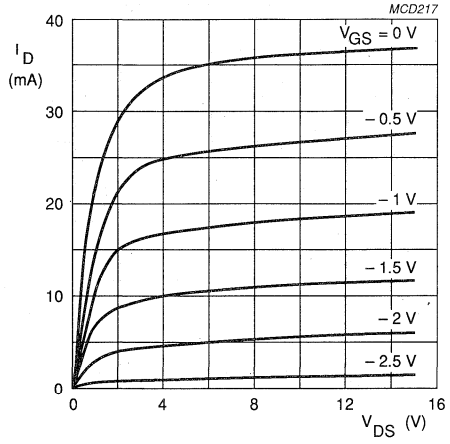
Fig.8 Output characteristics, typical values.



PMBFJ309.

V_{DS} = 10 V; T_j = 25 °C.

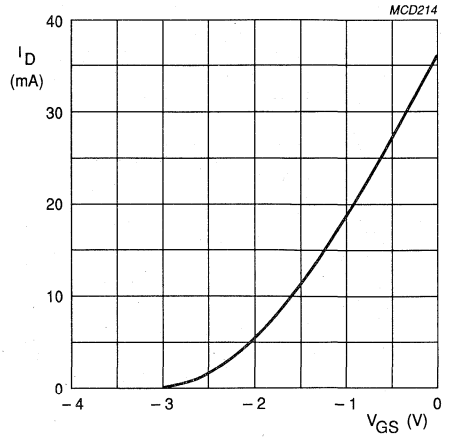
Fig.9 Input characteristics, typical values.



PMBFJ310.

T_j = 25 °C.

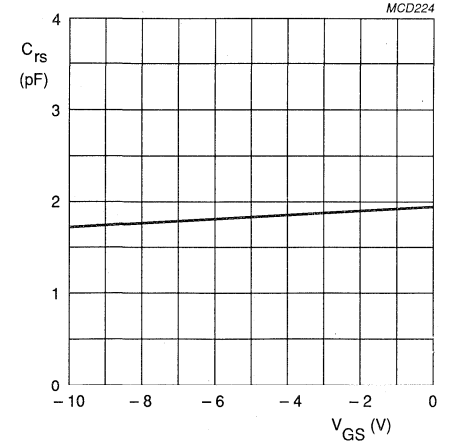
Fig.10 Output characteristics, typical values.



PMBFJ310.

V_{DS} = 10 V; T_j = 25 °C.

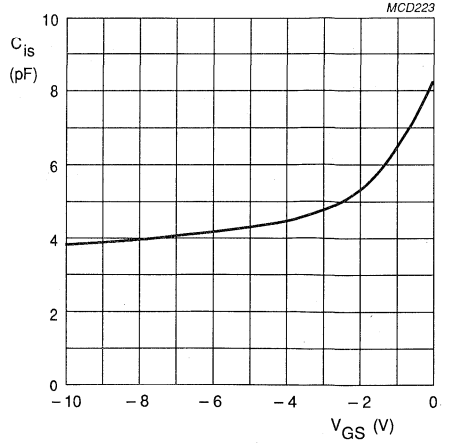
Fig.11 Input characteristics, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

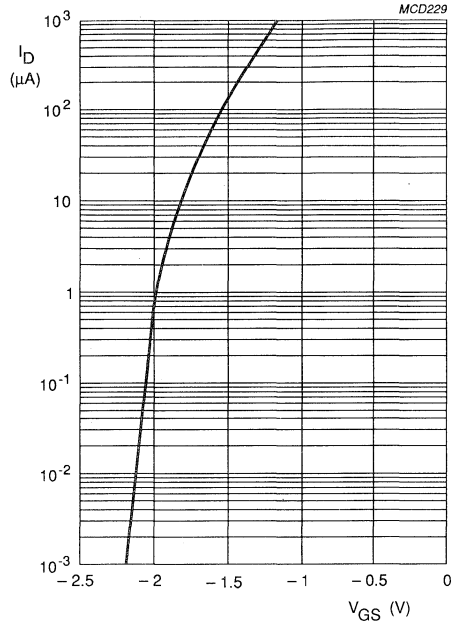
Fig.12 Feedback capacitance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; T_j = 25 °C.

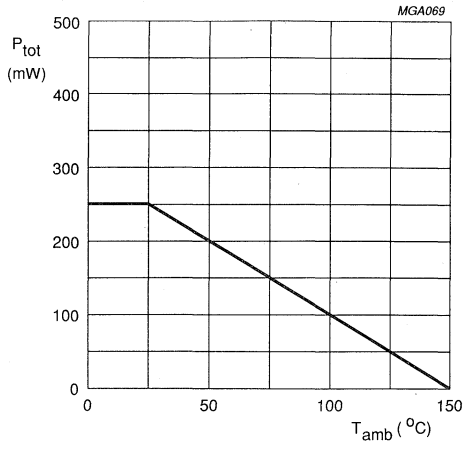
Fig.13 Input capacitance, typical values.



PMBFJ308, 309 & 310.

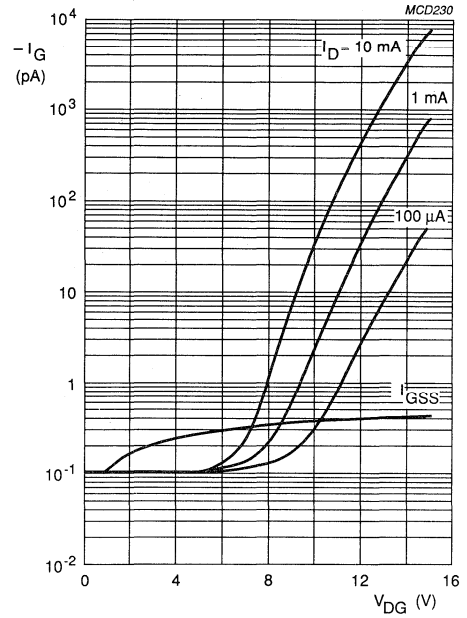
V_{DS} = 10 V; T_j = 25 °C.

Fig.14 Drain current as a function of gate-source voltage, typical values.



PMBFJ308, 309 & 310.

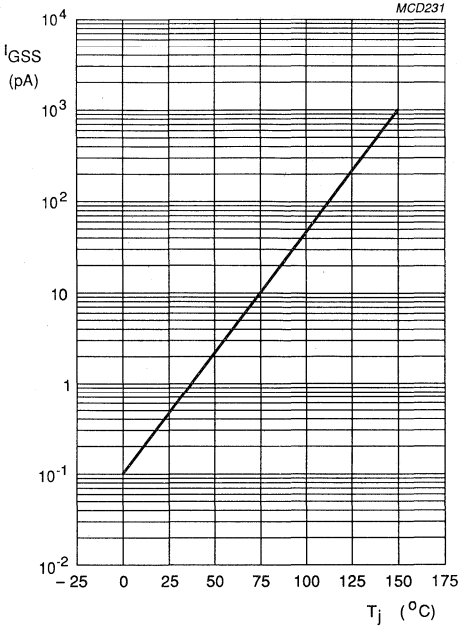
Fig.15 Power derating curve.



PMBFJ308, 309 & 310.

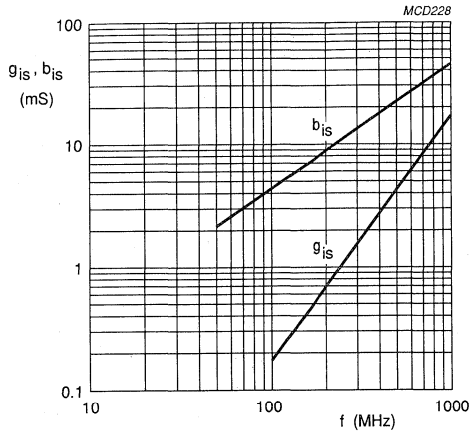
T_j = 25 °C.

Fig.16 Gate current as a function of drain-gate voltage, typical values.



PMBFJ308, 309 & 310.

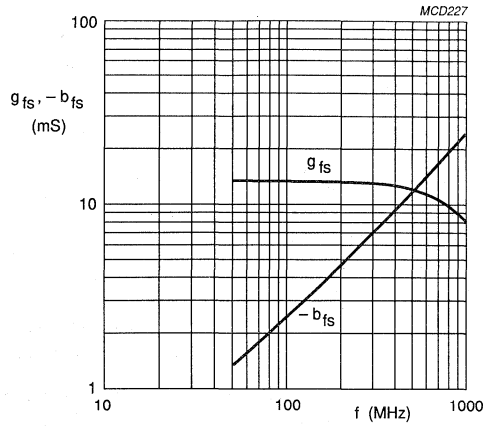
Fig.17 Gate current as a function of junction temperature, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

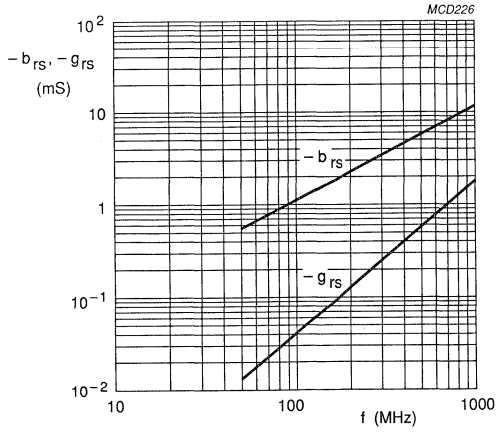
Fig.18 Input admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

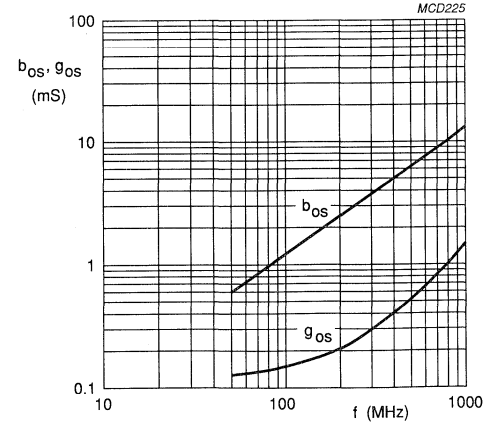
Fig.19 Forward admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.20 Reverse admittance, typical values.



PMBFJ308, 309 & 310.

V_{DS} = 10 V; I_D = 10 mA; T_{amb} = 25 °C.

Fig.21 Output admittance, typical values.

Philips Semiconductors

Date of Issue	May 23, 1990
Status	Product Specification
Application Specific Product	

80C31/80C51/87C51

CMOS single-chip, 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C31/80C51/87C51 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC51 is functionally compatible with the NMOS 8031/8051 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

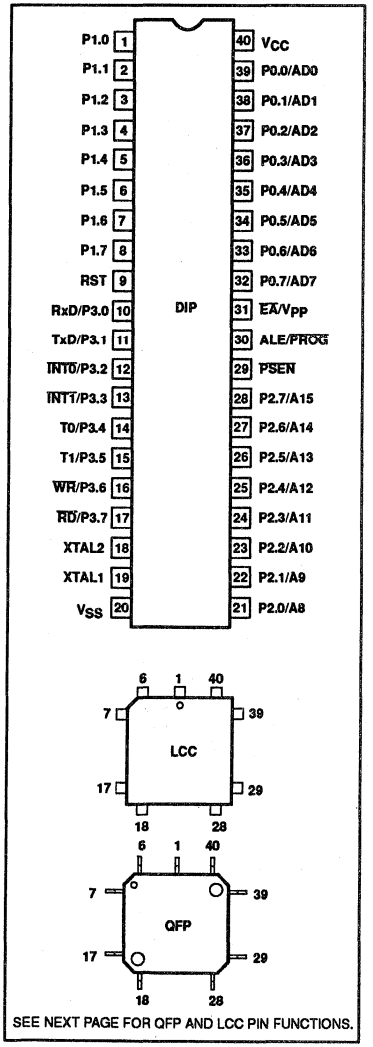
The 8XC51 contains a 4k x 8 ROM (80C51) EPROM (87C51), a 128 x 8 RAM, 32 I/O lines, two 16-bit counter/timers, a five-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the device has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

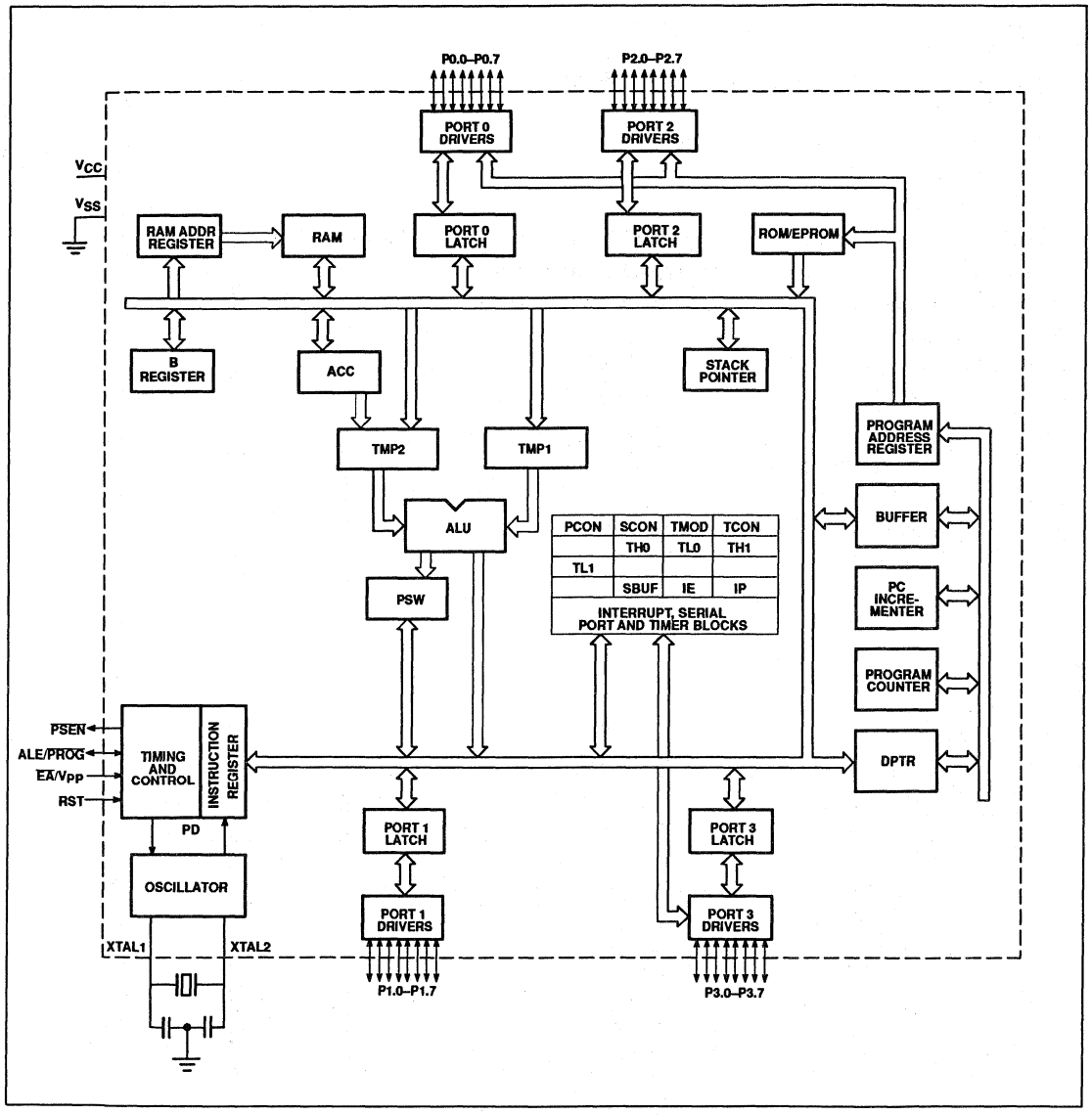
- 8031/8051 compatible
  - 4k x 8 ROM (80C51)
  - 4k x 8 EPROM (87C51)
  - ROMless (80C31)
  - 128 x 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Five speed ranges at V_{CC} = 5V
  - 12MHz
  - 16MHz
  - 20MHz
  - 24MHz
  - 30MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Low voltage 8-bit Microcontroller P80CL51

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL / mini-pack
- 4K x 8 ROM, expandable externally to 64K bytes
- 128 bytes RAM, expandable externally to 64K bytes
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Thirteen source, thirteen vector interrupt structure with two priority levels
- Full duplex serial port (UART)
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth up to 128 bytes
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at port 1
- Single supply voltage of 1.8 V to 6.0 V
- Frequency range of 32 kHz to 16 MHz *
- Very low current consumption
- Operating temperature range: –40 to +85 °C

* The currently available product is guaranteed upto 12MHz at 4.5 V. A device covering the rang upto 16MHz at 4.5 V will be available later in 1992.

GENERAL DESCRIPTION

The P80CL51 is manufactured in an advanced CMOS technology. The instruction set of the P80CL51 is based on that of the 8051. The P80CL51 is a general purpose microcontroller especially suited for battery-powered application. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The P80CL51 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P80CL51 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
P80CL51HFP	40	DIL	plastic	SOT129
P80CL51HFT	40	mini-pack	plastic	SOT158A

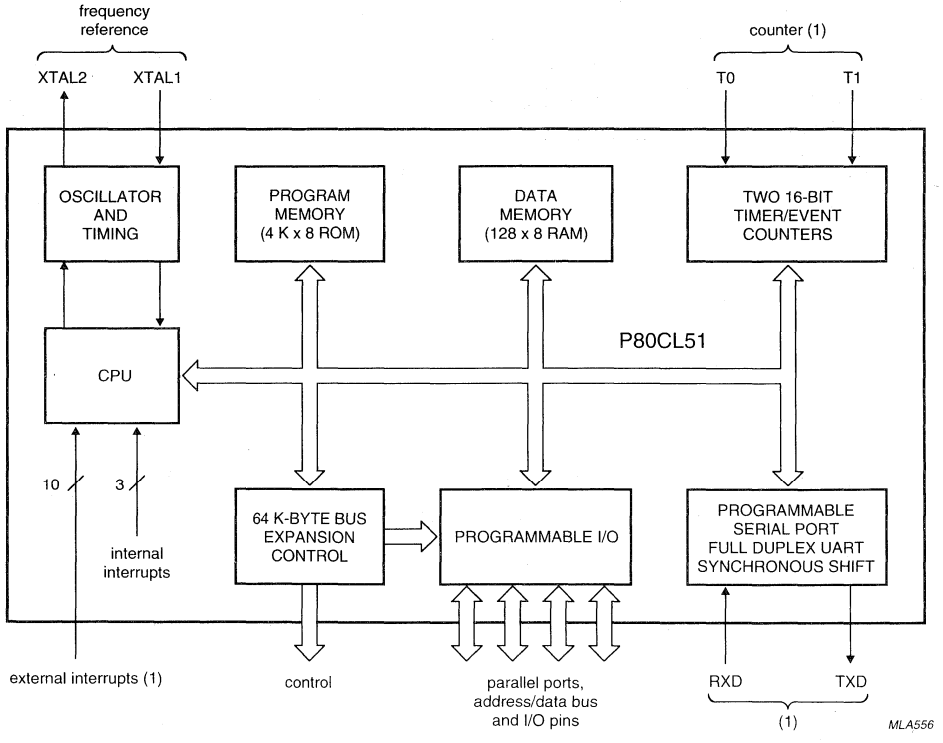


Fig.1 Block diagram.

Philips Semiconductors

Document No.	
ECN No.	
Date of Issue	January 1990
Status	Preliminary Specification
Application Specific Product	

80C32/80C52/87C52
CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C32/80C52/87C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 8XC52 is functionally compatible with the NMOS SCN-8032/8052 microcontrollers. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

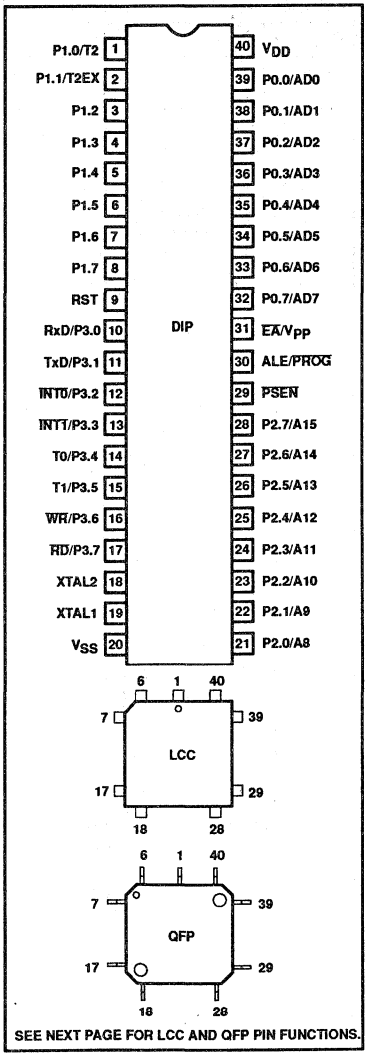
The 8XC52 contains an 8K x 8 ROM (80C52) EPROM (87C52), a 256 x 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 8XC52 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

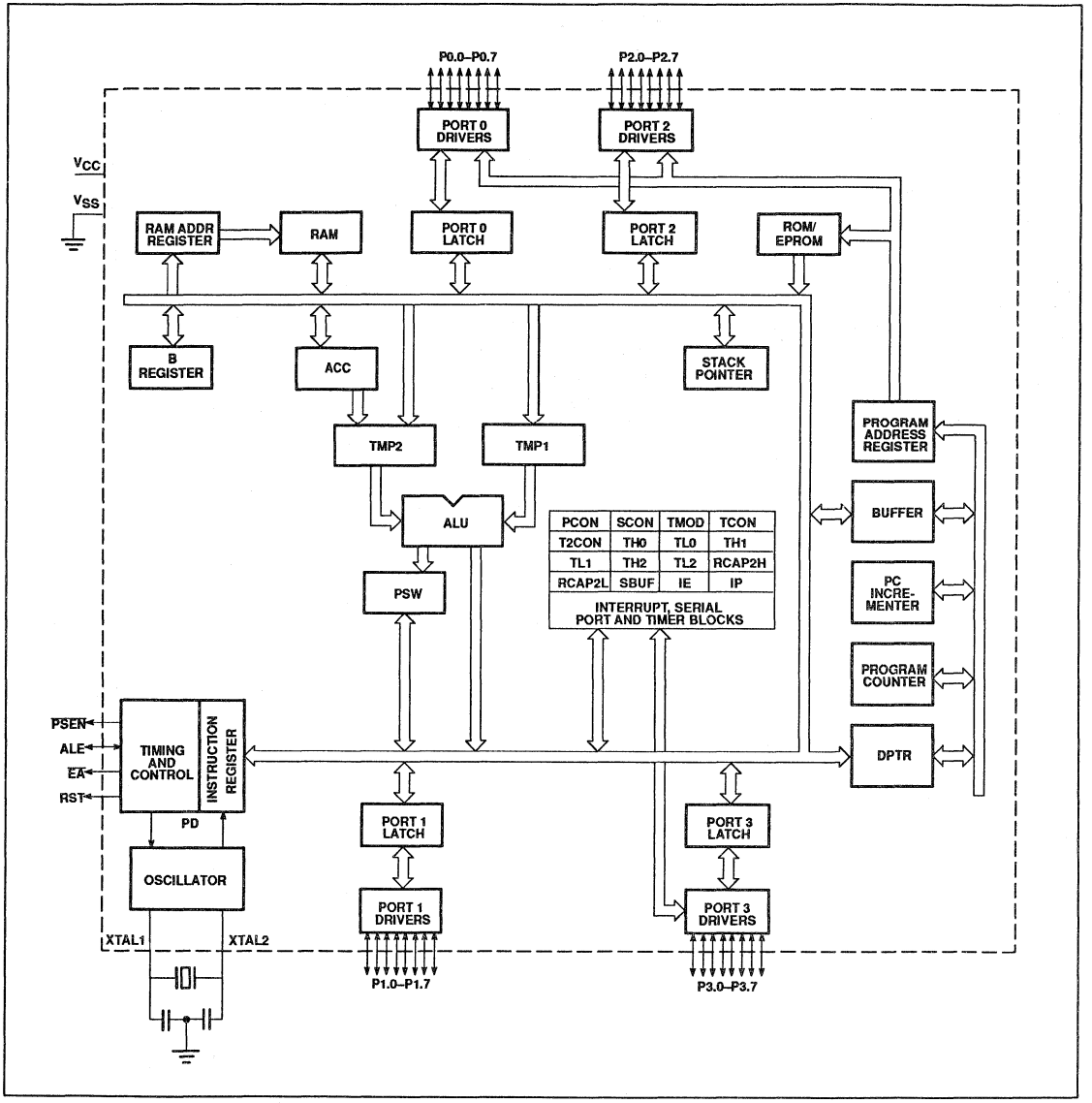
- 80C51 based architecture
- 8032/8052 compatible
  - 8k x 8 ROM (80C52)
  - 8k x 8 EPROM (87C52)
  - ROMless (80C32)
  - 256 x 8 RAM
  - Three 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Two speed ranges:
  - 3.5 to 16MHz
  - 3.5 to 20MHz
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC AND QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Semiconductors

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

80CL410/83CL410

Low voltage/low power single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 80CL410/83CL410 (hereafter generically referred to as 8XCL410) is manufactured in an advanced CMOS process that allows the part to operate at supply voltages down to 1.5V and oscillator frequencies down to DC. The 8XCL410 has the same instruction set as the 80C51.

The 8XCL410 features a 4k byte ROM (83CL410), 128 bytes RAM (both ROM and RAM are externally expandable to 64k bytes), four 8-bit ports, two 16-bit timer/counters, an I²C serial interface, a thirteen source, two priority level nested interrupt structure, and on-chip oscillator circuitry suitable for quartz crystal, ceramic resonator, RC, or LC.

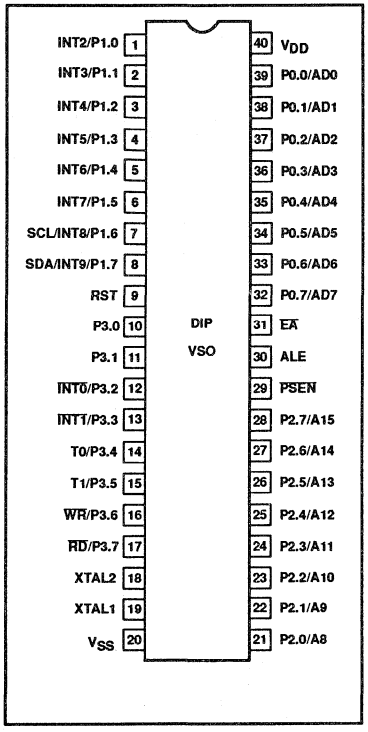
The 8XCL410 has two reduced power modes that are the same as those on the standard 80C51. The special reduced power feature of this part is that it can be stopped and then restarted. Running from an external clock source, the clock can be stopped and after a period of time restarted. The 8XCL410 will resume operation from where it was when the code stopped with no loss of internal state, RAM contents, or Special Function Register contents. If the internal oscillator is used the part cannot be stopped and started, but the power-down mode, which can be terminated via an interrupt, can be used to achieve similar power savings and then restart without loss of on-chip RAM and Special Function Register values.

For emulation purposes, the P85CL000 (Piggyback version) with 256 bytes of RAM is recommended.

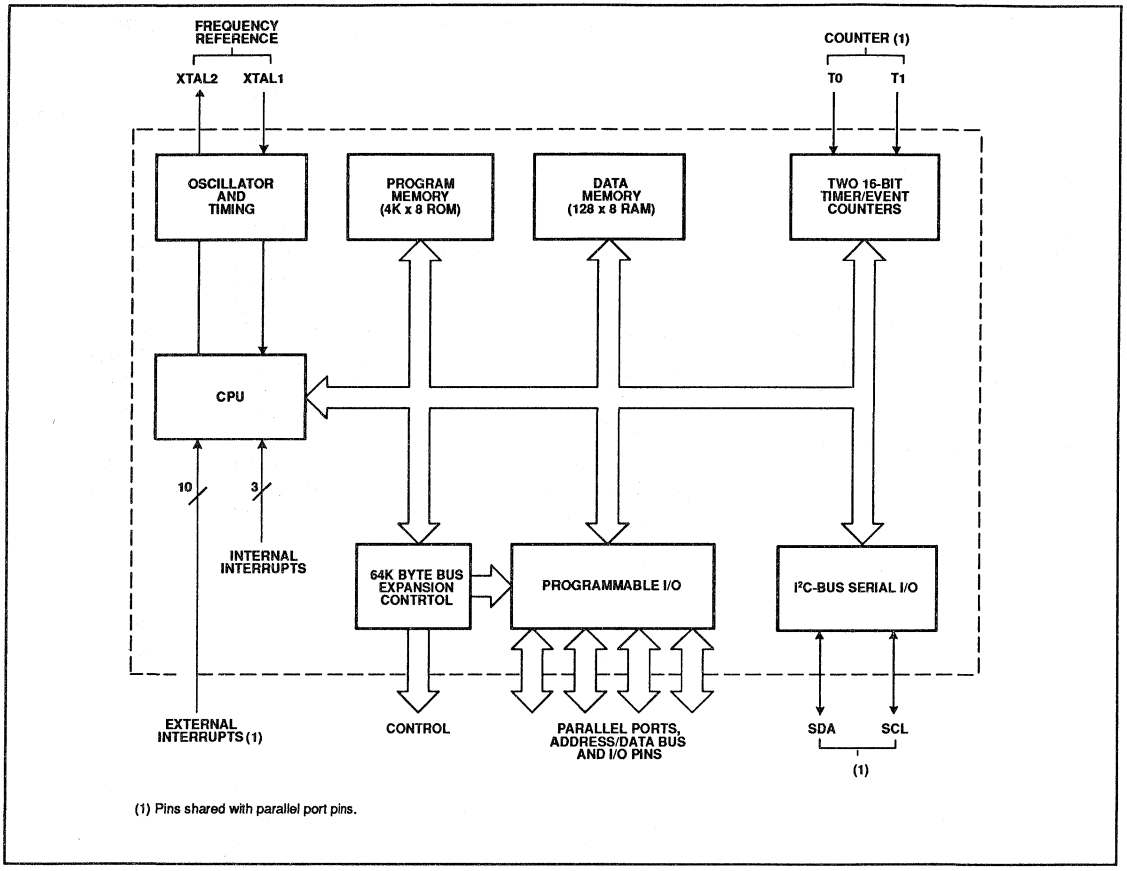
FEATURES

- Supply voltage from 1.5 to 5.5V
- Operating frequency from 32kHz to 20MHz
- 80C51 based architecture
  - 4k x 8 ROM (64k external)
  - 128 x 8 RAM (64k external)
  - Four 8-bit I/O ports
  - Two 16-bit timer/counters
  - A thirteen source, two level, nested priority interrupt structure
  - 10 external interrupts
- Fully static 80C51 CPU
- I²C Serial Interface
- Two power control modes
  - Idle mode
  - Power-down mode – can be terminated by reset or external interrupt
- Wake-up via external interrupts at port 1
- On-chip oscillator (quartz crystal, ceramic resonator, RC, LC)
- Very low power consumption
- Operating temperature range: –40 to +85°C

PIN CONFIGURATION



BLOCK DIAGRAM



(1) Pins shared with parallel port pins.

Philips Semiconductors

Date of Issue	February 1, 1990
Status	Product Specification
Application Specific Product	

80C451/83C451/87C451

CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 8XC451 is an I/O expanded single-chip microcontroller fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes latch-up sensitivity.

The 8XC451 is a functional extension of the 87C51 microcontroller with three additional I/O ports and four I/O control lines. The LCC version has a total of 68 pins. Four control lines associated with port 6 facilitate high-speed asynchronous I/O functions.

The 8XC451 includes a 4k X 8 ROM (83C451) EPROM (87C451), a 128 X 8 RAM, 56 (LCC) or 52 (DIP) I/O lines, two 16-bit timer/counters, a five source, two priority level, nested interrupt structure, a serial I/O port for either a full duplex UART, I/O expansion, or muti-processor communications, and on-chip oscillator and clock circuits. The 80C451 includes all of the 83C451 features except the on-board 4k X 8 ROM.

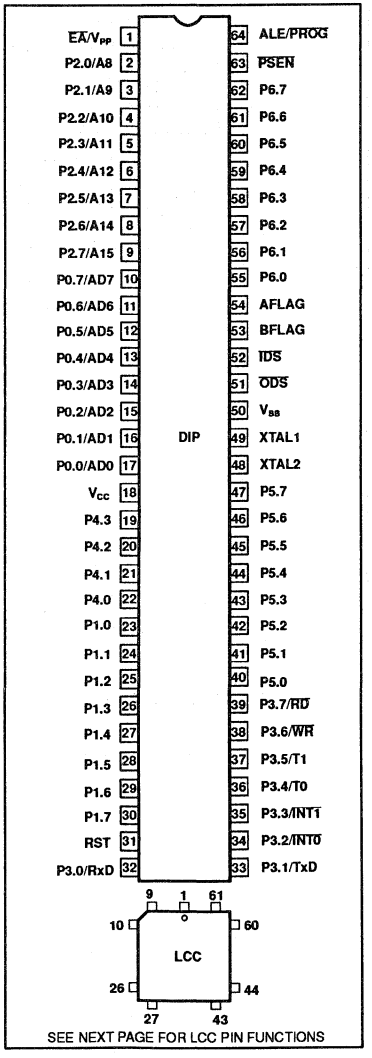
The 87C451 has 4k of EPROM on-chip as program memory and is otherwise identical to the 83C451.

The 8XC451 has two software selectable modes of reduced activity for further power reduction; idle mode and power-down mode. Idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. Power-down mode freezes the oscillator, causing all other chip functions to be inoperative while maintaining the RAM contents.

FEATURES

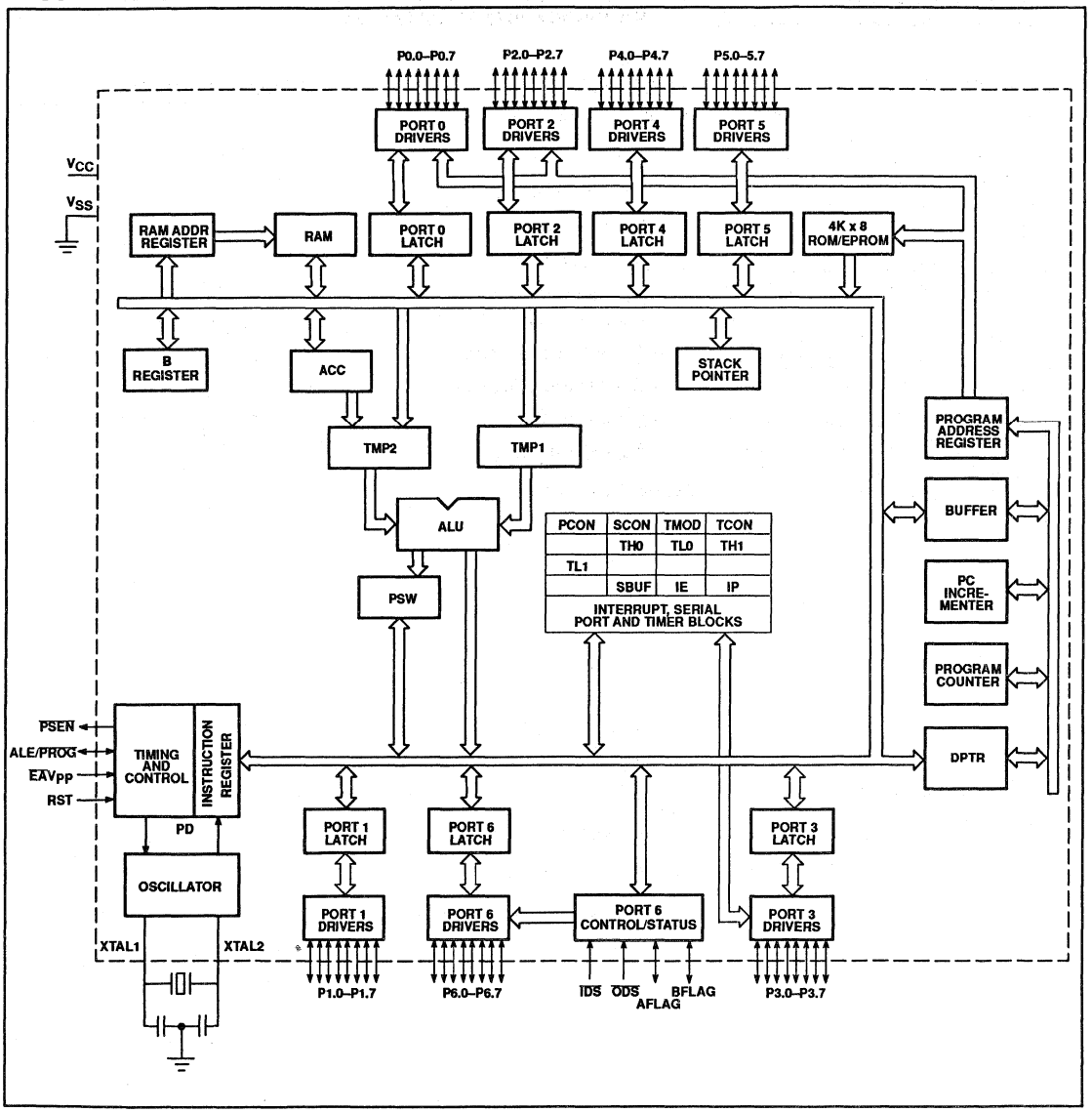
- 80C51 based architecture
- 68-pin LCC and 64-pin DIP packages:
  - Seven 8-bit I/O ports (LCC version)
  - Six 8-bit ports and one 4-bit port (DIP version)
- Port 6 features:
  - 8 data pins
  - 4 control pins
  - Direct MPU bus interface
  - Parallel printer interface
- On the microcontroller:
  - 4k X 8 ROM (83C451)
    4k X 8 EPROM (87C451)
    ROMless version (80C451)
  - 128 X 8 RAM
  - Two 16-bit counter/timers
  - Two external interrupts
- External memory addressing capability
  - 64k ROM and 64k RAM
- Low power consumption:
  - Normal operation: less than 24mA at 5V, 12MHz
  - Idle mode
  - Power-down mode

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC PIN FUNCTIONS

BLOCK DIAGRAM



Philips Semiconductors

Document No.	
ECN No.	
Date of Issue	February 1990
Status	Preliminary Specification
Application Specific Product	

80C528/83C528/87C528

CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 8XC528 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroler family. The 8XC528 has the same instruction set as the 80C51.

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems, especially in those systems which need large ROM and RAM capacity on-chip.

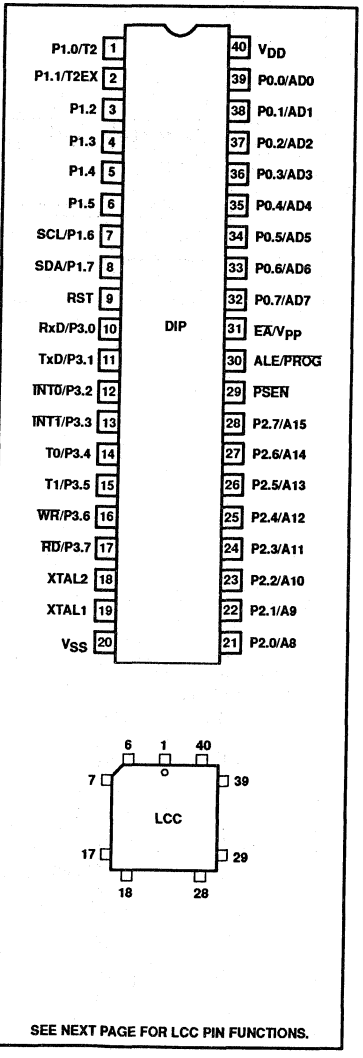
The 8XC528 contains a 32k x 8 ROM (83C528)/EPROM (87C528), a 512 x 8 RAM, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a 16-bit timer (identical to the timer 2 of the 80C52), a watchdog timer with a separate oscillator, a multisource, two-priority-level, nested interrupt structure, two serial interfaces (UART and I²C-bus), and on-chip oscillator and timing circuits.

In addition, the 8XC528 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

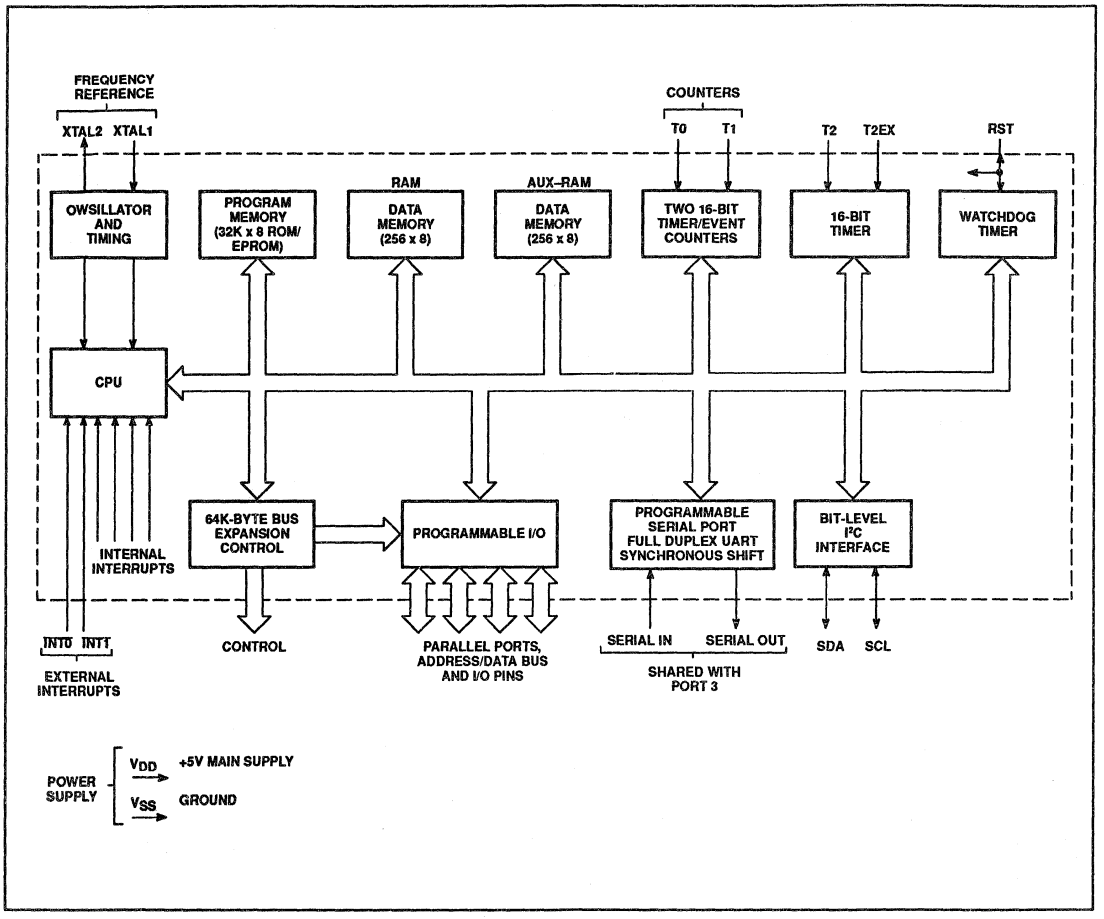
- 80C51 instruction set
  - 32k x 8 ROM (83C528)
  - 32k x 8 EPROM (87C528)
  - ROMless (80C528)
  - 512 x 8 RAM
  - Memory addressing capability – 64k ROM and 64k RAM
  - Three 16-bit counter/timers
  - On-chip watchdog timer
  - Full duplex UART
  - I²C serial interface
- Power control modes:
  - Idle mode
  - Power-down mode
  - Warm start from power-down
- CMOS and TTL compatible
- Three speed ranges at V_{DD} = 5V ±10%
  - 3.5 to 12MHz
  - 3.5 to 16MHz
  - 0.5 to 12MHz
- Extended temperature ranges
- OTP package available
- ROM/EPROM code protection

PIN CONFIGURATION



SEE NEXT PAGE FOR LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Document No.	
ECN No.	
Date of Issue	August 1990
Status	Preliminary Specification
Application Specific Product	

80C550/83C550/87C550

CMOS single-chip 8-bit microcontroller with A/D and watchdog timer

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 8XC550 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. This Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity. The CMOS 8XC550 has the same instruction set as the 80C51.

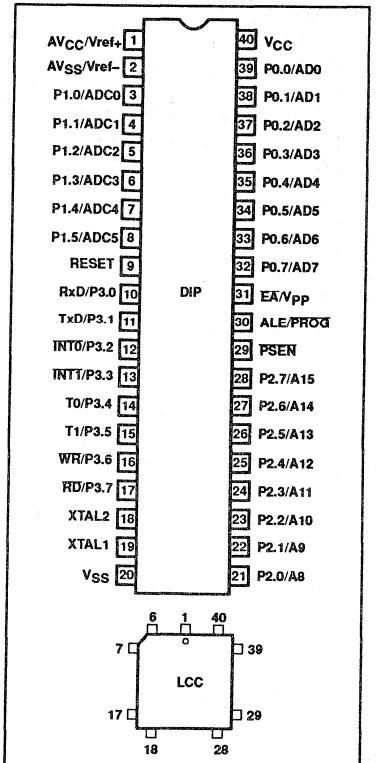
The 8XC550 contains a 4k x 8 EPROM (87C550)/ROM (83C550)/ROMless (80C550 has no program memory on-chip), a 128 x 8 RAM, 8 channels of 8-bit A/D, four 8-bit ports (port 1 is input only), a watchdog timer, two 16-bit counter/timers, a seven-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and an on-chip oscillator and clock circuits.

In addition, the 8XC550 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k x 8 EPROM (87C550)/ ROM (83C550)
  - 128 x 8 RAM
  - 8 channels of 8-bit A/D
  - Two 16-bit counter/timers
  - Watchdog timer
  - Full duplex serial channel
  - Boolean processor
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- Three speed ranges at V_{CC} = 5V ±10%
  - 3.5 to 12MHz
  - 3.5 to 16MHz
- Four package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION

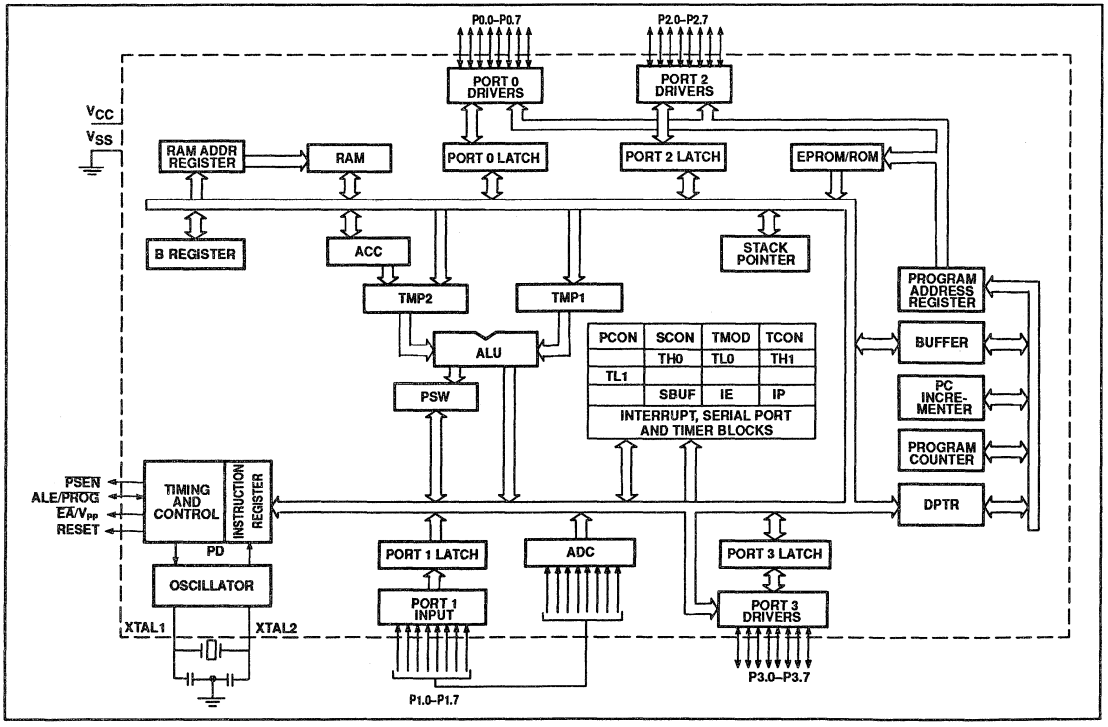


Pin	Function	Pin	Function	Pin	Function
1	AV_{CC}	16	P3.2/INT0	31	P2.6/A14
2	Vref+	17	P3.3/INT1	32	P2.7/A15
3	Vref–	18	P3.4/T0	33	PSEN
4	AV_{SS}	19	P3.5/T1	34	ALE/PROG
5	P1.0/ADC0	20	P3.6/WR	35	EA/V_{PP}
6	P1.1/ADC1	21	P3.7/RD	36	P0.7/AD7
7	P1.2/ADC2	22	XTAL2	37	P0.6/AD6
8	P1.3/ADC3	23	XTAL1	38	P0.5/AD5
9	P1.4/ADC4	24	V_{SS}	39	P0.4/AD4
10	P1.5/ADC5	25	P2.0/A8	40	P0.3/AD3
11	P1.6/ADC6	26	P2.1/A9	41	P0.2/AD2
12	P1.7/ADC7	27	P2.2/A10	42	P0.1/AD1
13	RESET	28	P2.3/A11	43	P0.0/AD0
14	P3.0/RxD	29	P2.4/A12	44	V_{CC}
15	P3.1/TxD	30	P2.5/A13		

PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE AND PACKAGE	FREQUENCY
P80C550BBF	P83C550BBF	P87C550BBF	0 to +70°C, ceramic DIP	3.5 to 12MHz
P80C550EBF	P83C550EBF	P87C550EBF	0 to +70°C, ceramic DIP	3.5 to 16MHz
P80C550BBK	P83C550BBK	P87C550BBK	0 to +70°C, ceramic LCC	3.5 to 12MHz
P80C550EBK	P83C550EBK	P87C550EBK	0 to +70°C, ceramic LCC	0.5 to 16MHz
P80C550BBP	P83C550BBP	P87C550BBP	0 to +70°C, plastic DIP	3.5 to 12MHz
P80C550EBP	P83C550EBP	P87C550EBP	0 to +70°C, plastic DIP	3.5 to 16MHz
P80C550BBA	P83C550BBA	P87C550BBA	0 to +70°C, plastic LCC	3.5 to 12MHz
P80C550EBA	P83C550EBA	P87C550EBA	0 to +70°C, plastic LCC	3.5 to 16MHz
P80C550BFP	P83C550BFP	P87C550BFP	–40 to +85°C, plastic DIP	3.5 to 12MHz
P80C550EFP	P83C550EFP	P87C550EFP	–40 to +85°C, plastic DIP	3.5 to 16MHz
P80C550BFA	P83C550BFA	P87C550BFA	–40 to +85°C, plastic LCC	3.5 to 12MHz
P80C550EFA	P83C550EFA	P87C550EFA	–40 to +85°C, plastic LCC	3.5 to 16MHz
P80C550BFF	P83C550BFF	P87C550BFF	–40 to +85°C, ceramic DIP	3.5 to 12MHz
P80C550EFF	P83C550EFF	P87C550EFF	–40 to +85°C, ceramic LCC	3.5 to 12MHz
P80C550BFK	P83C550BFK	P87C550BFK	–40 to +85°C, ceramic LCC	3.5 to 16MHz
P80C550EFK	P83C550EFK	P87C550EFK	–40 to +85°C, ceramic DIP	3.5 to 16MHz

BLOCK DIAGRAM



Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C552/83C552/87C552

Single-chip 8-bit microcontroller with 10-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C552/83C552/87C552 (hereafter generically referred to as 8XC552) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 has the same instruction set as the 80C51. Three versions of the derivative exist:

- 83C552 — 8k bytes mask programmable ROM
- 80C552 — ROMless version of the 83C552
- 87C552 — 8k bytes EPROM

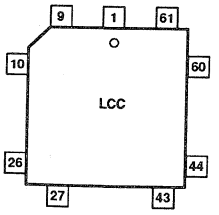
The 8XC552 contains a non-volatile 8k x 8 read-only program memory (83C552) EPROM (87C552), a volatile 256 x 8 read/write data memory, five 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC552 can be expanded using standard TTL compatible memories and logic.

In addition, the 8XC552 has two software selectable modes of power reduction—idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial ports, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

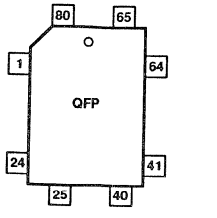
FEATURES

- 80C51 central processing unit
- 8k x 8 ROM expandable externally to 64k bytes
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Two standard 16-bit timer/counters
- 256 x 8 RAM, expandable externally to 64k bytes
- Capable of producing 8 synchronized, timed outputs
- A 10-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Two speed ranges:
  - 12MHz
  - 16MHz
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION

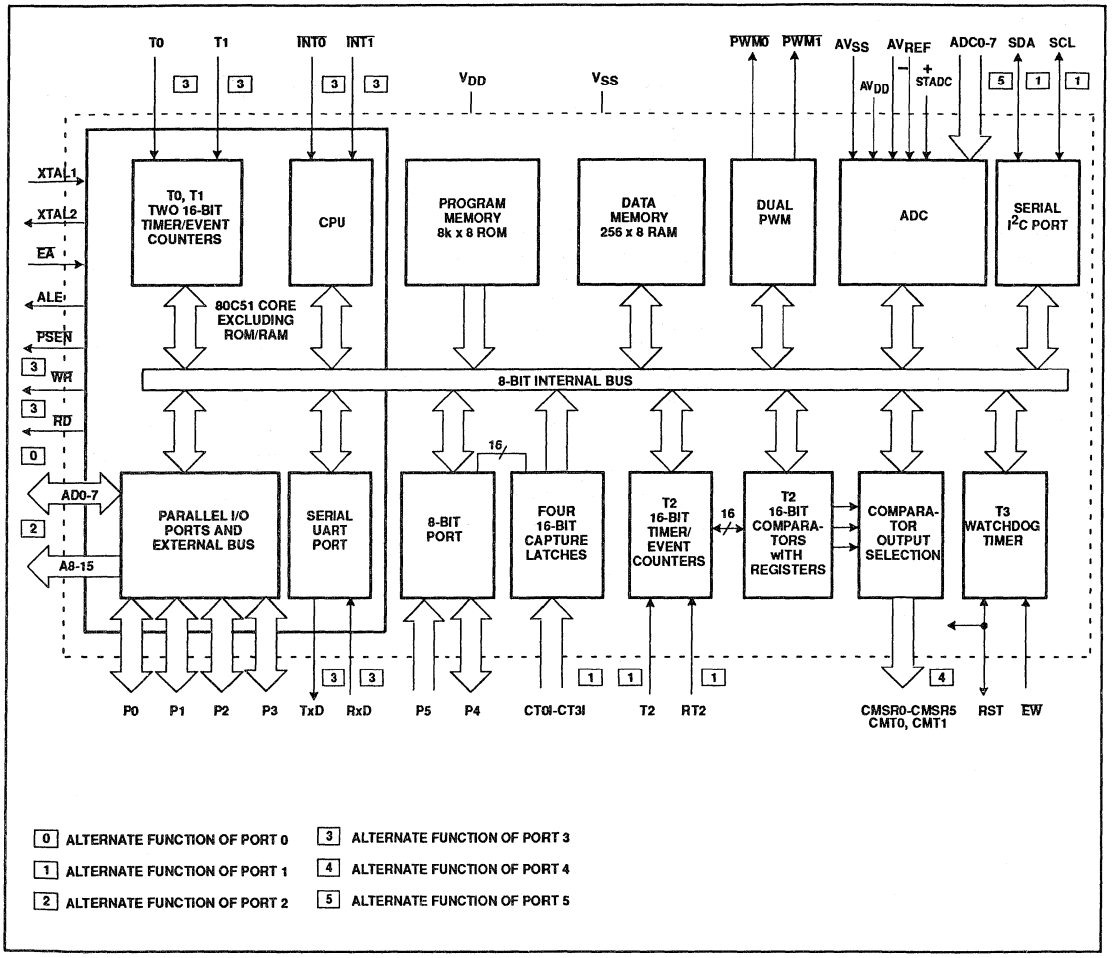


Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	45	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE/$\overline{PROG}$
15	RST	49	$\overline{EA}/V_{PP}$
16	P1.0/CT0I	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref−
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



SEE PAGE 347 FOR QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Semiconductors

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C562/83C562

Single-chip 8-bit microcontroller with 8-bit A/D, capture/compare timer, high-speed outputs, PWM

DESCRIPTION

The 80C562/83C562 (hereafter generically referred to as 8XC562) Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C562/83C562 has the same instruction set as the 80C51.

The 8XC562 contains a non-volatile 256 x 8 read-only program memory, a volatile 256 X 8 read/write data memory (83C562) (the 80C562 is ROMless), a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, an 8-input ADC, two pulse width modulated outputs, standard 80C51 UART, a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 83C562 can be expanded using standard TTL compatible memories and logic.

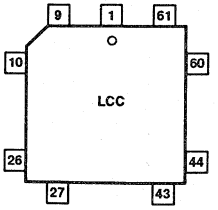
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

For emulation purposes, the 87C552 is recommended.

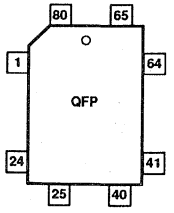
FEATURES

- 80C51 instruction set
- 8k x 8 ROM expandable externally to 64k bytes
- 256 x 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- Capable of producing 8 synchronized, timed outputs
- A 8-bit ADC with 8 multiplexed analog inputs
- Two 8-bit resolution, pulse width modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Three temperature ranges
  - 0 to +70°C
  - –40 to +85°C
  - –40 to +125°C

PIN CONFIGURATION

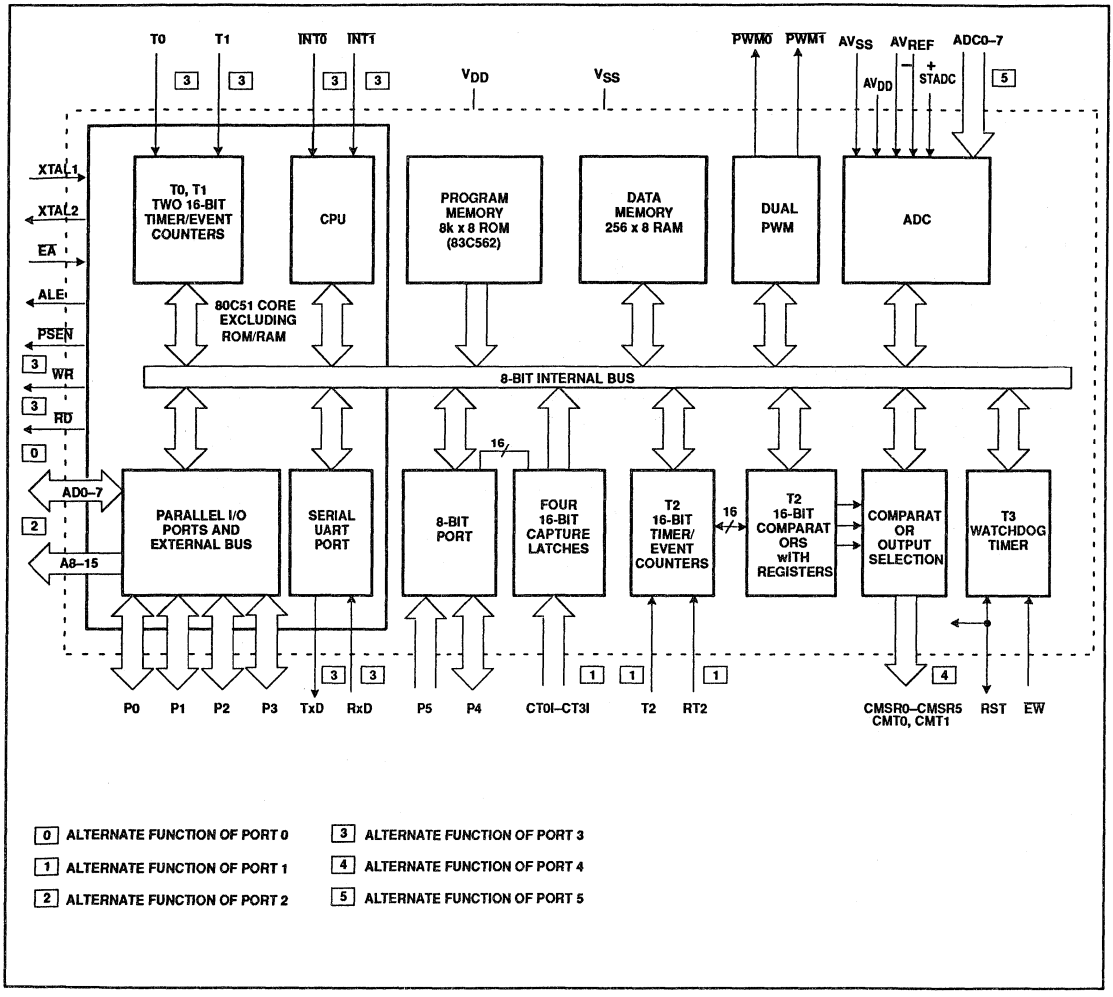


Pin	Function	Pin	Function
1	P5.0/ADC0	35	XTAL1
2	V_{DD}	36	V_{SS}
3	STADC	37	V_{SS}
4	$\overline{PWM0}$	38	NC
5	$\overline{PWM1}$	39	P2.0/A08
6	$\overline{EW}$	40	P2.1/A09
7	P4.0/CMSR0	41	P2.2/A10
8	P4.1/CMRS1	42	P2.3/A11
9	P4.2CMSR2	43	P2.4/A12
10	P4.3/CMSR3	44	P2.5/A13
11	P4.4/CMSR4	45	P2.6/A14
12	P4.5/CMSR5	46	P2.7/A15
13	P4.6/CMT0	47	$\overline{PSEN}$
14	P4.7/CMT1	48	ALE
15	RST	49	$\overline{EA}$
16	P1.0/CT01	50	P0.7/AD7
17	P1.1/CT1I	51	P0.6/AD6
18	P1.2/CT2I	52	P0.5/AD5
19	P1.3/CT3I	53	P0.4/AD4
20	P1.4/T2	54	P0.3/AD3
21	P1.5/RT2	55	P0.2/AD2
22	P1.6/SCL	56	P0.1/AD1
23	P1.7/SDA	57	P0.0/AD0
24	P3.0/RxD	58	AVref–
25	P3.1TxD	59	AVref+
26	P3.2/$\overline{INT0}$	60	AV_{SS}
27	P3.3/$\overline{INT1}$	61	AV_{DD}
28	P3.4/T0	62	P5.7/ADC7
29	P3.5/T1	63	P5.6/ADC6
30	P3.6/$\overline{WR}$	64	P5.5/ADC5
31	P3.7/$\overline{RD}$	65	P5.4/ADC4
32	NC	66	P5.3/ADC3
33	NC	67	P5.2/ADC2
34	XTAL2	68	P5.1/ADC1



SEE NEXT PAGE FOR QFP PIN FUNCTIONS.

BLOCK DIAGRAM



Single-chip 8-bit microcontroller with CAN controller

80C592/83C592/87C592

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 80C592/83C592/87C592 (hereafter referred to generically as the 8XC592) is a stand-alone high-performance microcontroller designed for use in automotive and general industrial applications. In addition to the 80C51 standard features, this device provides a number of dedicated hardware functions for these applications. Three versions of this derivative will be offered:

- 83C592 (ROM version)
- 80C592 (ROMless version)
- 87C592 (EPROM/OTP version)

It combines the functions of the existing 8XC552 and the Philips CAN-Controller PCA82C200 (CAN: Controller Area Network) with the following enhanced features:

- 16K byte Program Memory
- 2 × 256 byte Data Memory
- DMA between CAN Transmit/Receive buffer and internal RAM

The temperature range includes –40°C to +85°C as well as automotive temperature range –40°C to +125°C for the ROM and ROMless version with a maximum clock frequency of 16MHz. The 87C592 has a temperature range of –40°C to +85°C.

The main differences to the 8XC552 microcontroller are:

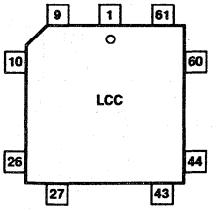
- a Can-controller substitutes the I^2C-serial interface
- 16K byte programmable ROM resp. EPROM instead of 8K byte
- additional 256 byte RAM.

The 8XC592 contains a 16k × 8 EPROM (87C592), ROM (83C592) program memory, a volatile 512 × 8 read/write data memory, a Controller Area Network (CAN) controller, six 8-bit I/O ports, one 8-bit input port, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a 15-source, two-priority-level, nested interrupt structure, a 10-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and CAN), a "watchdog" timer and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC592 memory can be expanded externally using standard TTL compatible memories and logic.

FEATURES

- 80C51 core architecture
- 16k × 8 EPROM (87C592)
- 16k × 8 ROM (83C592)
- ROMless (80C592)
- 512 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with eight multiplexed analog inputs
- Two 8-bit resolution, pulse width modulation outputs
- 15 interrupt sources with 2 priority levels
- Five 8-bit I/O ports plus one 8-bit input port shared with analog inputs
- CAN controller with DMA transfer between internal data RAM and CAN registers
- 1 Mbit/s CAN-Controller with bus failure management facility
- $V_{DD}/2$ reference voltage
- Full-duplex UART compatible with the standard 80C51
- On-chip watchdog timer
- Extended temperature ranges (–40 to +125°C)
- OTP package available

PIN CONFIGURATION

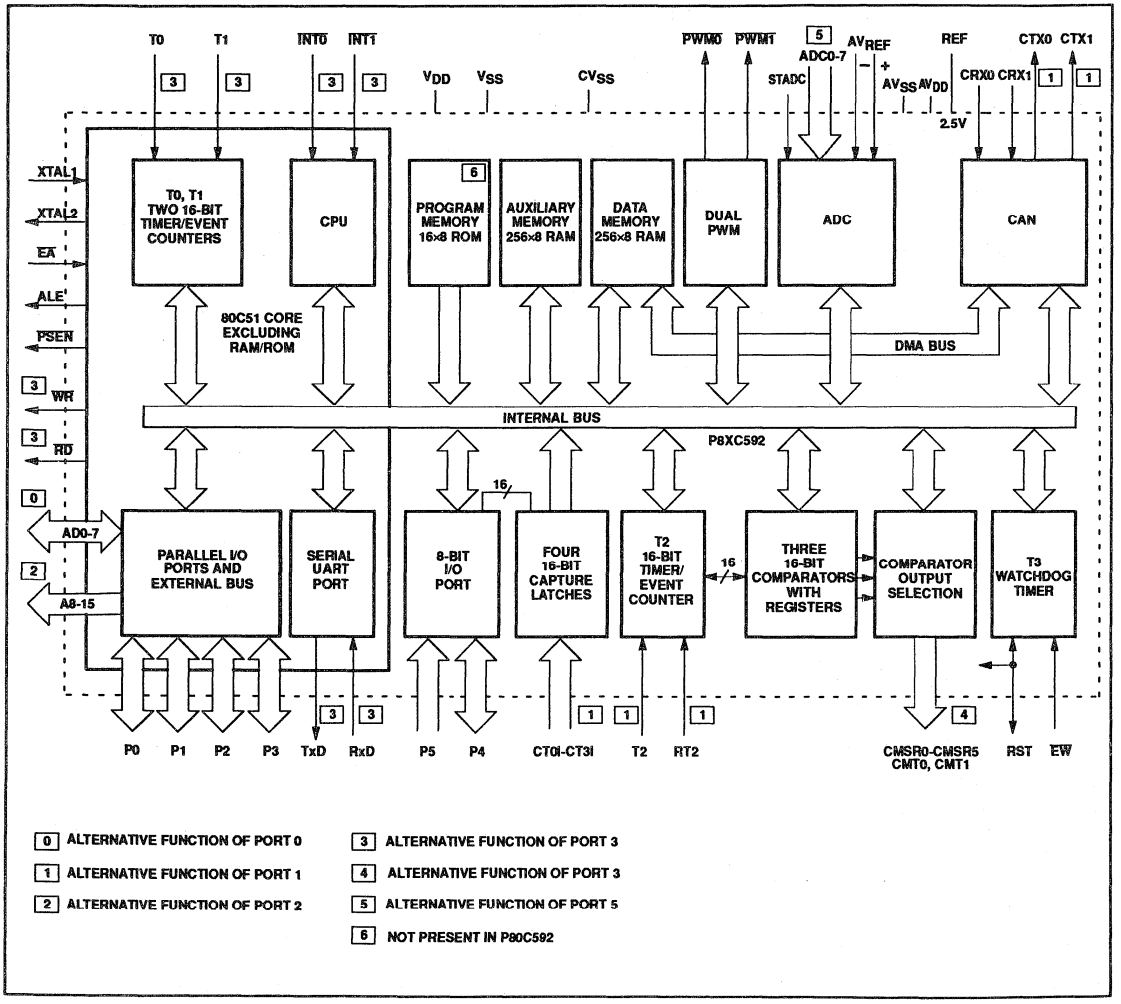


Pin	Function	Pin	Function
1	P5.0/ADC0	35	V_{SS}
2	V_{DD}	36	P2.0/A08
3	STADC	37	P2.1/A09
4	$\overline{PWM0}$	38	P2.2/A10
5	$\overline{PWM1}$	39	P2.3/A11
6	$\overline{EW}$	40	P2.4/A12
7	P4.0/CMSR0	41	P2.5/A13
8	P4.1/CMRS1	42	P2.6/A14
9	P4.2CMSR2	43	P2.7/A15
10	P4.3/CMSR3	44	$\overline{PSEN}$
11	P4.4/CMSR4	45	ALE/$\overline{PROG}$
12	P4.5/CMSR5	46	$\overline{EA}/V_{PP}$
13	P4.6/CMT0	47	P0.7/AD7
14	P4.7/CMT1	48	P0.6/AD6
15	RST	49	P0.5/AD5
16	P1.0/CT0I/INT2	50	P0.4/AD4
17	P1.1/CT1I/INT3	51	P0.3/AD3
18	P1.2/CT2I/INT4	52	P0.2/AD2
19	P1.3/CT3I/INT5	53	P0.1/AD1
20	P1.4/T2	54	P0.0/AD0
21	P1.5/RT2	55	REF
22	CV_{SS}	56	CRX1
23	P1.6/CTX0	57	CRX0
24	P1.7/CTX1	58	AVref–
25	P3.0/RxD	59	AVref+
26	P3.1TxD	60	AV_{SS}
27	P3.2/$\overline{INT0}$	61	AV_{DD}
28	P3.3/$\overline{INT1}$	62	P5.7/ADC7
29	P3.4/T0	63	P5.6/ADC6
30	P3.5/T1	64	P5.5/ADC5
31	P3.6/$\overline{WR}$	65	P5.4/ADC4
32	P3.7/$\overline{RD}$	66	P5.3/ADC3
33	XTAL2	67	P5.2/ADC2
34	XTAL1	68	P5.1/ADC1

PART NUMBER SELECTION

ROMless	ROM	EPROM	TEMPERATURE °C AND PACKAGE	FREQUENCY
P80C592FFA	P83C592FFA	–	–40° to +85°C, PLCC 68	1.2 to 16MHz
P80C592FHA	P83C592FHA	–	–40° to +125°C, PLCC 68	1.2 to 16MHz
–	–	P87C592EFL	–40° to +85°C, ceramic window LCC	3.5 to 16MHz
–	–	P87C592EFA	–40° to +85°C, plastic LCC	3.5 to 16MHz

BLOCK DIAGRAM



Philips Semiconductors

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

80C652/83C652/87C652

CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 80C652/83C652/87C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652/87C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 – 8k bytes mask programmable ROM

80C652 – ROMless version

87C652 – EPROM version

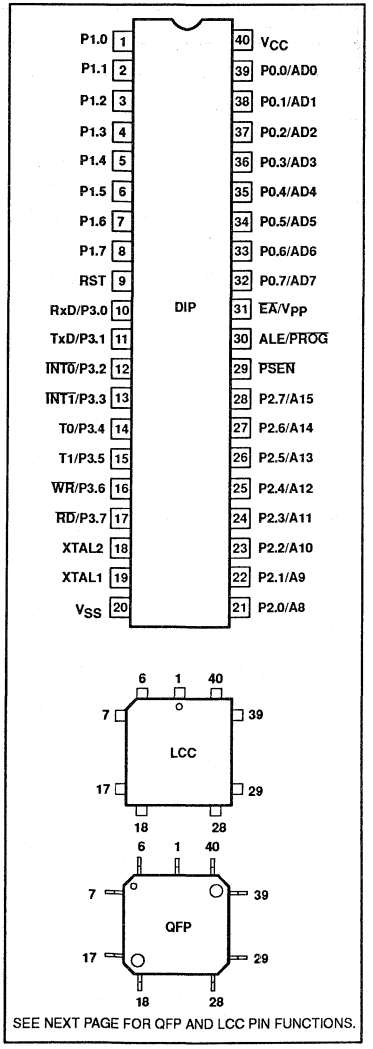
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k X 8 read-only program memory (83C652) EPROM (87C652), a volatile 256 X 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

FEATURES

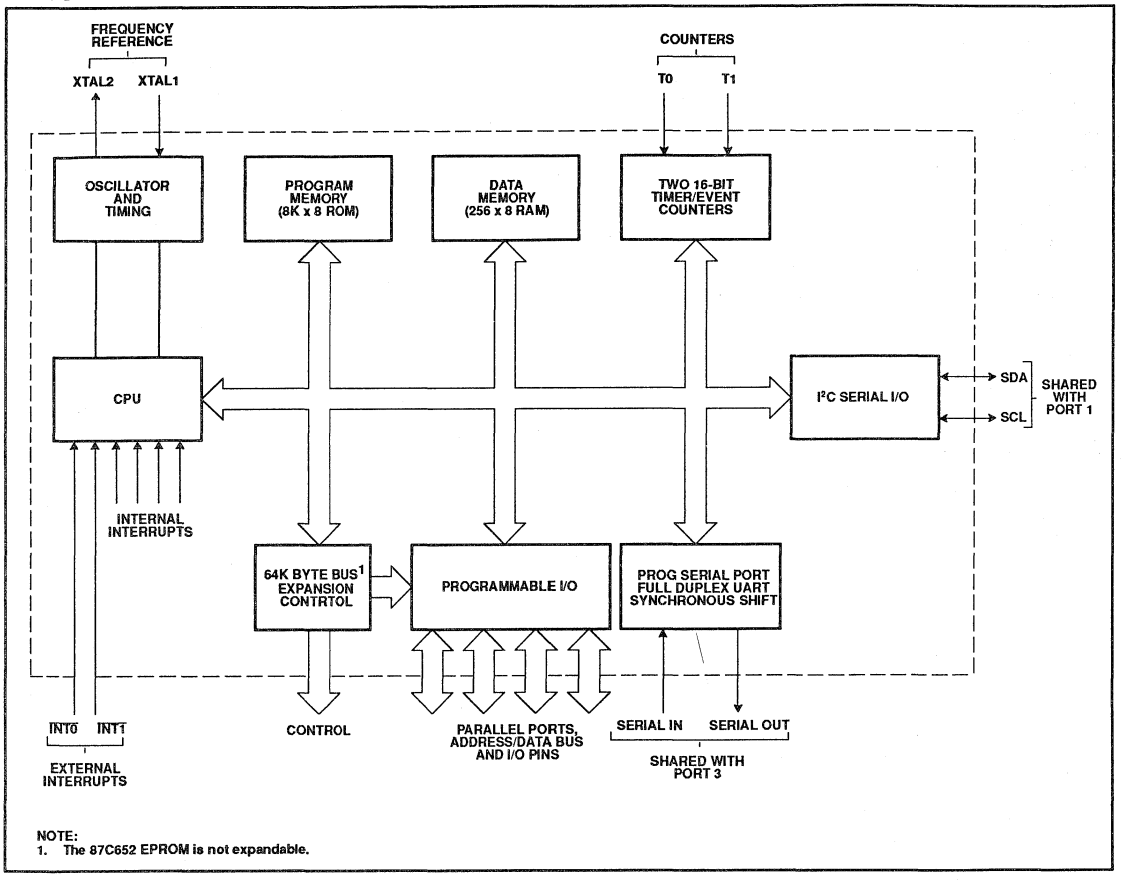
- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes (87C652 EPROM is not expandable)
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



NOTE:
1. The 87C652 EPROM is not expandable.

Low-voltage single-chip 8-bit microcontroller

P83CL580

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

FEATURES

- Full static 80C51 CPU
- 8-bit CPU, ROM, RAM, I/O in a single 56-lead mini-pack
- 6K x 8 ROM, expandable externally to 64K bytes
- 256 bytes RAM, expandable externally to 64K bytes
- Five 8-bit ports, 40 I/O lines
- Three 16-bit timer / event counters
- External memory expandable up to 128K, external ROM up to 64K and / or RAM up to 64K
- On-chip oscillator suitable for RC, LC, quartz crystal or ceramic resonator
- Fifteen source, fifteen vector interrupt structure with two priority levels
- Full duplex serial UART
- I^2C-bus interface for serial transfer on two lines
- A/D converter with power-down mode (8-bit, 4 inputs)
- Pulse width modulated output (8-bit resolution)
- Watchdog timer
- Enhanced architecture with:
  - non-page oriented instructions
  - direct addressing
  - four eight byte RAM register banks
  - stack depth limited only by available internal RAM (max. 256 bytes)
  - multiply, divide, subtract and compare instructions
- STOP and IDLE instructions
- Wake-up via external interrupts at Port 1
- Single supply voltage of 2.5 V to 6.0 V
- Frequency range of 32 kHz to 16 MHz *
- Very low current consumption: typically 5 mA (3 V, 8 MHz)
- Operating temperature range: –40 to +85 °C

* The currently available product is guaranteed up to 12 MHz at 4.5 V. A device covering the range up to 16 MHz at 4.5 V will be available later in 1992.

GENERAL DESCRIPTION

The P83CL580 is manufactured in an advanced CMOS technology. The instruction set of the P83CL580 is based on that of the 8051. The P83CL580 is an 8-bit general purpose microcontroller especially suited for "cordless phones" and mobile communication applications. The device has low power consumption and a wide range of supply voltage. For emulation purposes, the P85CL000 (Piggy-back version) with 256 bytes of RAM is recommended. The P83CL580 has two software selectable modes of reduced activity for further power reduction: Idle and Power-down. The P83CL580 also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 46 two-byte, and 16 three-byte.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
P83CL580 HFT	56	VSO56	plastic	SOT190

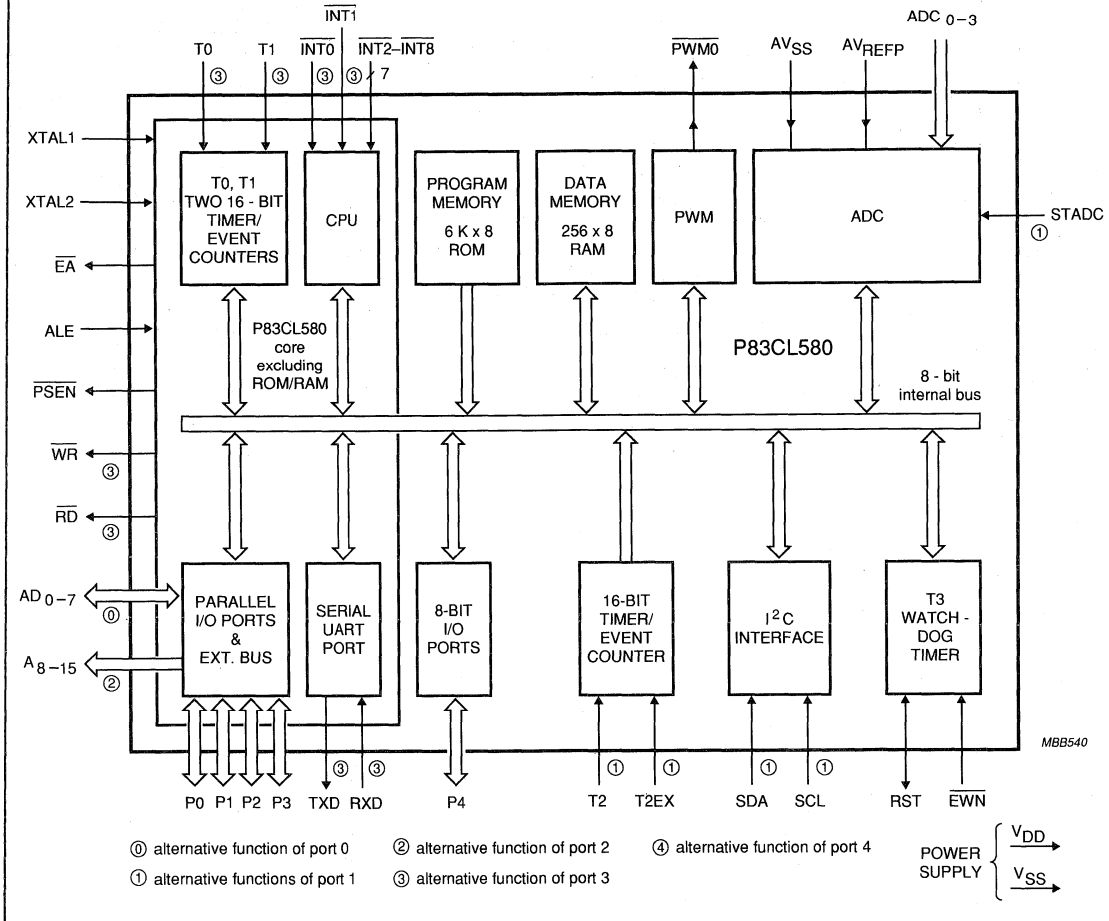


Fig.1 Block diagram.

Philips Semiconductors

Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Products	

83C654/87C654

CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The 83C654/87C654 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 83C654/87C654 has the same instruction set as the 80C51. Two versions of the derivative exist:

83C654 – 16k bytes mask programmable ROM

87C654 – EPROM version

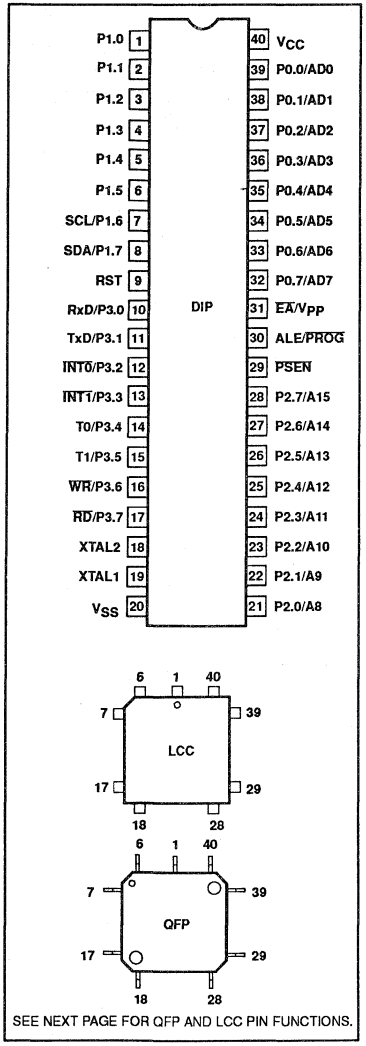
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC654 contains a non-volatile 16k X 8 read-only program memory (83C654) EPROM (87C654), a volatile 256 X 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC654 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12MHz crystal, 58% of the instructions are executed in 1μs and 40% in 2μs. Multiply and divide instructions require 4μs.

FEATURES

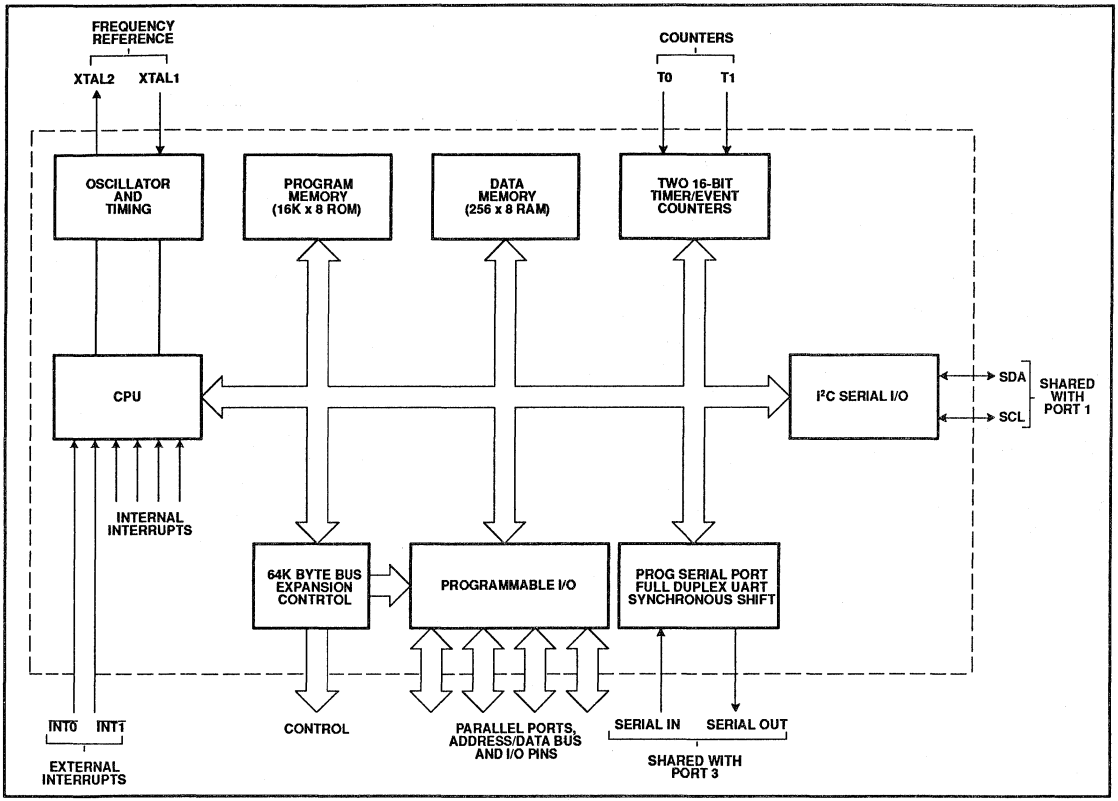
- 80C51 central processing unit
- 16k X 8 ROM expandable externally to 64k bytes
- 256 X 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Five package styles
- Extended temperature ranges
- OTP package available

PIN CONFIGURATION



SEE NEXT PAGE FOR QFP AND LCC PIN FUNCTIONS.

BLOCK DIAGRAM



Philips Semiconductors

Date of Issue	June 15, 1990
Status	Product Specification
Application Specific Product	

83C751/87C751

CMOS single-chip 8-bit microcontroller

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 83C751/87C751 offers the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC751 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

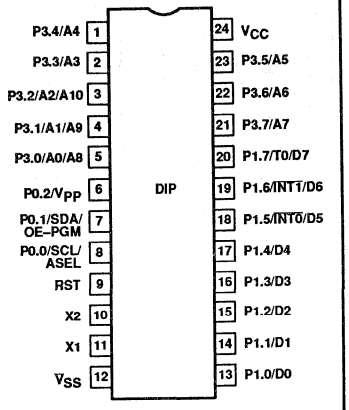
The 8XC751 contains a 2k x 8 ROM (83C751) EPROM (87C751), a 64 x 8 RAM, 19 I/O lines, a 16-bit auto-reload counter/timer, a five-source, fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, and an on-chip oscillator.

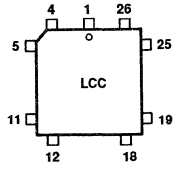
The on-board inter-integrated circuit (I^2C) bus interface allows the 8XC751 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

FEATURES

- 80C51 based architecture
- Inter-Integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 24-pin DIP (300 mil "skinny DIP")
  - 28-pin PLCC
- 87C751 available in erasable quartz lid or one-time programmable plastic packages
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C751)
  2k × 8 EPROM (87C751)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

PIN CONFIGURATION



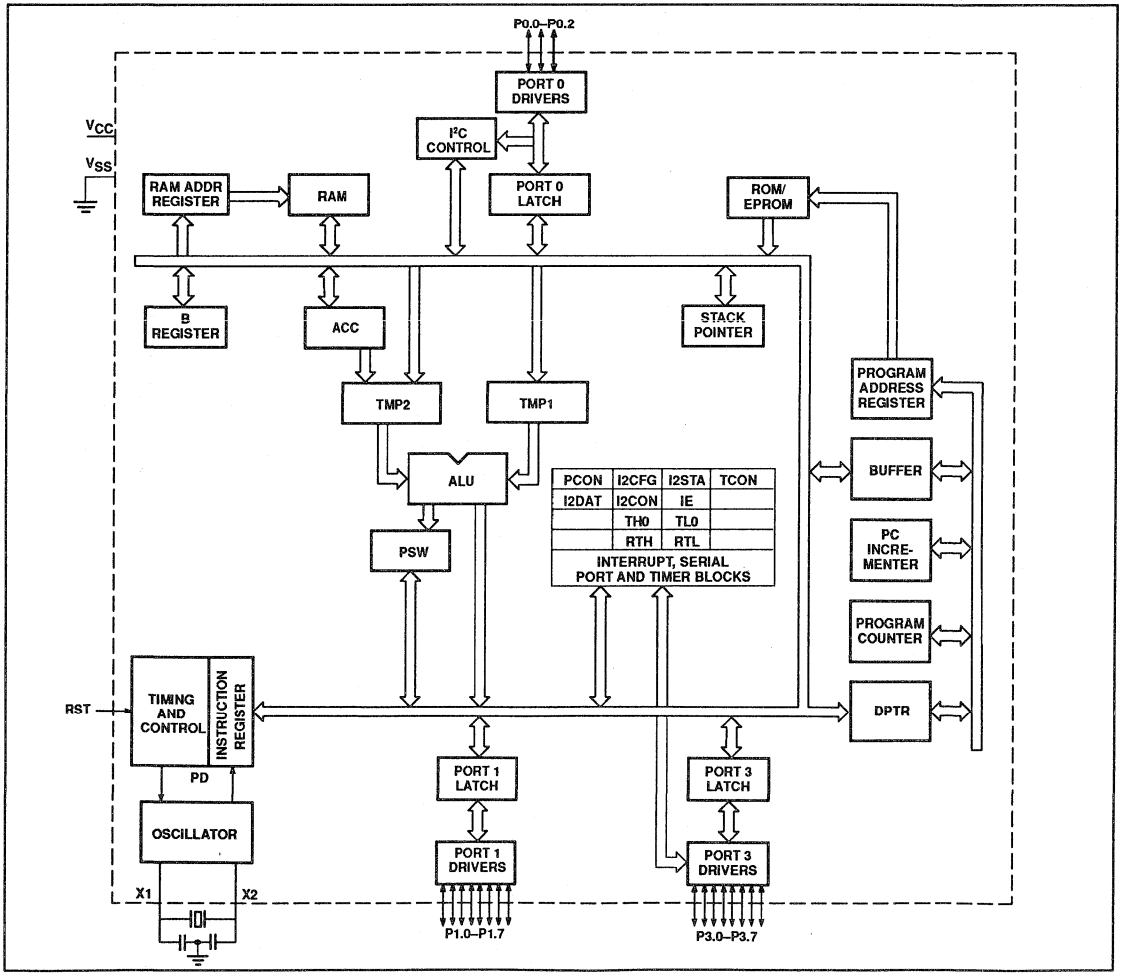


Pin	Function	Pin	Function
1	P3.4/A4	15	P1.0/D0
2	P3.3/A3	16	P1.1/D1
3	P3.2/A2/A10	17	P1.2/D2
4	P3.1/A1/A9	18	P1.3/D3
5	N.C.	19	P1.4/D4
6	P3.0/A0/A8	20	P1.5/INT0/D5
7	P0.2/V_{PP}	21	N.C.
8	P0.1/SDA/OE–PGM	22	N.C.
9	P0.0/SCL/ASEL	23	P1.6/INT1/D6
10	N.C.	24	P1.7/T0/D7
11	RST	25	P3.7/A7
12	X2	26	P3.6/A6
13	X1	27	P3.5/A5
14	V_{SS}	28	V_{CC}

PART NUMBER SELECTION

ROM	EPROM	SPEED	TEMPERATURE AND PACKAGE
	S87C751–1F24	3.5 to 12MHz	0 to +70°C, ceramic DIP
	S87C751–2F24	3.5 to 12MHz	–40 to +85°C, ceramic DIP
	S87C751–4F24	3.5 to 16MHz	0 to +70°C, ceramic DIP
	S87C751–5F24	3.5 to 16MHz	–40 to +85°C, ceramic DIP
S83C751–1N24	S87C751–1N24	3.5 to 12MHz	0 to +70°C, plastic DIP
S83C751–2N24	S87C751–2N24	3.5 to 12MHz	–40 to +85°C, plastic DIP
S83C751–4N24	S87C751–4N24	3.5 to 16MHz	0 to +70°C, plastic DIP
S83C751–5N24	S87C751–5N24	3.5 to 16MHz	–40 to +85°C, plastic DIP
S83C751–1A28	S87C751–1A28	3.5 to 12MHz	0 to +70°C, plastic LCC
S83C751–2A28	S87C751–2A28	3.5 to 12MHz	–40 to +85°C, plastic LCC
S83C751–4A28	S87C751–4A28	3.5 to 16MHz	0 to +70°C, plastic LCC
S83C751–5A28	S87C751–5A28	3.5 to 16MHz	–40 to +85°C, plastic LCC

BLOCK DIAGRAM



Philips Semiconductors

Date of Issue	June 15, 1990
Status	Product Specification
Application Specific Product	

83C752/87C752

CMOS single-chip 8-bit microcontroller with A/D, PWM

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 83C752/87C752 offers many of the advantages of the 80C51 architecture in a small package and at low cost.

The 8XC752 Microcontroller is fabricated with Philips high-density CMOS technology. Philips epitaxial substrate minimizes CMOS latch-up sensitivity.

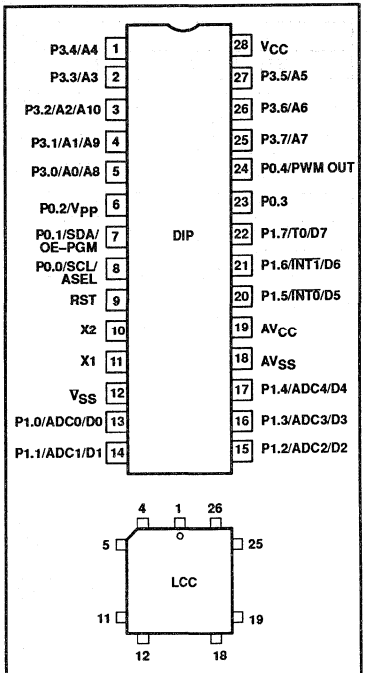
The 8XC752 contains a 2k x 8 ROM (83C752) EPROM (87C752), a 64 x 8 RAM, 21 I/O lines, a 16-bit auto-reload counter/timer, a fixed-priority level interrupt structure, a bidirectional inter-integrated circuit (I^2C) serial bus interface, an on-chip oscillator, a five channel multiplexed 8-bit A/D converter, and an 8-bit PWM output.

The onboard inter-integrated circuit (I^2C) bus interface allows the 8XC752 to operate as a master or slave device on the I^2C small area network. This capability facilitates I/O and RAM expansion, access to EEPROM, processor-to-processor communication, and efficient interface to a wide variety of dedicated I^2C peripherals.

FEATURES

- Available in erasable quartz lid or One-Time Programmable plastic packages
- 80C51 based architecture
- Inter-integrated Circuit (I^2C) serial bus interface
- Small package sizes
  - 28-pin DIP
  - 28-pin PLCC
- Wide oscillator frequency range
- Low power consumption:
  - Normal operation: less than 11mA @ 5V, 12MHz
  - Idle mode
  - Power-down mode
- 2k × 8 ROM (83C752) EPROM (87C752)
- 64 × 8 RAM
- 16-bit auto reloadable counter/timer
- 5-channel 8-bit A/D converter
- 8-bit PWM output/timer
- Fixed-rate timer
- Boolean processor
- CMOS and TTL compatible
- Well suited for logic replacement, consumer and industrial applications

PIN CONFIGURATION

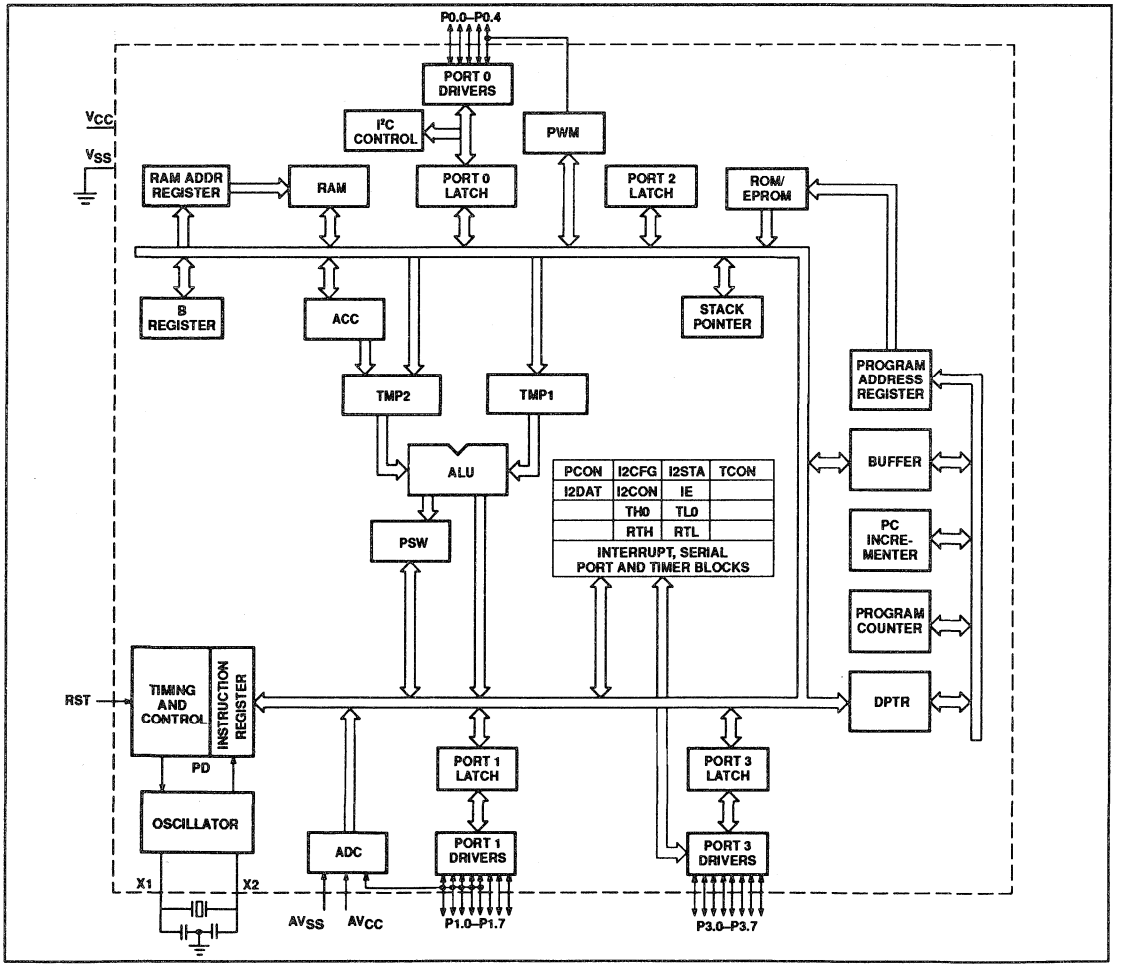


Pin	Function	Pin	Function
1	P3.4/A4	15	P1.2/ADC2/D2
2	P3.3/A3	16	P1.3/ADC3/D3
3	P3.2/A2/A10	17	P1.4/ADC4/D4
4	P3.1/A1/A9	18	AV_{SS}
5	P3.0/A0/A8	19	AV_{CC}
6	$P0.2/V_{PP}$	20	P1.5/INT0/D5
7	P0.1/SDA/OE–PGM	21	P1.6/INT1/D6
8	P0.0/SCL/ASEL	22	P1.7/T0/D7
9	RST	23	P0.3
10	X2	24	P0.4/PWM OUT
11	X1	25	P3.7/A7
12	V_{SS}	26	P3.6/A6
13	P1.0/ADC0/D0	27	P3.5/A5
14	P1.1/ADC1/D1	28	V_{CC}

PART NUMBER SELECTION

ROM	EPROM	SPEED	TEMPERATURE AND PACKAGE
	87C752–1F28	3.5 to 12MHz	0 to +70°C, ceramic DIP
	87C752–2F28	3.5 to 12MHz	–40 to +85°C, ceramic DIP
	87C752–4F28	3.5 to 16MHz	0 to +70°C, ceramic DIP
	87C752–5F28	3.5 to 16MHz	–40 to +85°C, ceramic DIP
83C752–1N28	87C752–1N28	3.5 to 12MHz	0 to +70°C, plastic DIP
83C752–2N28	87C752–2N28	3.5 to 12MHz	–40 to +85°C, plastic DIP
83C752–4N28	87C752–4N28	3.5 to 16MHz	0 to +70°C, plastic DIP
83C752–5N28	87C752–5N28	3.5 to 16MHz	–40 to +85°C, plastic DIP
83C752–1A28	87C752–1A28	3.5 to 12MHz	0 to +70°C, plastic LCC
83C752–2A28	87C752–2A28	3.5 to 12MHz	–40 to +85°C, plastic LCC
83C752–4A28	87C752–4A28	3.5 to 16MHz	0 to +70°C, plastic LCC
83C752–5A28	87C752–5A28	3.5 to 16MHz	–40 to +85°C, plastic LCC
83C752–6A28	87C752–6A28	3.5 to 12MHz	–55 to +125°C, plastic LCC
83C752–6F28	87C752–6F28	3.5 to 12MHz	–55 to +125°C, ceramic DIP
83C752–6N28	87C752–6N28	3.5 to 12MHz	–55 to +125°C, plastic DIP

BLOCK DIAGRAM



Date of Issue	September 6, 1990
Status	Product Specification
Application Specific Product	

80C851/83C851

CMOS single-chip 8-bit microcontroller with on-chip EEPROM

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC20 OR DATASHEET

DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

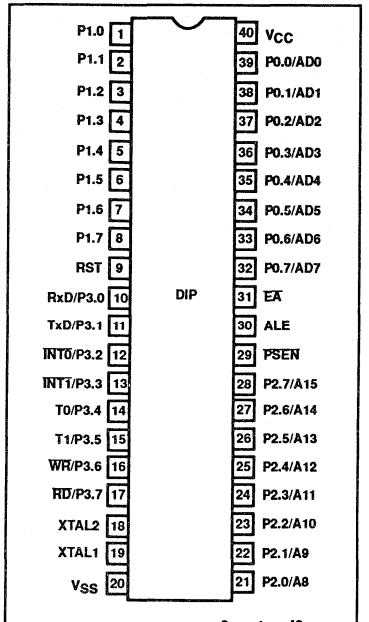
The 80C851/83C851 contains a 4k x 8 ROM with mask-programmable ROM code protection, a 128 x 8 RAM, 256 x 8 EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

FEATURES

- 80C51 based architecture
  - 4k x 8 ROM
  - 128 x 8 RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile 256 x 8-bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 10,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 12MHz
- Two temperature ranges
- Three package styles

PIN CONFIGURATION



Pin	Function	Pin	Function	Pin	Function
1	NC	15	INT1/P3.3	30	P2.6/A14
2	P1.0	16	T0/P3.4	31	P2.7/A15
3	P1.1	17	T1/P3.5	32	PSEN
4	P1.2	18	WR/P3.6	33	ALE
5	P1.3	19	RD/P3.7	34	NC
6	P1.4	20	XTAL2	35	EA
7	P1.5	21	XTAL1	36	P0.7/AD7
8	P1.6	22	V_{SS}	37	P0.6/AD6
9	P1.7	23	NC	38	P0.5/AD5
10	RST	24	P2.0/A8	39	P0.4/AD4
11	RxD/P3.0	25	P2.1/A9	40	P0.3/AD3
12	NC	26	P2.2/A10	41	P0.2/AD2
13	TxD/P3.1	27	P2.3/A11	42	P0.1/AD1
14	INT0/P3.2	28	P2.4/A12	43	P0.0/AD0
		29	P2.5/A13	44	V_{CC}

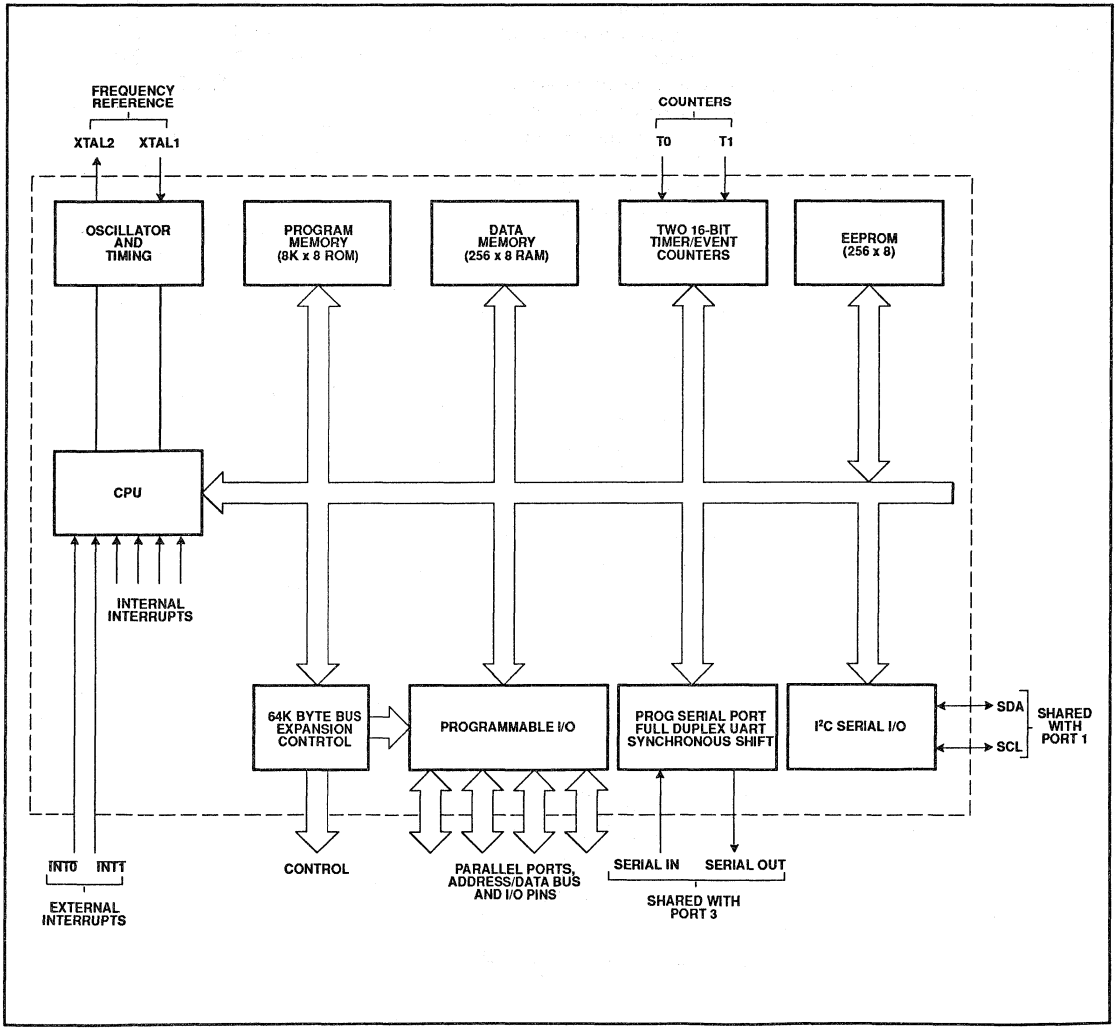
CMOS single-chip EEPROM 8-bit microcontroller

80C851/83C851

PART NUMBER SELECTION

PHILIPS		PHILIPS COMPONENTS-SIGNETICS		TEMPERATURE AND PACKAGE	FREQUENCY (MHz)
ROMless Version	ROM Version	ROMless Version	ROM Version		
PCB80C851P	PCB83C851P	S80C851-1N40	S83C851-1N40	0 to +70°C plastic DIP	1.2 to 12
PCB80C851WP	PCB83C851WP	S80C851-1A44	S83C851-1A44	0 to +70°C plastic LCC	1.2 to 12
PCB80C851H	PCB83C851H	S80C851-1B44	S83C851-1B44	0 to +70°C plastic QFP	1.2 to 12
PCF80C851P	PCF83C851P	S80C851-2N40	S83C851-2N40	–40 to +85°C plastic DIP	1.2 to 12
PCF80C851WP	PCF83C851WP	S80C851-2A44	S83C851-2A44	–40 to +85°C plastic LCC	1.2 to 12
PCF80C851H	PCF83C851H	S80C851-2B44	S83C851-2B44	–40 to +85°C plastic QFP	1.2 to 12

BLOCK DIAGRAM



NE/SA572
Programmable Analog Compandor

Product Specification

DESCRIPTION

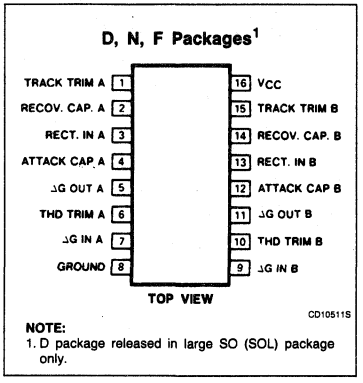
The NE572 is a dual-channel, high-performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full-wave rectifier to detect the average value of input signal, a linearized, temperature-compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high-performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

- **Independent control of attack and recovery time**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external op amp**
- **Wide dynamic range — greater than 110dB**
- **Temperature-compensated gain control**
- **Low distortion gain cell**
- **Low noise — 6μV typical**
- **Wide supply voltage range — 6V – 22V**
- **System level adjustable with external components**

PIN CONFIGURATION



NOTE:
1. D package released in large SO (SOL) package only.

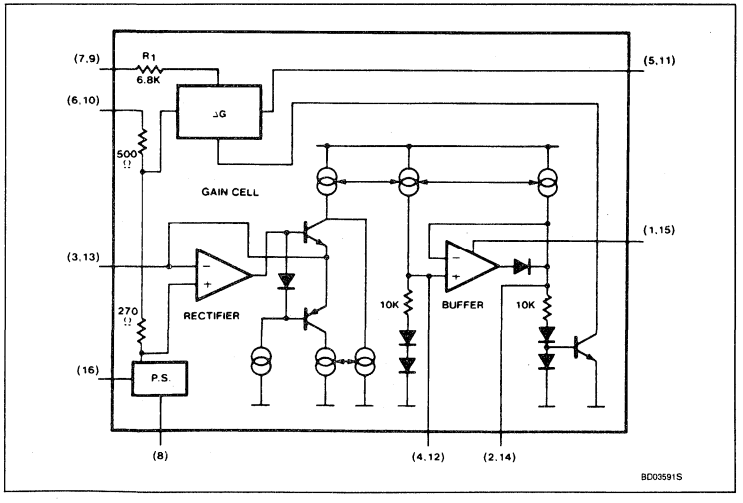
APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High-level limiter**
- **Low-level noise gate**
- **State variable filter**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE572D
16-Pin Plastic DIP	0 to +70°C	NE572N
16-Pin Plastic SO	-40°C to +85°C	SA572D
16-Pin Cerdip	-40°C to +85°C	SA572F
16-Pin Plastic DIP	-40°C to +85°C	SA572N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

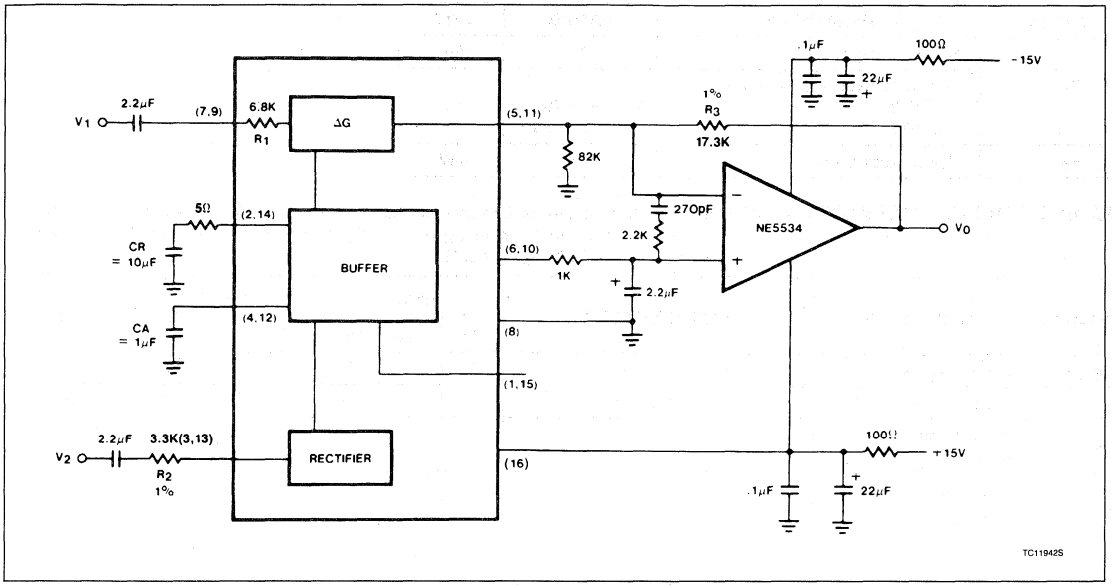
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	V_{DC}
T_A	Operating temperature range NE572 SA572	 0 to +70 −40 to +85	°C
P_D	Power dissipation	500	mW

DC ELECTRICAL CHARACTERISTICS

Standard test conditions (unless otherwise noted) V_{CC} = 15V, T_A = 25°C; Expandor mode (see Test Circuit). Input signals at unity gain level (0dB) = 100mV_{RMS} at 1kHz; $V_1 = V_2$; R_2 = 3.3kΩ; R_3 = 17.3kΩ.

SYMBOL	PARAMETER	TEST CONDITIONS	NE572			SA572			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		22	6		22	V_{DC}
I_{CC}	Supply current	No signal			6			6.3	mA
V_R	Internal voltage reference		2.3	2.5	2.7	2.3	2.5	2.7	V_{DC}
THD	Total harmonic distortion (untrimmed)	1kHz C_A = 1.0μF		0.2	1.0		0.2	1.0	%
THD	Total harmonic distortion (trimmed)	1kHz C_R = 10μF		0.05			0.05		%
THD	Total harmonic distortion (trimmed)	100Hz		0.25			0.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20 − 20kHz)		6	25		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV_{RMS}		±20	±50		±20	±50	mV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dB
	Large-signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0		0.7	3	%
	Tracking error (measured relative to value at unity gain) = [$V_O - V_O$ (unity gain)]dB − V_2dB	Rectifier input V_2 = +6dB V_1 = 0dB V_2 = −30dB V_1 = 0dB		 ±0.2 ±0.5	 −1.5 +0.8		 ±0.2 ±0.5	 −2.5 +1.6	dB
	Channel crosstalk	200mV_{RMS} into channel A, measured output on channel B	60			60			dB
PSRR	Power supply rejection ratio	120Hz		70			70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK/SLOW RECOVERY LEVEL SENSOR

In high-performance audio gain control applications, it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high-performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature-compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current-to-voltage conversion, the VCA features low distortion, low noise and wide dynamic range.

The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor C_A with an internal 10k resistor R_A defines the attack time t_A. The recovery time t_R of a tone burst is defined by a recovery capacitor C_R and an internal 10k resistor R_R. Typical attack time of 4ms for the high-frequency spectrum and 40ms for the low frequency band can be obtained with 0.1μF and 1.0μF attack capacitors, respectively. Recovery time of 200ms can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result, the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100Hz signal, the third harmonic distortion is improved by more than 10dB over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16-pin dual in-line plastic package and in oversized SOL package. It operates over a wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0 – 70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature-compensated gain cells (ΔG), each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\triangle V_{BEQ3-Q4} = \triangle_{BEQ1-Q2}$$

$$(V_{BE} = V_T \ln IC/IS)$$

$$V_T \ln\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T \ln\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T \ln\left(\frac{I_1 + I_{IN}}{I_S}\right) - V_T \ln\left(\frac{I_2 - I_1 - I_{IN}}{I_S}\right) \quad (2)$$

where $I_{IN} = \frac{V_{IN}}{R_1}$

$R_1 = 6.8k\Omega$

$I_1 = 140\mu A$

$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplified to:

$$I_O = \frac{2}{I_2} \cdot I_{IN} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \quad (3)$$

The first term of Equation 3 shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feedthrough due to the mismatch of devices. In the design, this has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin.

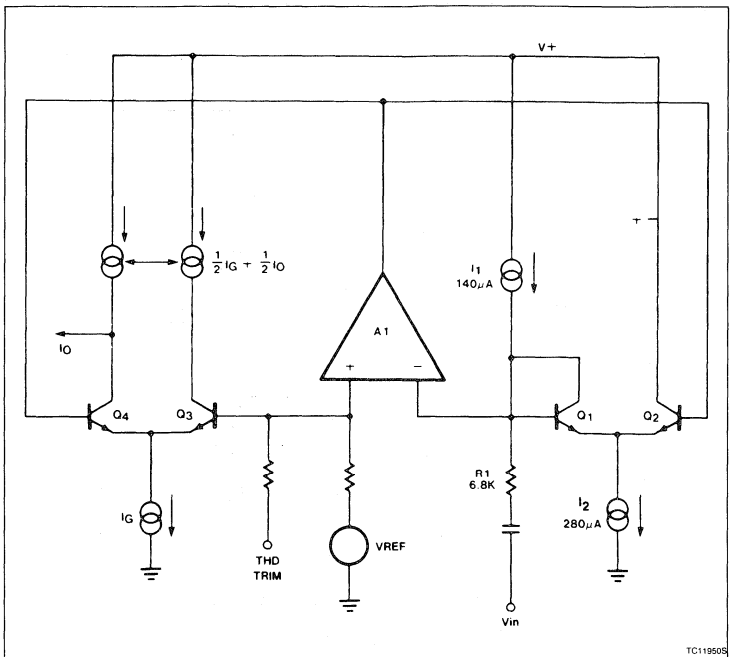


Figure 1. Basic Gain Cell Schematic

The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improve ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of 0.17% typ. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10Hz – 20kHz). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at V_{REF} if the output current I_O is DC coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R_2 and turns on either Q_5 or Q_6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A_2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A_2. The input bias current is typically about 70nA. Frequency response of the gain block A_2 also causes second-order error at high frequency. The collector current of Q_6 is mirrored and summed at the collector of Q_5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \frac{V_{IN} - V_{REF}}{R_2} \quad (4)$$

If V_{IN} is AC-coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{V_{IN(AVG)}}{R_2}$$

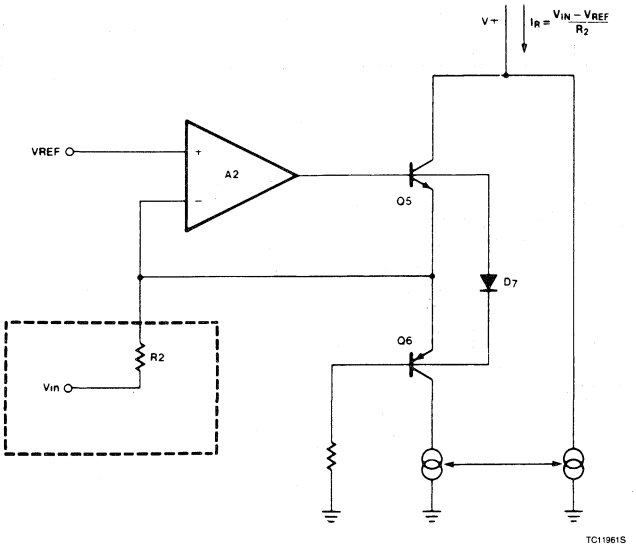


Figure 2. Simplified Rectifier Schematic

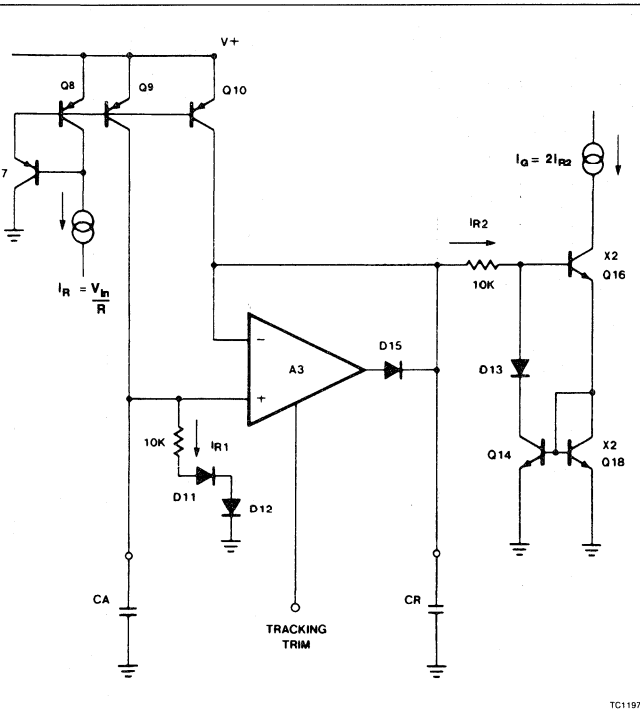


Figure 3. Buffer Amplifier Schematic

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ±1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low-frequency ripple distortion. The low-frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common-mode bias for A_3. For a positive-going input signal, the buffer amplifier acts like a voltage-follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance, the gain Ga(t) for ΔG can be expressed as follows:

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\ e^{\frac{-t}{\tau_A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

Ga_{FNL} = Final Gain

$\tau_A = R_A \cdot CA = 10k \cdot CA$

where τ_A is the attack time constant and R_A is a 10k internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative-going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR · R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\ e^{\frac{-t}{\tau_R}} + G_{R\ FNL}$$

$\tau R = R_R \cdot CR = 10k \cdot CR$

where τR is the recovery time constant and R_R is a 10k internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim pin into A_3 with a current source of ±3μA.

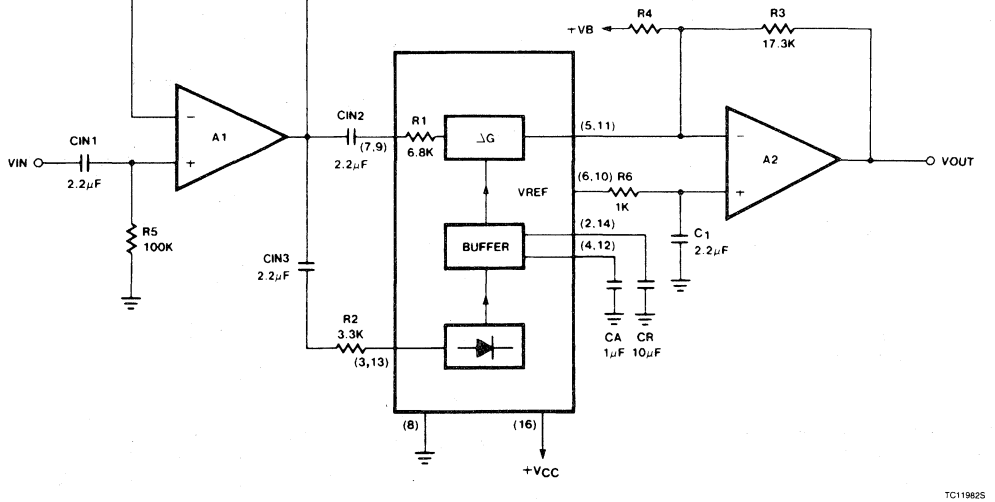


Figure 4. Basic Expandor Schematic

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN(AVG)}}{R_2 \cdot R_1} \qquad (5)$$

($I_1 = 140\mu A$)

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8k internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8k = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R_3/R_2 for desirable system voltage and current levels. A small R_2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high-performance applications, A_2 has to be low-noise, high-speed and wide band so that the high-performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference Pin 6 or 10. Resistor R_4 is used to bias up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN(AVG)}} \right)^{1/2} \quad (7)$$

R_{DC1}, R_{DC2}, and CDC form a DC feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF} \left(1 + \frac{R_{DC1} + R_{DC2}}{R_4} \right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4} \right) \quad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

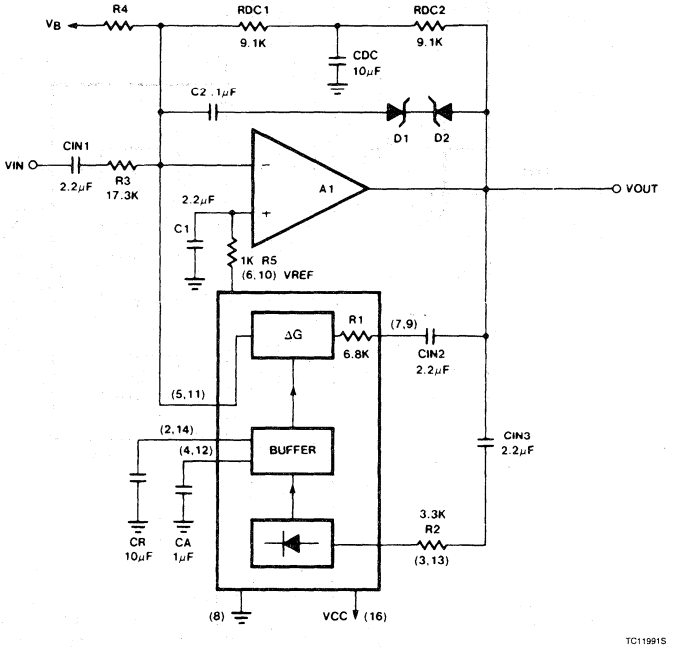


Figure 5. Basic Compressor Schematic

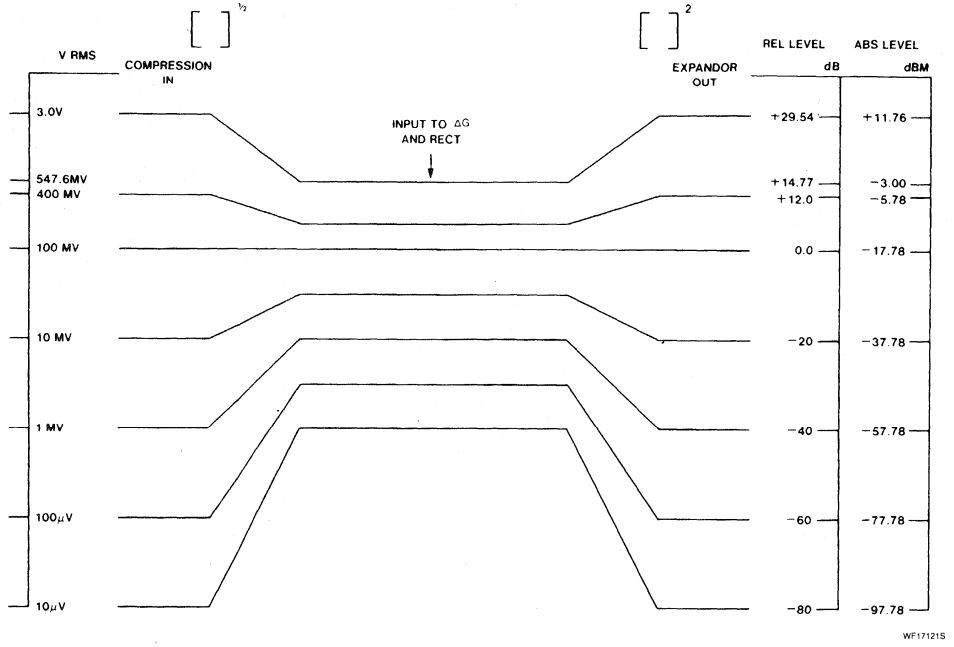


Figure 6. NE572 System Level

Low power compandor — NE/SA576

DESCRIPTION

The NE/SA576 is a unity gain level programmable compandor designed for low power applications. The NE576 is internally configured as an expandor and a compressor to minimize external component count.

The NE576 can operate at 1.8V. During normal operations, the NE576 can operate from at least a 2V battery. If the battery voltage drops to 1.8V, this part will still continue to function, however, turning on the part at a V_{CC} of 1.8V requires two external resistors to bring V_{REF} to half V_{CC}. One resistor connects between V_{CC} and V_{REF}; the other connects from V_{REF} to ground. A typical value for these external resistors is approximately 20k. A lower value can be used, but the power consumption will go up.

The NE576 is available in a 14-pin plastic DIP and SO packages.

FEATURES

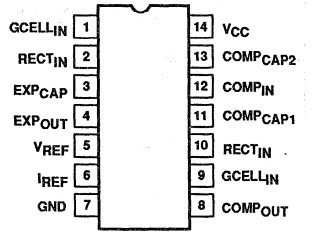
- Operating voltage range: 1.8V to 7V
- Low power consumption (1.4mA @ 3.6V)
- Over 80dB of dynamic range
- Wide input/output swing capability (rail-to-rail)
- Low external component count
- ESD hardened

APPLICATIONS

- Cordless telephone
- Consumer audio
- Wireless microphones
- Modems
- Electric organs
- Hearing aids
- Automatic level control

PIN CONFIGURATION

D and N Packages



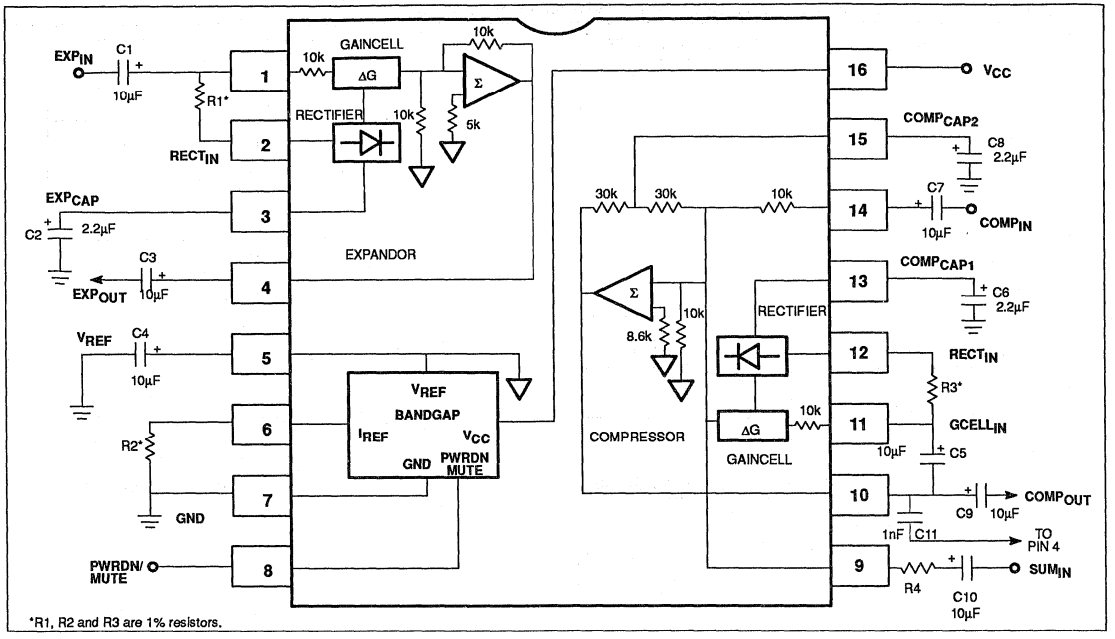
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE576N
14-Pin Plastic SO	0 to +70°C	NE576D
14-Pin Plastic DIP	–40 to +85°C	SA576N
14-Pin Plastic SO	–40 to +85°C	SA576D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE576	SA576	
V_{CC}	Supply voltage	8	8	V
T_A	Operating ambient temperature range	0 to +70	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	–65 to +150	°C
θ_{JA}	Thermal impedance DIP SO	90 125	90 125	°C/W °C/W

BLOCK DIAGRAM and TEST AND APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.6VDC, compandor 0dB level = –20dBV = 100mV_{RMS}, output load R_L = 10kΩ, Freq = 1kHz, unless otherwise specified. R1, R2 and R3 are 1% resistors.

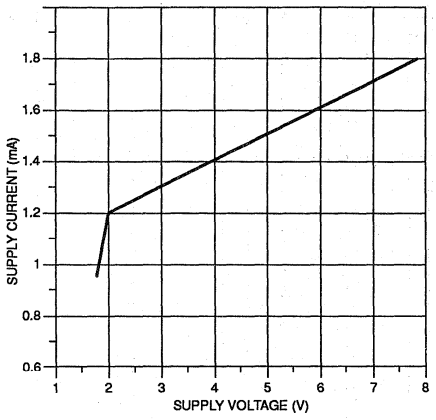
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA576			
			MIN	TYP	MAX	
V_{CC}	Supply voltage[1]		2	3.6	7	V
I_{CC}	Supply current	No signal R_2 = 100kΩ		1.4	3	mA
V_{REF}	Reference voltage[2]	V_{CC} = 3.6V		1.8		V
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.25	1.5	%
E_{NO}	Expandor output noise voltage	BW = 20kHz, R_S = 0Ω		10	30	µV
0dB	Unity gain level	0dB at 1kHz	–1.5	0.18	1.5	dB
V_{OS}	Output voltage offset	No signal	–150	1	150	mV
	Expandor output DC shift	No signal to 0dB	–100	7	100	mV
	Tracking error relative to 0dB output	-20dB expandor	–1.0	0.3	1.0	dB
	Crosstalk, COMP to EXP	1kHz, 0dB, C_{REF} = 10µF		–80		dB
V_O	Output swing low			0.2		V
	Output swing high			V_{CC} – 0.2		V

NOTE:
1. Operation down to V_{CC} = 1.8V is possible, see description on front page of NE576 data sheet.
2. Reference voltage, V_{REF}, is typically at 1/2 V_{CC}.

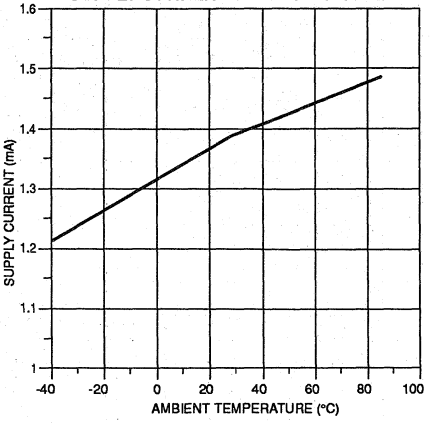
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.6V, T_A = 25°C, R1=R3=18.7kΩ, R2=24.3kΩ, 0dB level = 100mV, Freq. = 1kHz

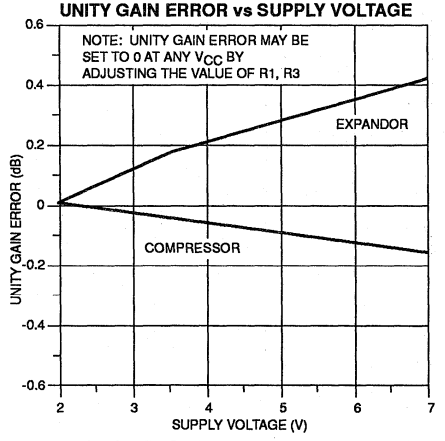
SUPPLY CURRENT vs SUPPLY VOLTAGE



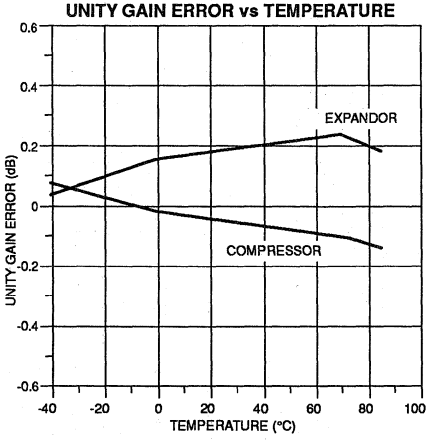
SUPPLY CURRENT vs TEMPERATURE



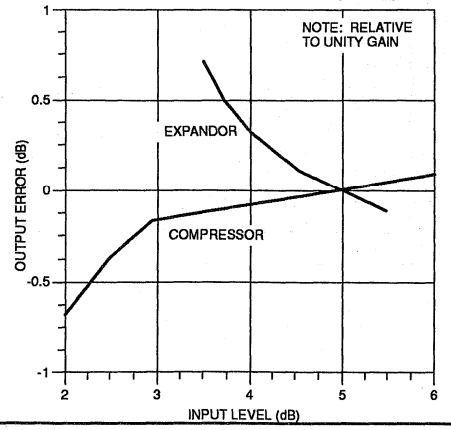
UNITY GAIN ERROR vs SUPPLY VOLTAGE



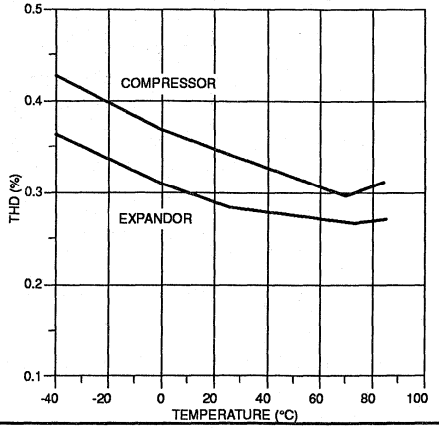
UNITY GAIN ERROR vs TEMPERATURE



TRACKING ERROR vs INPUT LEVEL



THD vs TEMPERATURE



FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT CMOS MICROCONTROLLER

DESCRIPTION

The PC80CXX family of single-chip 8-bit CMOS microcontrollers consists of:

- The PCB80C49 with resident mask programmed 2 K x 8 ROM, 128 x 8 RAM.
- The PCB80C39 without resident program memory for use with external EPROM/ROM, 128 x 8 RAM.

All versions are pin and function compatible to their NMOS counter parts but with additional features and high performance.

The PC80CXX family are designed to be efficient control processors as well as arithmetic processors. Their instruction set allows the user to directly set and reset individual I/O, and to test individual individual bits within the accumulator. A large variety of branch and table look-up instructions enable efficient implementation of standard logic functions. Code efficiency is high; over 70% of the instructions are single byte; all others are two byte.
An on-chip 8-bit counter is provided, which can count either machine cycles (÷ 32) or external events. The counter can be programmed to cause an interrupt to the processor.
Program and data memories can be expanded using standard devices. Input/output capabilities can be expanded using standard devices.
The family has low power consumption and in addition a power down mode is provided.
For further detailed information see the 8048 family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-pin package
- PCB80C49: 2K x 8 ROM, 128 x 8 RAM
- Internal counter/timer
- Internal oscillator, clock driver
- Single-level interrupts: external and counter/timer
- 17 internal registers: accumulator, 16 addressable registers
- Over 90 instructions: 70% single byte
- All instructions: 1 or 2 cycles
- Easily expandable memory and I/O
- TTL compatible inputs and outputs
- Single 5 V supply
- Wide frequency operating range
- Low current consumption
- Available with extended temperature ranges: (PCB version) 0 to + 70 °C
  (PCF version) −40 to + 85 °C
  (PCA version) −40 to + 110 °C
- Frequency range: 1 to 15 MHz for all temperature ranges

APPLICATIONS

- Peripheral interfaces and controllers
- Test and measurement instruments
- Sequencers
- Audio/video systems
- Environmental control systems
- Modems and data enciphering

PACKAGE OUTLINES

PCB/F/A80C39/C49P: 40-lead DIL; plastic (SOT129).
PCB/F/A80C39/C49WP: 44-lead PLCC; plastic leaded chip carrier (SOT187AA).

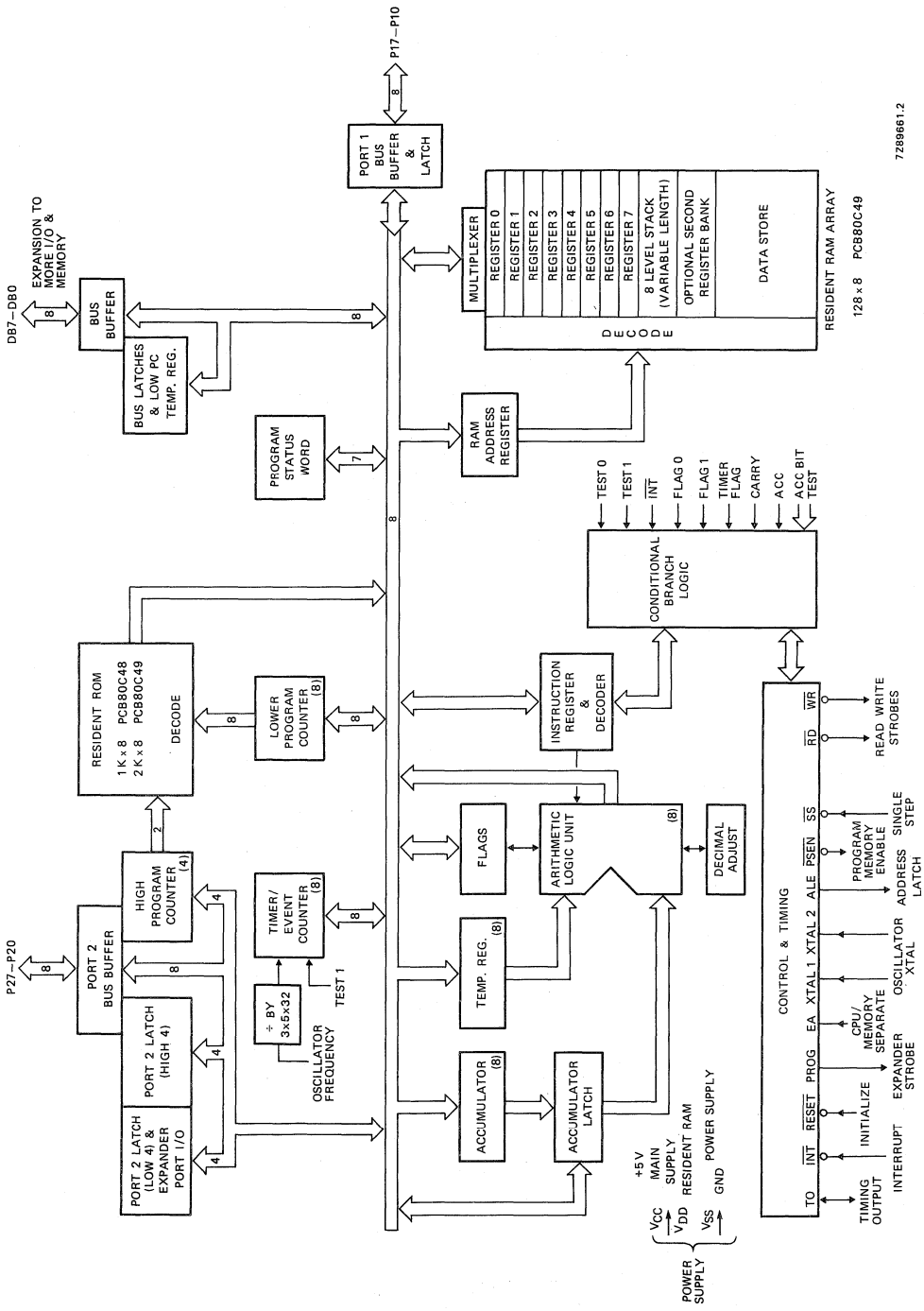


Fig. 1 Block diagram.

I²C-BUS CONTROLLER

GENERAL DESCRIPTION

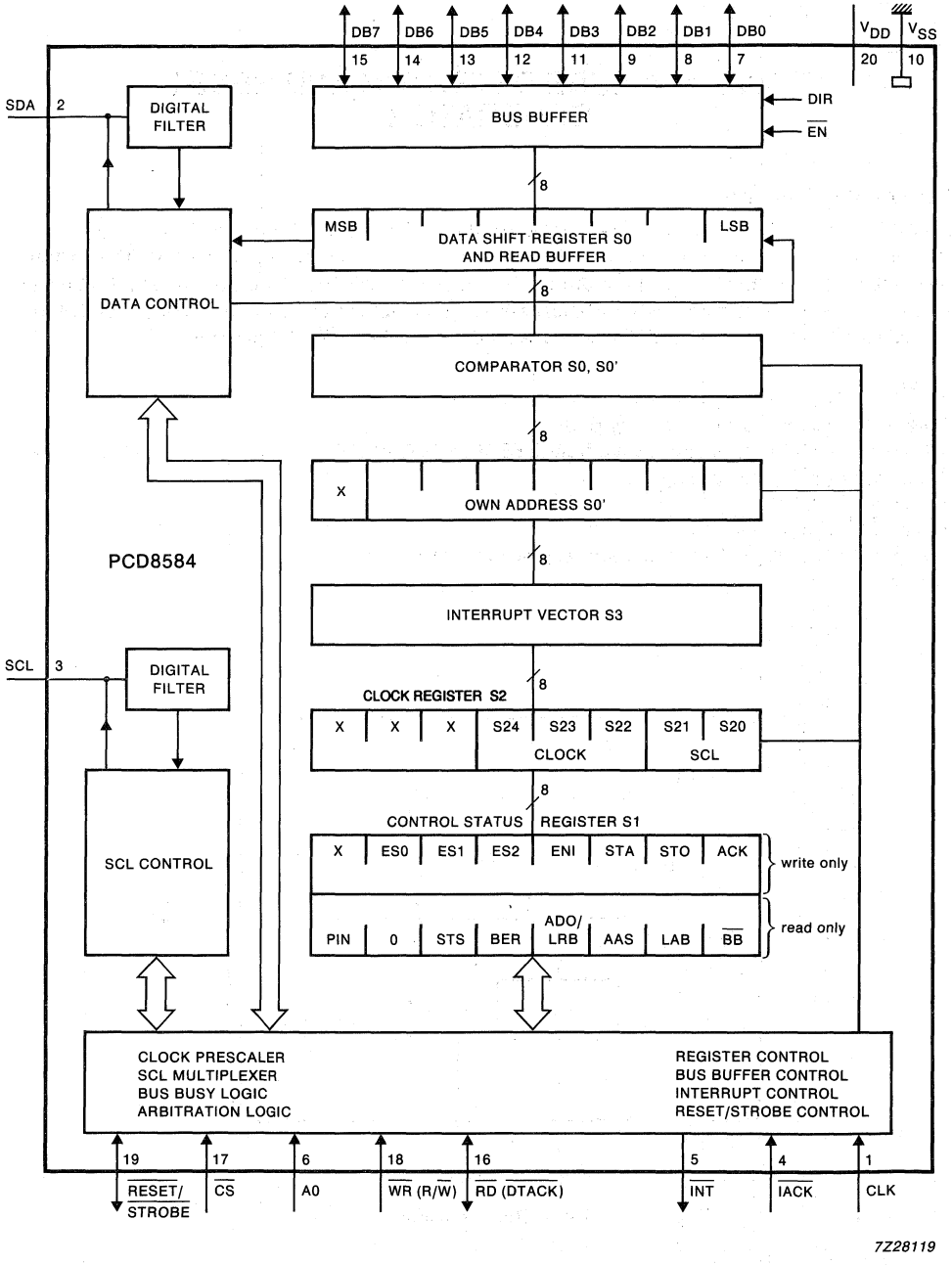
The PCD8584 is an integrated circuit designed in CMOS technology which serves as an interface between most standard parallel-bus microcontrollers/processors and the serial I²C-bus. The PCD8584 provides both master and slave functions. Communication with the I²C-bus is carried out on a byte-wise basis using interrupt or polled handshake. It controls all the I²C-bus specific sequencing, protocol, arbitration and timing. The PCD8584 allows parallel-bus systems to communicate bidirectionally with the I²C-bus.

Features

- Parallel-bus/I²C-bus protocol converter
- Compatible with most parallel-bus processors including MAB8049, MAB8051, SCN68000 and Z80
- Automatic selection of bus interface
- Programmable interrupt vector
- Multi-master capability
- I²C-bus monitor mode
- Long-distance mode
- Operating supply voltage 4.5 to 5.5 V
- Operating temperature range −20 to + 70 °C

PACKAGE OUTLINES

PCD8584P: 20-lead DIL; plastic (SOT146).
PCD8584T: 20-lead mini-pack; plastic (SO20; SOT163A).



7Z28119

Where:

( ) indicate the SCN68000 pin name designations.
X = don't care.

Fig.1 Block diagram.

POWER FAILURE DETECTOR AND RESET GENERATOR

GENERAL DESCRIPTION

The PCF1252-X family are CMOS voltage detectors designed especially for power-ON/OFF detection in microcontroller/microprocessor systems (for initialization and data storage purposes). The output $\overline{POWF}$ is activated at a precise, temperature stable, trip-point. The RESET output has a built-in delay with duration determined by an external capacitor (C_{CT}). A second comparator (comparator 2) has been included to allow for the possibility of a second monitoring point in the system.

Features

- Low current consumption, typically 6 μA
- 10 versions available, trip-points vary from 2.55 V to 4.75 V
- Temperature stable trip-point
- Variable RESET delay
- Reset polarity selection
- Comparator for second level detection (e.g. overvoltage detection)
- Advance warning of power failure

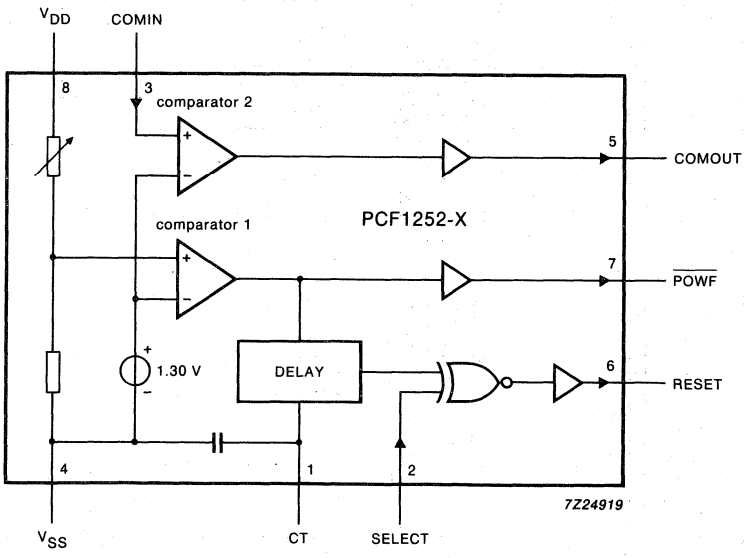


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1252-XP: 8-lead DIL; plastic (SOT97).
PCF1252-XT: 8-lead mini-pack; plastic (SO8; SOT96A).

INFRARED REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

GENERAL DESCRIPTION

The PCF1254 is intended for remote control systems. The circuit can be used to transmit an individual code to a receiver by infrared radiation. The code is stored in an EEPROM which is programmed with 5 V by the equipment manufacturer. Application in identification and security systems are also possible.

Features

- 22 bits of EEPROM code with automatic 2-bit preamble
- Two operating modes: single or repetitive transmission
- Supply voltage range 2.5 V to 6.5 V
- High output current drive (typ. 50 mA at 5 V)
- Operating ambient temperature range −40 to + 85 °C

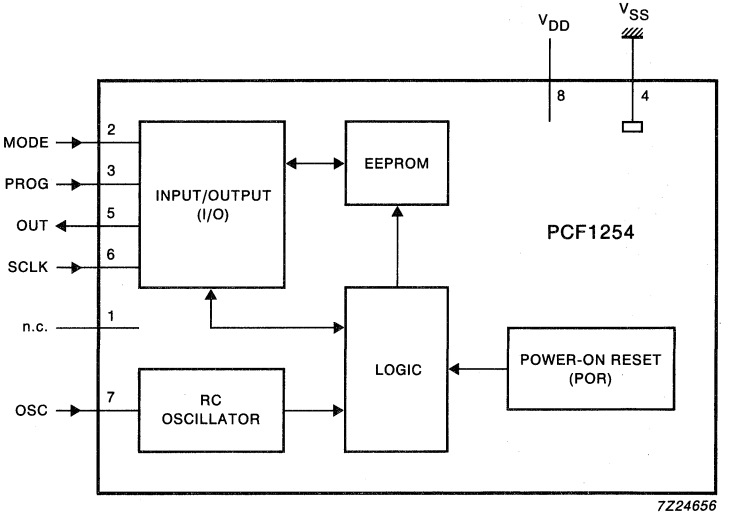


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF1254P: 8-lead DIL; plastic (SOT97).
PCF1254T: 8-lead mini-pack; plastic (SO8; SOT96A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

18-ELEMENT BAR GRAPH LCD DRIVER

GENERAL DESCRIPTION

The PCF1303T is an 18-element bar graph LCD driver with linear relation to control voltage (V_c) when in pointer or thermometer mode.

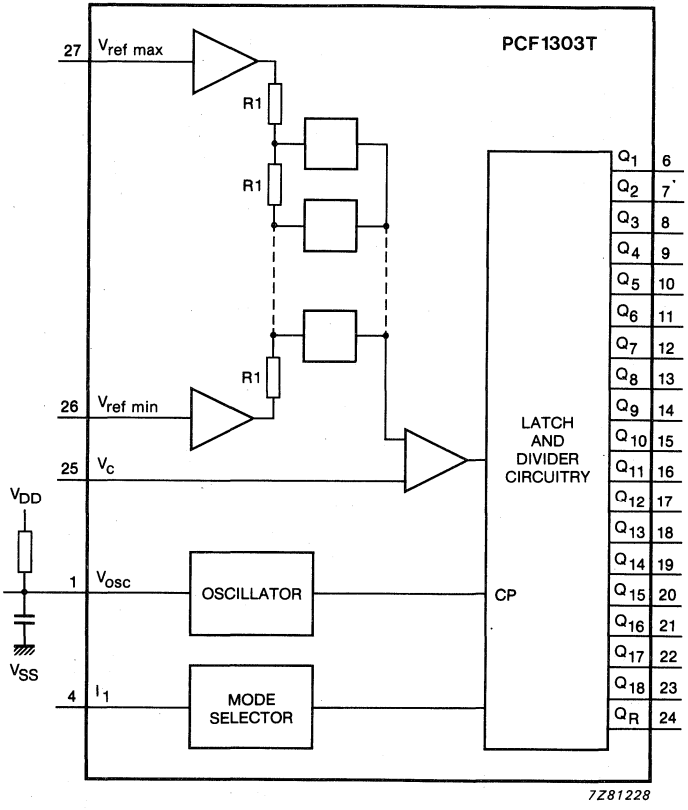


Fig. 1 Block diagram.

PACKAGE OUTLINE

PCF1303T: 28-lead mini-pack; plastic (SO28; SOT136A).

LCD controller/driver for 2-line x 24 or 4-line x 12 character displays

PCF2115

FEATURES

- Single-chip LCD controller/driver
- 1 or 2-line display with up to 24 characters per line or 4 lines of up to 12 characters per line
- 5 x 7 character format plus cursor (5 x 8 for kana and user defined symbols)
- On-chip generation of LCD supply voltage (external supply also possible)
- On-chip generation of intermediate LCD bias voltages
- On-chip oscillator requires no external components (external clock is also possible)
- Display data RAM: 80 characters
- Character generator ROM: 240 5 x 8 characters
- Character generator RAM: 8 5 x 8 characters
- 4 or 8-bit parallel I²C-bus
- CMOS/TTL compatible
- 32 row, 60 column outputs
- MUX rates 1:32 and 1:16 (for 4, 2 and 1-line displays respectively)
- Uses common 11 code instruction set
- Optimized for single-plane wiring applications
- Logic supply voltage range, V_{DD} - V_{SS} = 2.5 to 6.0 V
- Display supply voltage range, V_{DD} - V_{LCD} = 3.5 to 9.0 V
- Low power consumption.

APPLICATIONS

- Car radios
- Telecom equipment
- Portable instruments
- Point-of-sale terminals

GENERAL DESCRIPTION

The PCF2115 is a low-power CMOS LCD controller and driver which has been designed to drive a split screen dot matrix LCD display of 1 or 2 lines x 24 characters or 4 lines x 12 characters with a 5 x 8-dot format. All essential functions for the display are provided on a single chip, including on-chip generation of LCD bias voltages. This results in a minimum requirement of external components and lower system power consumption. The chip contains a character generator and can display alphnumeric and kana characters. The PCF2115 can interface to the majority of microcontrollers via a 4 or 8-bit I²C-bus.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF2115	108	CPGA108	CERAMIC	SOT265

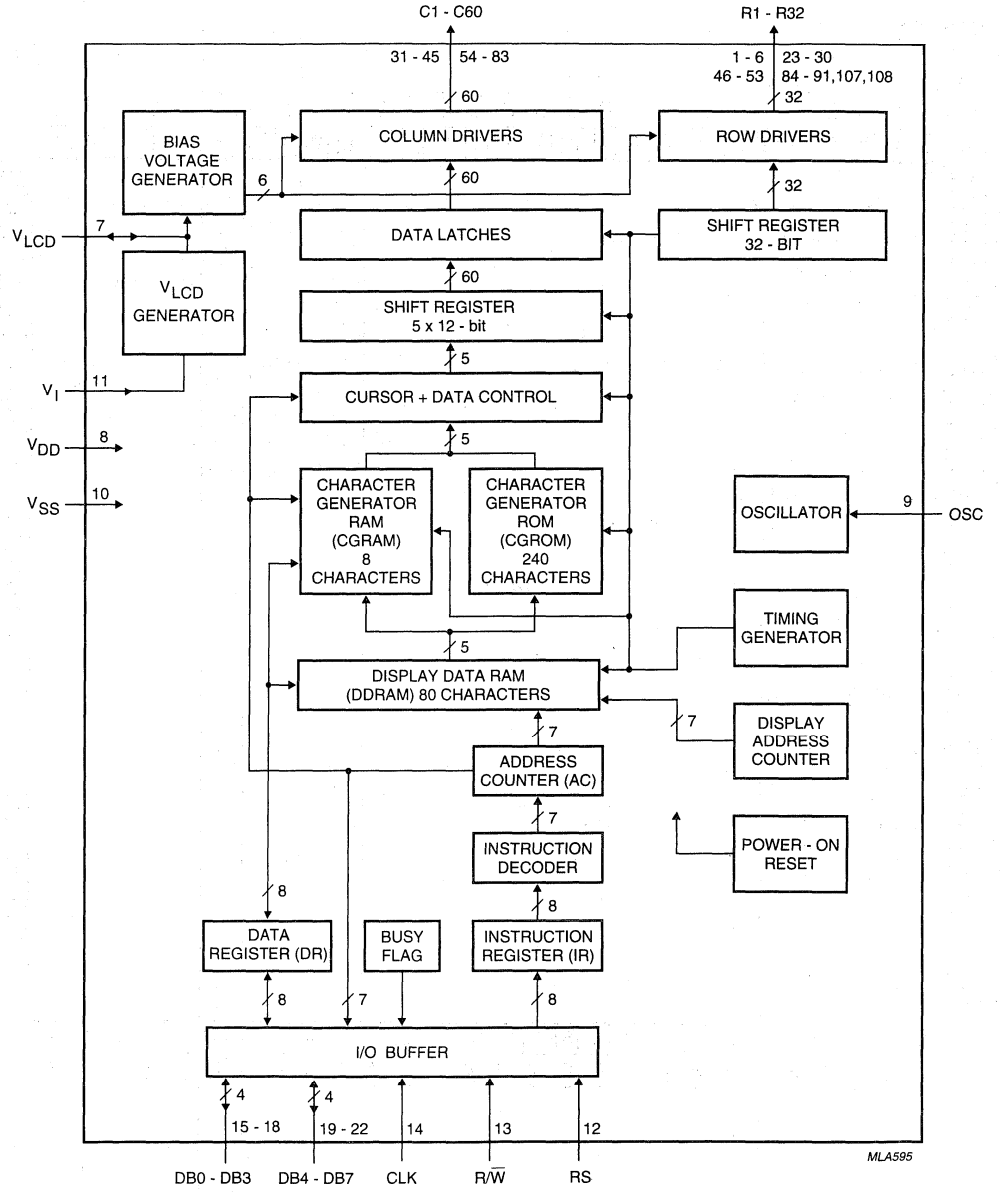


Fig.1 Block diagram.

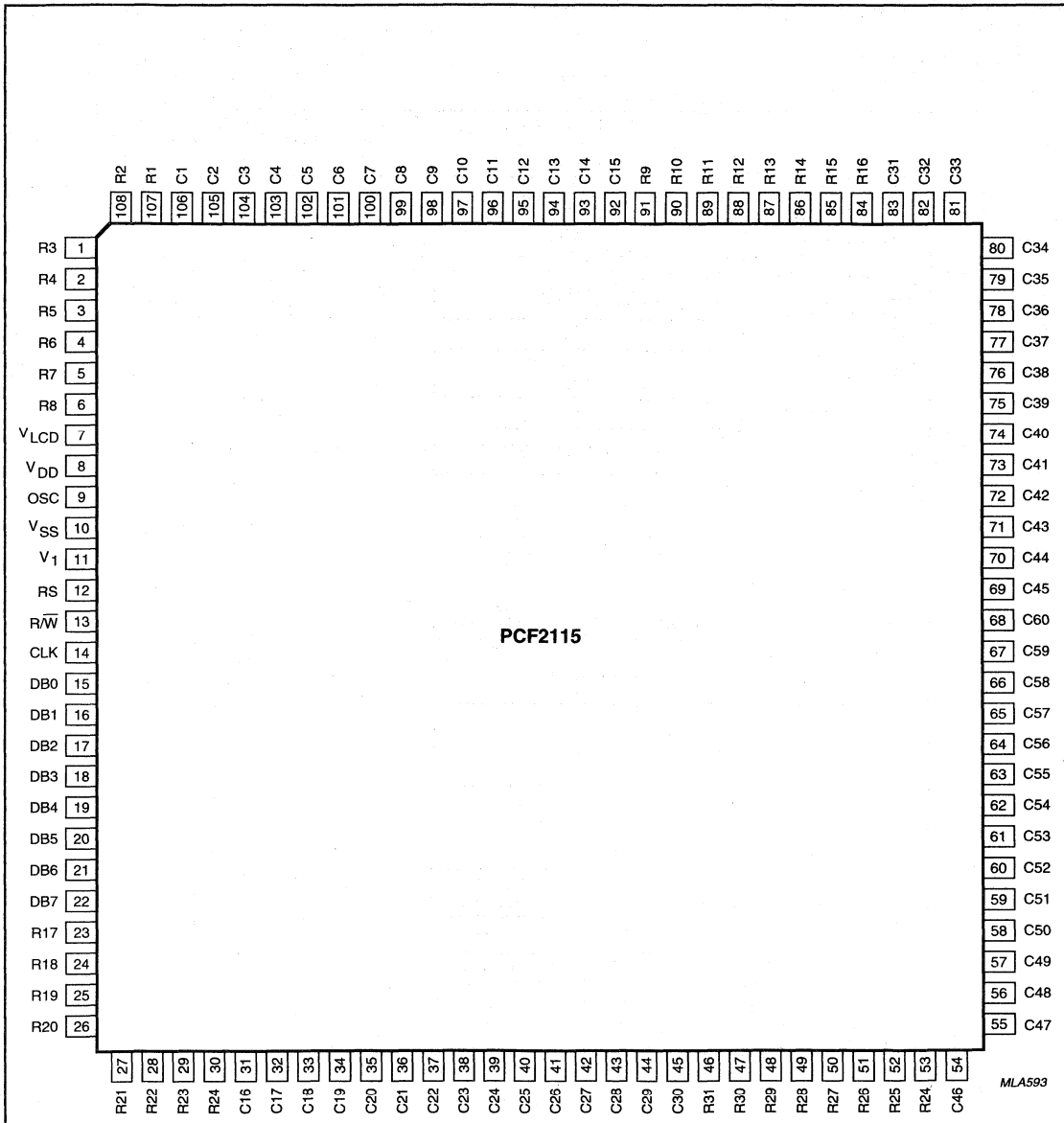


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
R1-R8	1 - 6, 107, 108	LCD row driver outputs
V_{LCD}	7	LCD supply voltage
V_{DD}	8	positive supply voltage
OSC	9	oscillator/external clock input
V_{SS}	10	ground (logic)
V_I	11	control input for V_{LCD}
RS	12	register select input
R/$\overline{W}$	13	read/write input
CLK	14	data bus clock input
DB0 - DB7	15 - 22	bidirectional data bus inputs
R17 - R24	23 - 30	LCD row driver outputs
C16 - C30	31 - 45	LCD column driver outputs (16 to 30 and 75 to 61)
R32 - R25	46 - 53	LCD row driver outputs
C46 - C60	54 - 68	LCD column driver outputs (46 to 60 and 105 to 91)
C45 - C31	69 - 83	LCD column driver outputs (45 to 31 and 106 to 120)
R16 - R9	84 - 91	LCD row driver outputs
C15 - C1	92 - 106	LCD column driver outputs (15 to 1 and 76 to 90)

APPLICATION INFORMATION

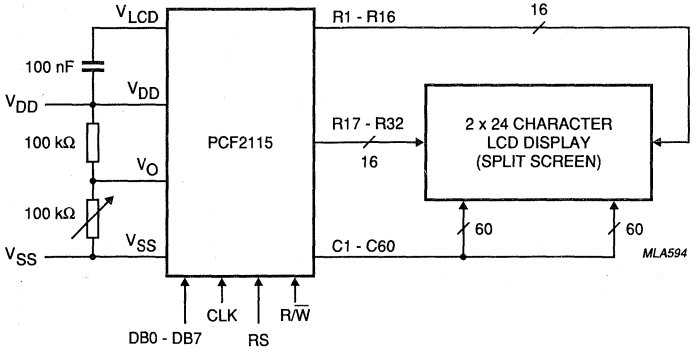


Fig.3 Typical application.

SINGLE-CHIP 8-BIT MICROCONTROLLERS WITH I²C-BUS INTERFACE

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84C00, PCF84C21/C, PCF84C41/C and PCF84C81/C microcontrollers. The PCF84C21C, PCF84C41C and PCF84C81C operate at a higher clock frequency. Each device has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits. On-chip RAM and ROM content is as follows:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 64 x 8 RAM, 2 K x 8 ROM
- PCF84C41 – 128 x 8 RAM, 4 K x 8 ROM
- PCF84C81 – 256 x 8 RAM, 8 K x 8 ROM

These efficient controllers also perform well as arithmetic processors. They have facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set is similar to that of the MAB8048.

These microcontrollers are members of the 84CXXX family. For detailed information, consult the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2K, 4 K or 8 K x ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs, one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter and serial I/O
- I²C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz ; C versions: 1 MHz to 12 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 to 5,5 V)
- STOP and IDLE modes
- Power-on reset circuit
- Operating temperature range: −40 to +85 °C
- High current on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00).

For following sections see 84CXXX family specification

Program memory
Data memory
Program counter stack
IDLE and STOP modes
I/O facilities
Serial I/O
Interrupts
Oscillator
Timer/event counter
Program status word

Program counter
Central processing unit
Conditional branch logic
Test input T1

Power-on reset
Instruction set

PACKAGE OUTLINES

PCF84C21/41/81P: 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T: 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (supports up to 28-pin EPROM).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

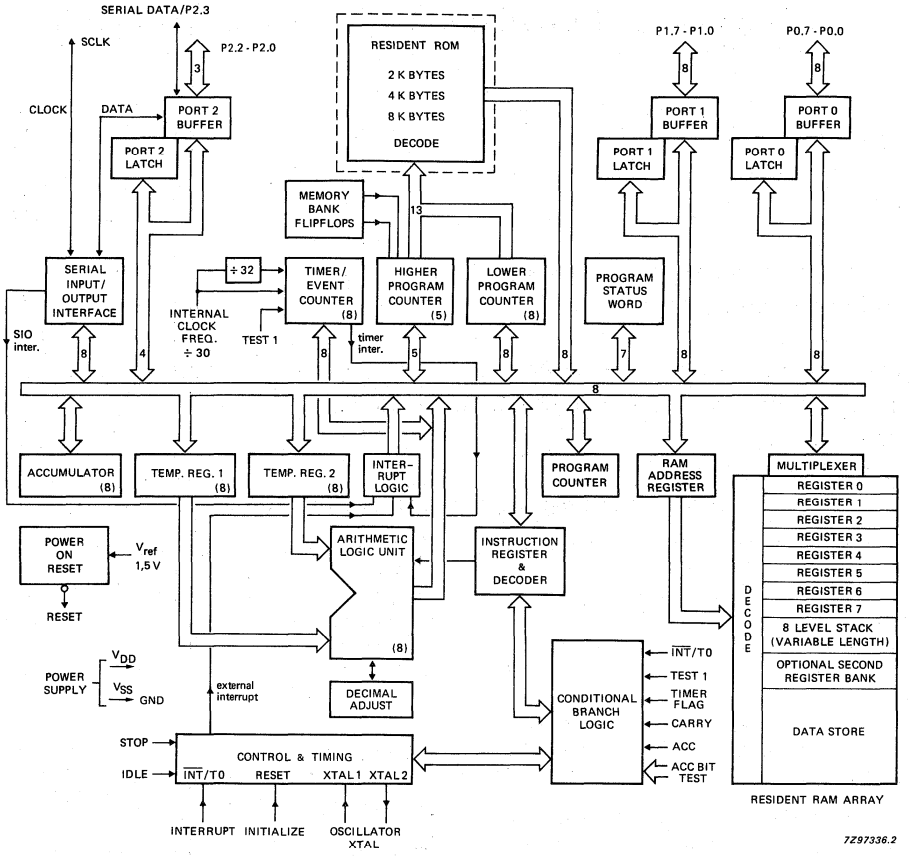


Fig. 1 Block diagram.

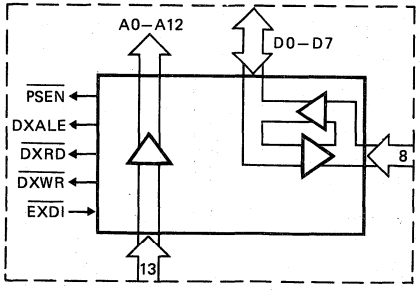
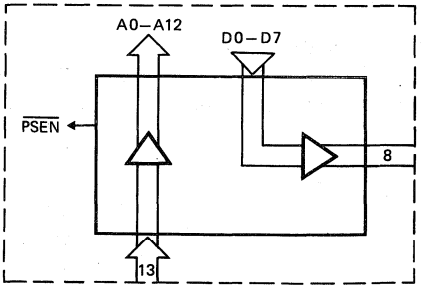


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.



7Z20149.1

Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

8-Bit Microcontroller

PCF84C12A, PCF84C22A, PCF84C42A

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 20-lead package
- 1k ROM bytes (PCF84C12A)
- 2k ROM bytes (PCF84C22A)
- 4k ROM bytes (PCF84C42A)
- 64 RAM bytes
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 13 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter 1
- Two single-level vectored interrupts: external, 8-bit programmable timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- Stop and idle modes
- Logic supply V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz - Operating temperature range: –40 °C to 85 °C
- Manufactured in silicon gate CMOS process

GENERAL DESCRIPTION

This data sheet details the specific properties of the PCF84C12A, PCF84C22A and PCF84C42A. The shared characteristics of the PCF84CXXXA family of microcontrollers are described in the PCF84CXXXA family data sheet, which should be read in conjunction with this publication.

The PCF84C12A, PCF84C22A and PCF84C42A are general purpose CMOS microcontrollers with 1k, 2k and 4k bytes of program memory, respectively. They include 64 bytes of RAM and 13 I/O port lines. The instruction set is based on that of the MAB8048 and is software compatible with the PCF84CXXXA family.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF84C12AP/22AP/42AP	20	DIL	plastic	SOT146
PCF84C12AT/22AT/42AT	20	mini-pack	plastic	SOT163A

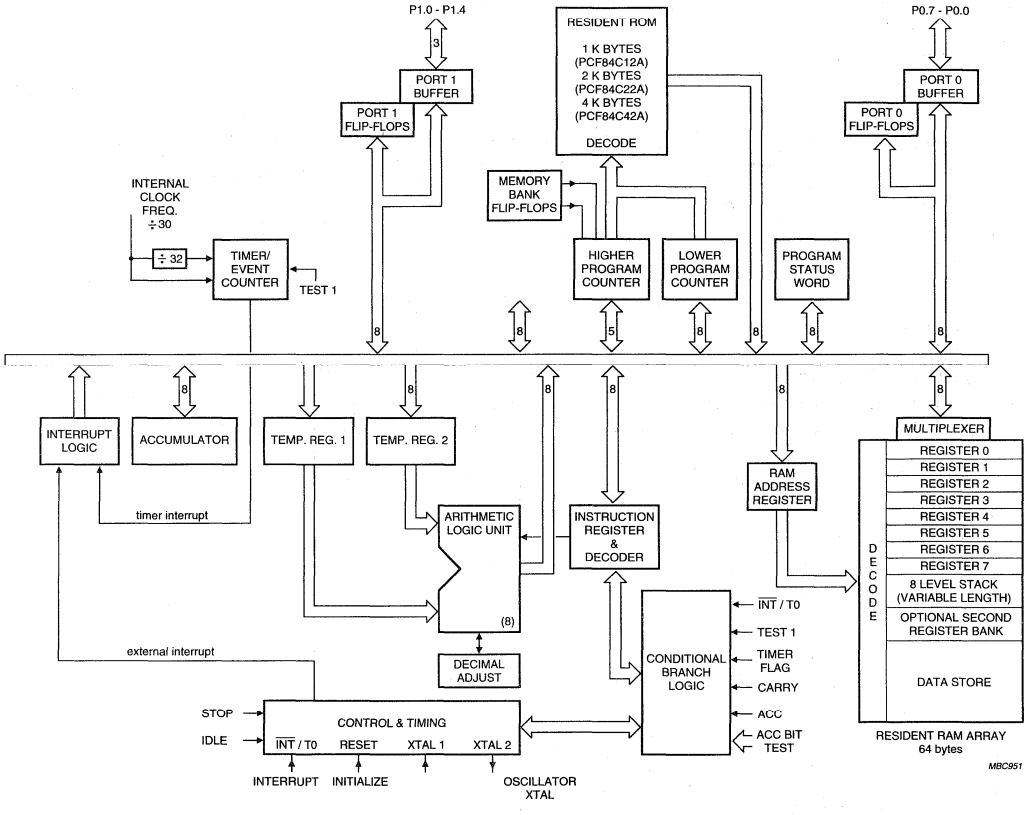


Fig.1 PCF84C12A/22A/42A Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 32 I/O LINES

DESCRIPTION

The PCF84C85 microcontroller is manufactured in CMOS, and is designed to be an efficient controller as well as an arithmetic processor. The instruction set is based on that of the MAB8048 and is software compatible with the 84CXXX family. The PCF84C85 has two additional derivative ports and the microcontroller has bit handling abilities and facilities for both binary and BCD arithmetic.

For detailed information see the 84CXXX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL or mini-pack package
- 8 K ROM
- 256 RAM bytes
- 32 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for two-line serial data transfer
  (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C

PACKAGE OUTLINES

PCF84C85P: 40-lead DIL; plastic (SOT129).
PCF84C85T: 40-lead; mini-pack (VSO40; SOT158A).

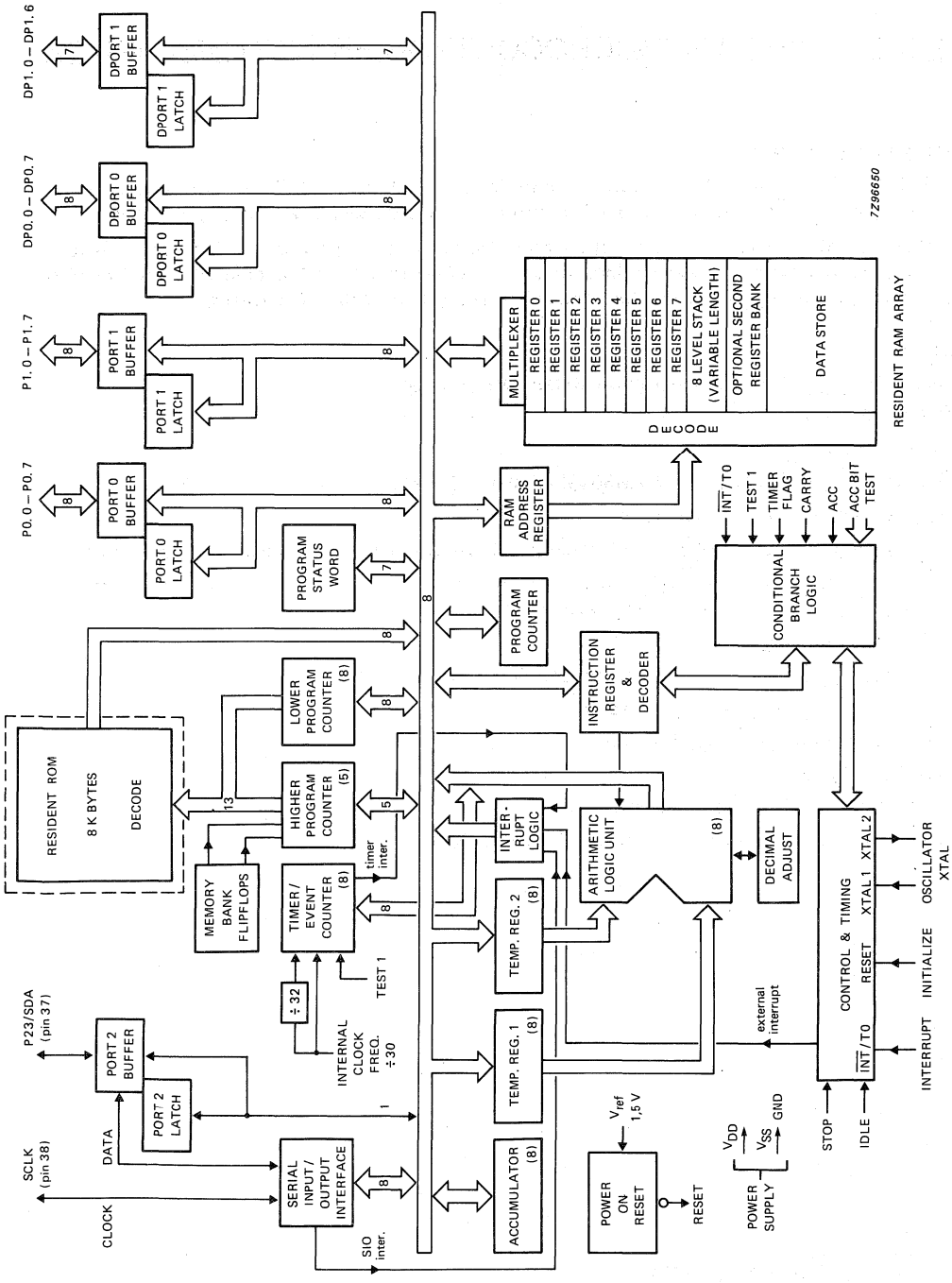


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The PCF84C230 is a single-chip 8-bit microcontroller manufactured in CMOS technology, and is a member of the 84CXXX family. For detailed information see the 84CXXX family specification.

The PCF84C230 provides 12 general purpose quasi-bidirectional I/O port lines, a line that is directly testable (T1), one external interrupt line, and an LCD driver for up to 64 graphic elements. The IC is mask-programmable and is designed for control in small systems with LCD displays.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead DIL package
- 2 K ROM bytes
- 64 RAM bytes
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 12 quasi-bidirectional I/O port lines
- Configuration of I/O lines can be individually selected by mask (pull-up, open drain, push-pull)
- LCD drive circuit with 16 segment drivers and selectable backplane drive configuration: static or 2/3/4 multiplex, to drive up to 64 graphic elements
- LCD possible during STOP mode
- Single-level vectored interrupts: external and timer/event counter
- Power-on reset and low voltage detector
- Single supply voltage from 2.5 V to 5.5 V
- STOP and IDLE modes
- Clock frequency 100 kHz to 10 MHz
- Operating ambient temperature range: −40 to + 85 °C

PACKAGE OUTLINES

40-lead DIL; plastic (SOT129).
40-lead mini-pack; plastic (VS040; SOT158A).

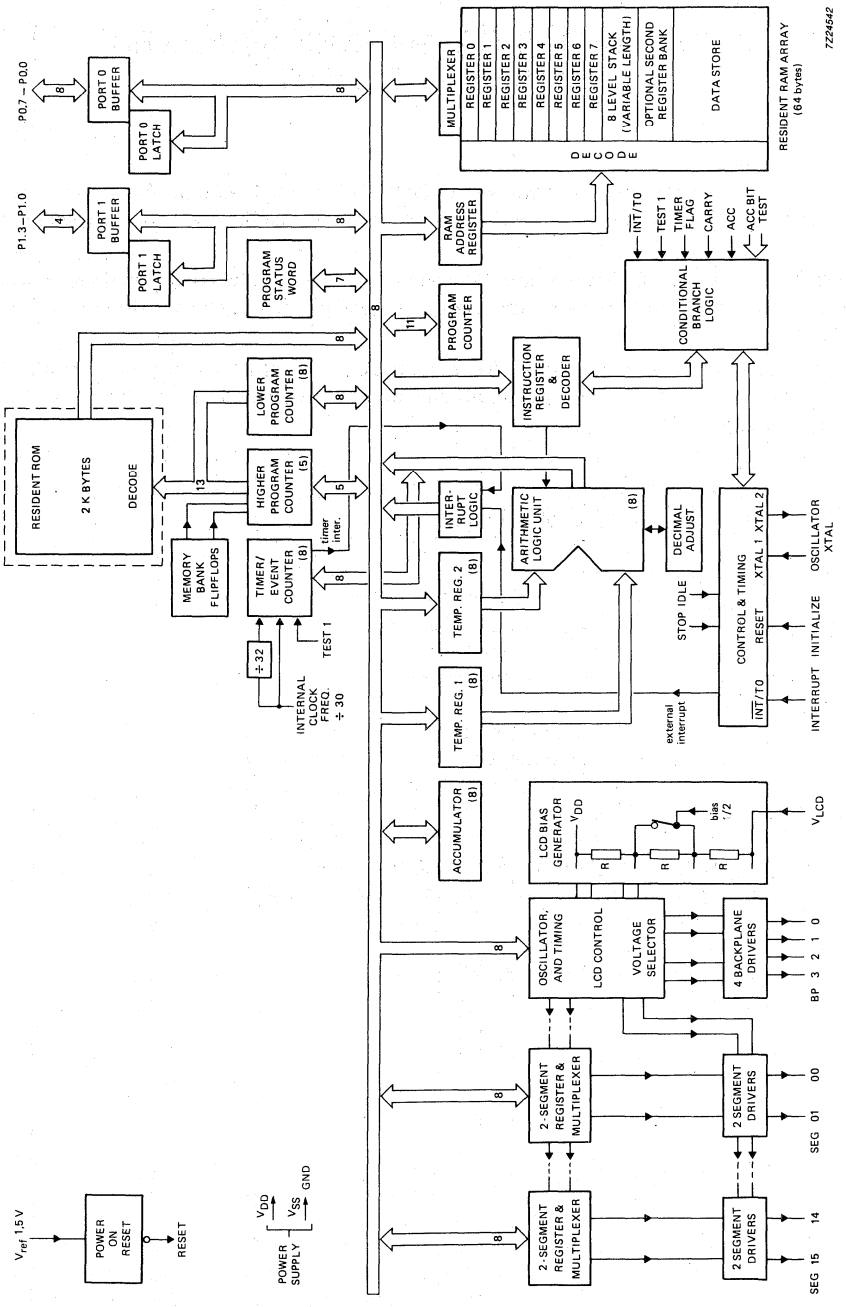


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVER

DESCRIPTION

The PCF84C430 microcontroller is a derivative of the 84CXXX family of microcontrollers and is manufactured in CMOS technology. For detailed information see the 84CXXX family specification.

The PCF84C430 contains a PCF84CXX core CPU and is completely software compatible. In addition, the PCF84C430 contains an LCD driver supporting four back planes and a maximum driving capacity of up to 96 segments.

The PCF84C430 has 16 quasi-bidirectional I/O port lines, plus a derivative 8-bit port, a serial I/O interface, a single-level vectored interrupt circuit, an 8-bit timer/event counter and on-board clock oscillator and clock circuits.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 64-lead QFP package
- 4 K ROM bytes
- 128 RAM bytes
- On-chip LCD driver with 24 outputs (max. 96 segments)
- LCD multiplexing rates at 1:1 (static), 1:2, 1:3 and 1:4
- Low-power oscillator for LCD driver during STOP mode
- 25 quasi-bidirectional I/O port lines are configured as two 8-bit ports, a 1-bit port (shared with SDA) and an 8-bit derivative port
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C-bus hardware interface for serial data transfer on two separate lines
- 8-bit programmable timer/event counter
- Clock frequency 100 kHz to 10 MHz
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- Single supply voltage from 2,5 V to 5,5 V ($V_{SS} \leqslant V_{LCD} < V_{DD}$)
- STOP and IDLE mode
- Power-on-reset circuit
- Operating temperature range: −40 to + 85 °C

PACKAGE OUTLINE

PCF84C430H: 64-lead quad flat-pack; plastic (SOT208).

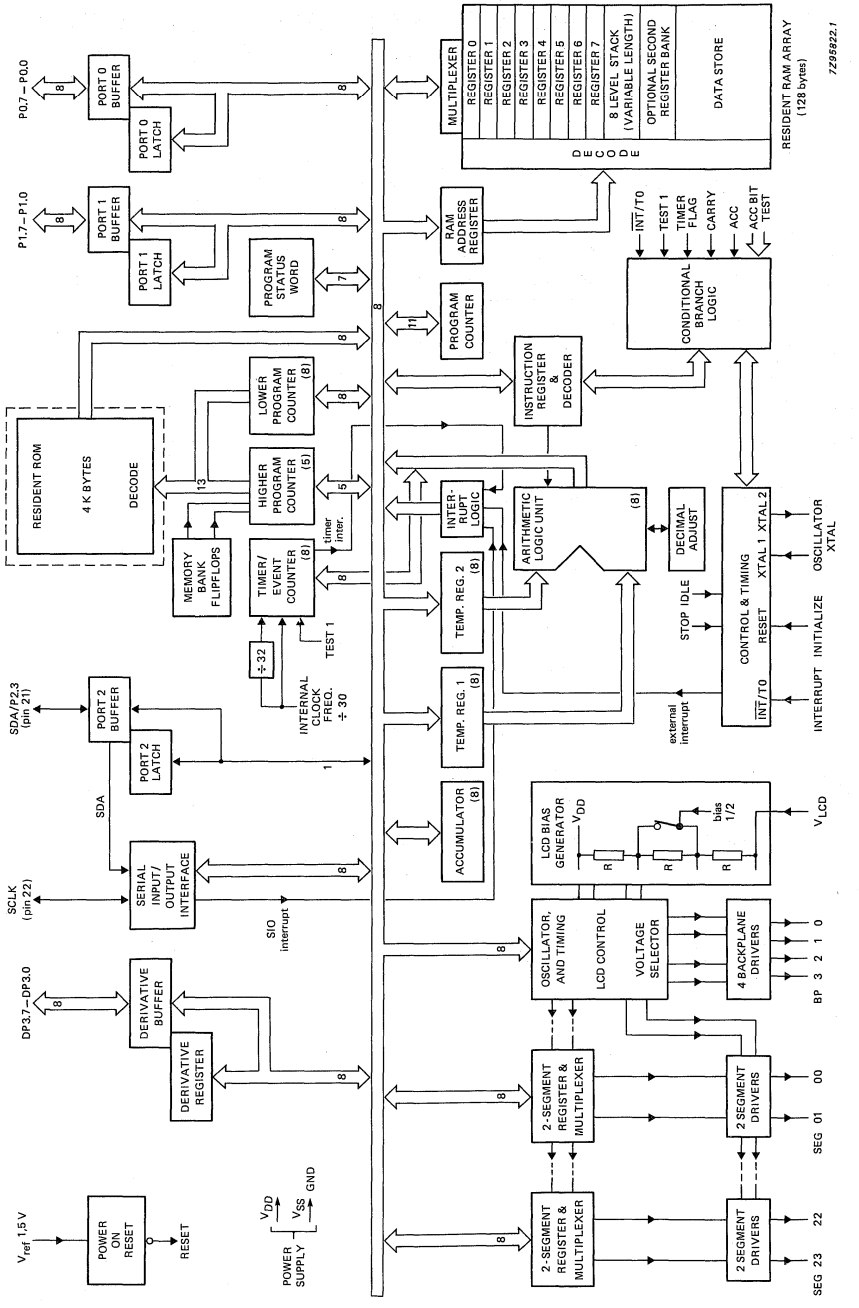


Fig. 1 Block diagram; PCF84C430.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH LCD DRIVERS, DERIVATIVE PORT, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C633A is a microcontroller with 20 on-chip liquid crystal display (LCD) outputs. These can be configured for one to four backplanes and 19 to 16 segment lines, yielding a maximum of 64 display elements. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C633A includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding real-time applications.

IMPORTANT

This data sheet details the specific properties of the PCF84C633A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 56-lead package
- 6 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB 8048) all of 1 or 2 cycles
- 28 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupts; external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- 20 LCD output configurable for one to four backplanes and 19 to 16 segment lines
- Drive for up to 64 display elements
- Display memory bank switching in static and duplex drive modes
- 19 of the LCD outputs may serve as additional low-drive logic outputs with optional level-shift
- Stop and idle modes
- Logic supply V_{DD}; 2.5 V to 5.5 V
- Independent LCD supply V_{DDLC}; 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to 85 °C
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINE

PCF84C633AT: 56-lead mini-pack; plastic (VSO56; SOT190)

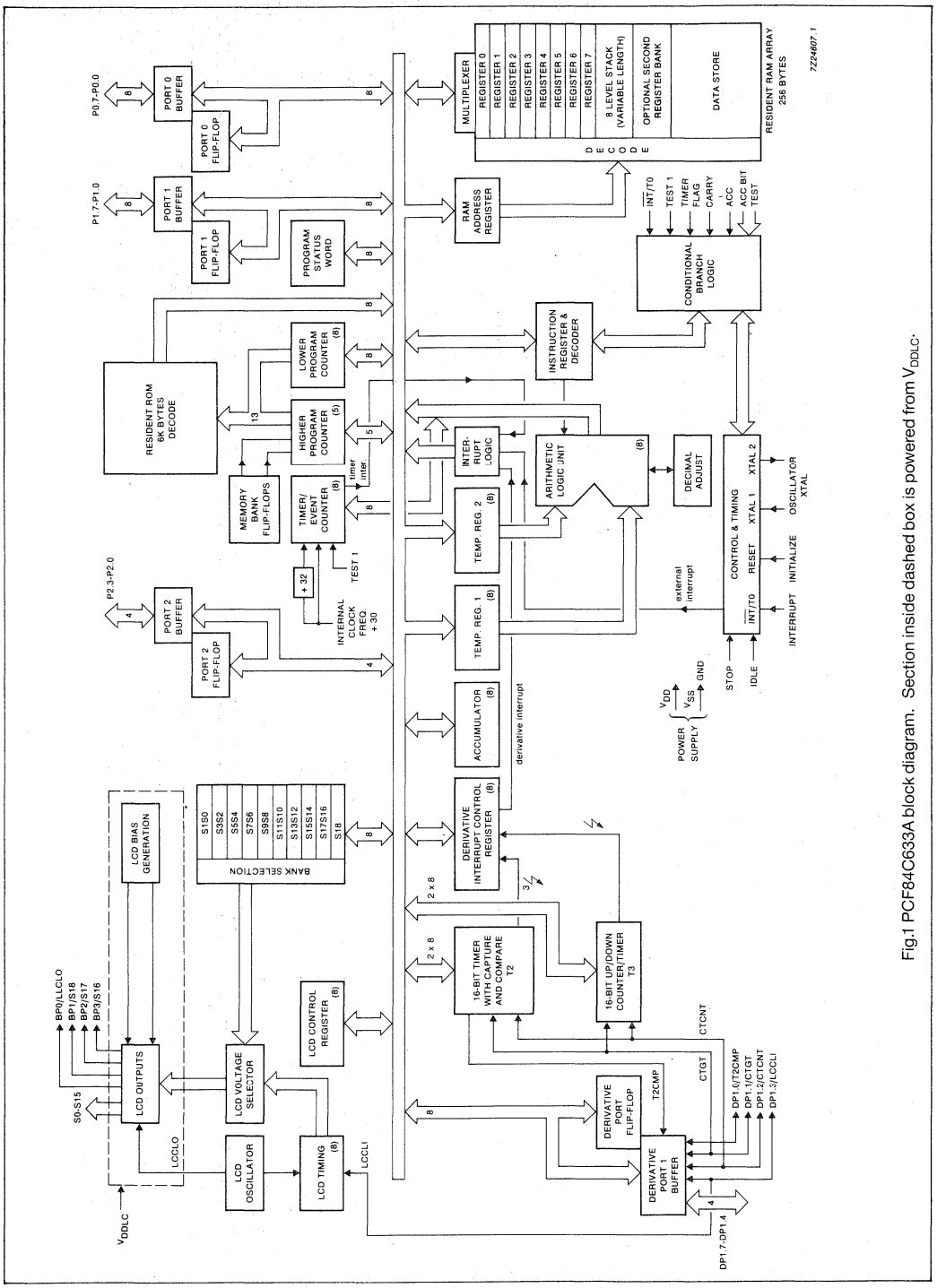


Fig.1 PCF84C633A block diagram. Section inside dashed box is powered from V_{DDLC}.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC14 OR DATASHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER WITH DERIVATIVE PORTS, TIMER/CAPTURE AND TIMER/COUNTER

DESCRIPTION

The PCF84C853A is a microcontroller with 33 quasi-bidirectional I/O port lines. In addition to the shared features of the PCF84CXX family of microcontrollers, the PCF84C853 includes a 16-bit timer with capture and compare registers, a 16-bit up/down counter/timer and two filtered control inputs. Together with additional derivative port lines, these powerful extensions make the device attractive for demanding realtime applications.

FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 40-lead package
- 8 K bytes ROM
- 256 bytes RAM
- Over 80 instructions (based on MAB8048) all of 1 or 2 cycles
- 33 quasi-bidirectional I/O port lines
- 8-bit programmable timer/event counter
- 16-bit derivative timer with capture and compare registers (T2)
- 16-bit up/down counter/timer (T3)
- 2 filtered input lines coupled to T2 and T3
- 3 single-level vectored interrupt: external, 8-bit programmable timer/event counter, derivative (triggered by 4 events in T2 and T3)
- 2 test inputs of which one also serves as the external interrupt input
- Stop and Idle modes
- Supply range V_{DD}: 2.5 V to 5.5 V
- Clock frequency: 1 MHz to 16 MHz
- Operating temperature range: −40 °C to + 85 °C
- Manufactured in silicon gate CMOS process

IMPORTANT

This data sheet details the specific properties of the PCF84C853A. The shared characteristics of the 84CXXX family of microcontrollers are described in 84CXXX family specification, which should be read in conjunction with this publication.

PACKAGE OUTLINES

PCF84C853AP: 40-lead DIL; plastic (SOT129)
PCF84C853AT: 40-lead mini-pack; plastic (VSO40; SOT158A)

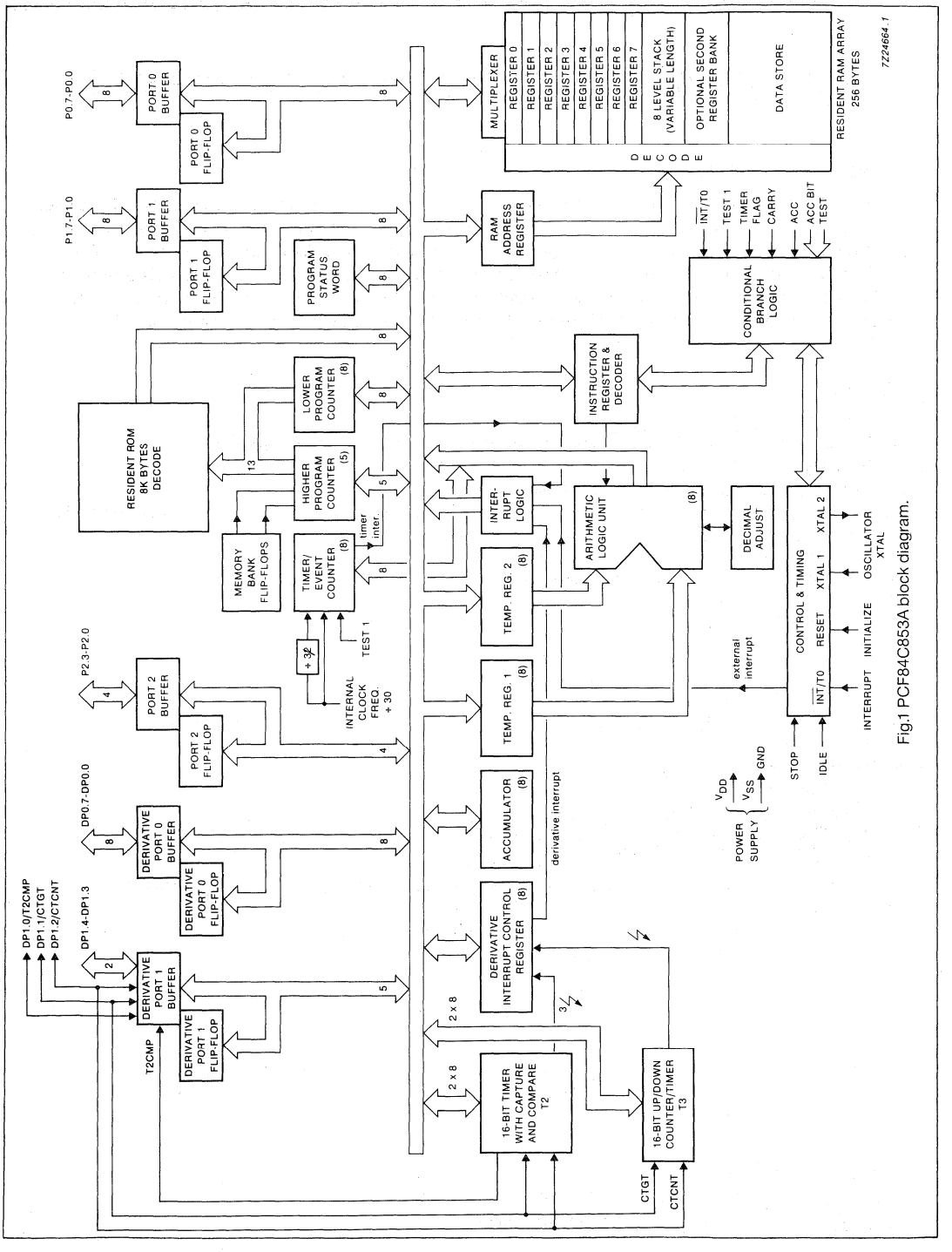


Fig.1 PCF84C853A block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

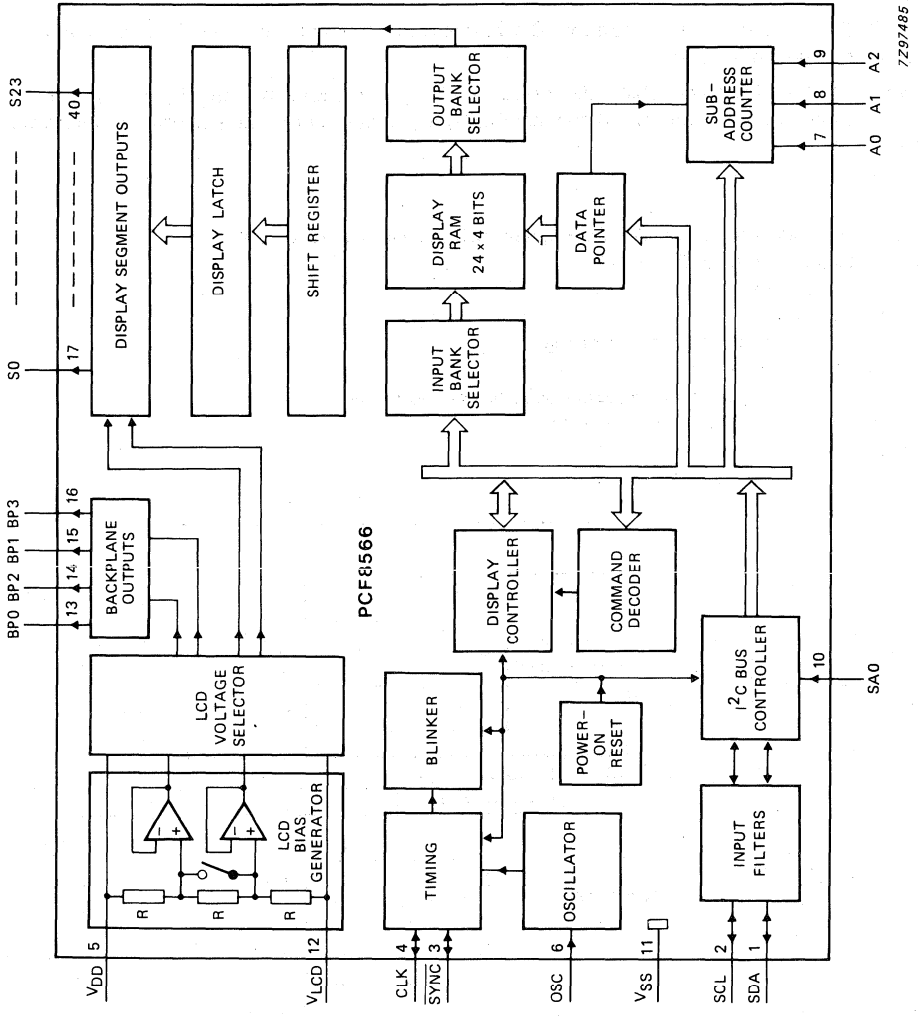


Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DIRECT MODE DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8567C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing and hardware subaddressing..

Features

- Direct drive mode with up to 32 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display

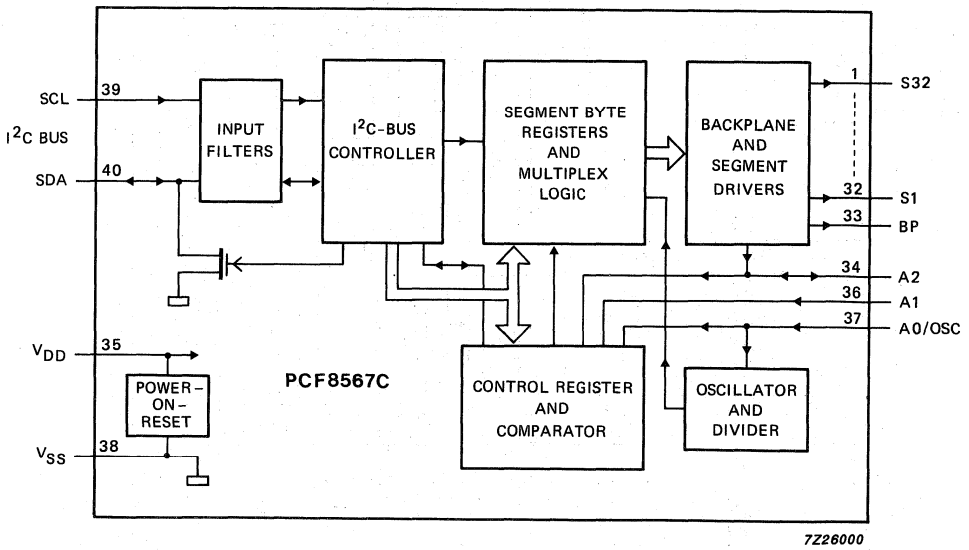


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8567CP: 40-lead DIL; plastic (SOT129).
PCF8567CT: 40-lead mini-pack; plastic (VSO40; SOT158A).

LCD row driver for dot matrix displays

PCF8568

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

FEATURES

- Single chip LCD row driver with 16 outputs
- Low power consumption
- Selectable multiplex rate 1:8, 1:16, 1:24, 1:32
- Cascadable to 1:24 or 1:32 multiplex rates
- Internally generated intermediate LCD bias voltages
- LCD column bias voltages available at pins VO3 and VO4
- Minimizes display system power requirements
- On-chip oscillator, requires only one external resistor
- Power-on reset blanks display
- Logic voltage range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9.0 V
- I²C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring
- Available in 28-lead plastic DIL or space saving mini-pack
- Compatible with chip-on-glass technology.

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- General instrumentation
- Consumer products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	+2.5	-	+6.0	V
V_{LCD}	LCD supply voltage range voltage	V_{DD} −9	-	V_{DD} −3.5	V
I_{DD2}	supply current with internal clock (R_{OSC} = 330 kΩ)	-	67	150	µA
T_{amb}	operating ambient temperature range	−40	-	+85	°C

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8568P	28	DIL	plastic	SOT117
PCF8568T	28	SO28	plastic	SOT136A
PCF8568U/7	(28 pads)	die: bumped chip on tape	-	-

GENERAL DESCRIPTION

The PCF8568 is a low power LCD row driver, designed to drive dot matrix graphic displays with multiplex rates of 1:8 or 1:16. The device has 16 row outputs. Two devices may be cascaded to drive displays with multiplex rates of 1:24 or 1:32. The PCF8568 is optimised for use with the PCF8569 and PCF8579 LCD dot matrix column drivers. Intermediate LCD bias voltages are internally generated. LCD column bias voltages are available at pins VO3 and VO4 for connection to the column drivers. The PCF8568 is compatible with most microcontrollers and communicates via a two- line bidirectional bus (I²C).

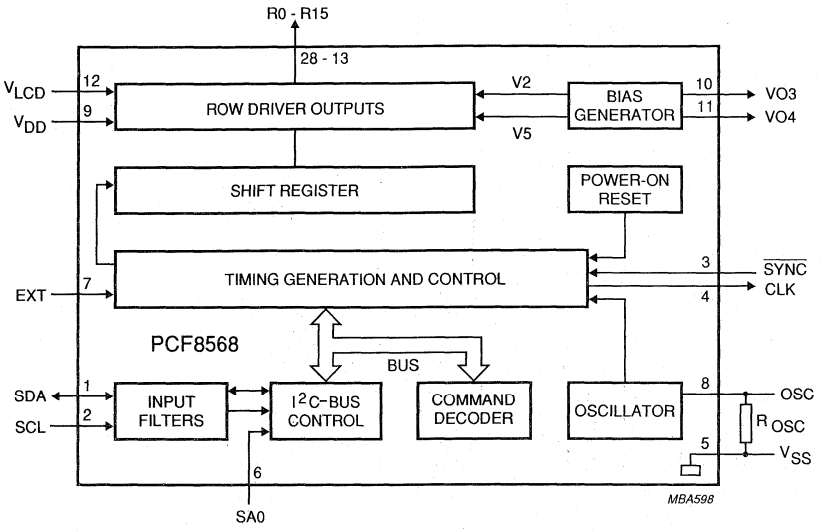


Fig.1 Block diagram.

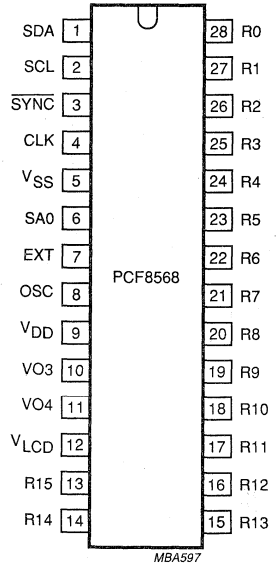


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDA	1	I²C-bus serial data line
SCL	2	I²C-bus serial clock line
$\overline{SYNC}$	3	cascade synchronization input/output
CLK	4	clock output
V_{SS}	5	ground (logic)
SA0	6	I²C-bus slave address input (bit 0)
EXT	7	external clock select pin
OSC	8	oscillator or external clock input pin
V_{DD}	9	positive supply voltage
VO3	10	LCD bias voltage output (V3)
VO4	11	LCD bias voltage output (V4)
V_{LCD}	12	LCD supply voltage
R15 to R0	13 to 28	LCD row driver outputs

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

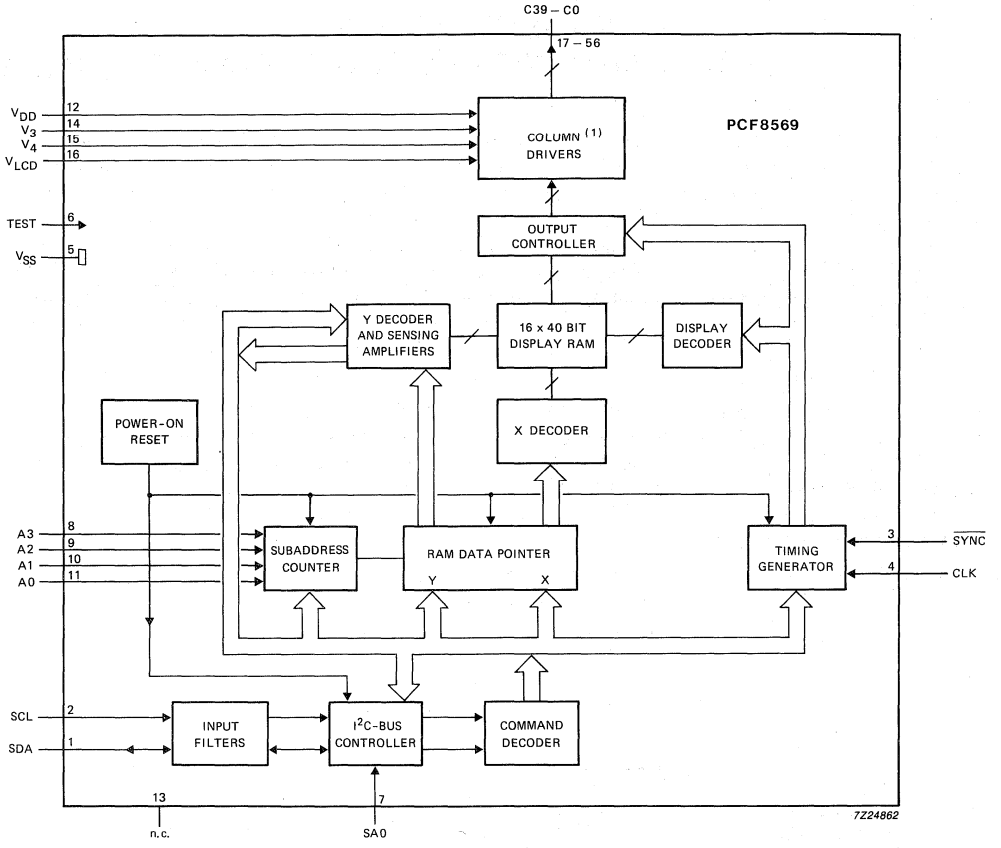
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

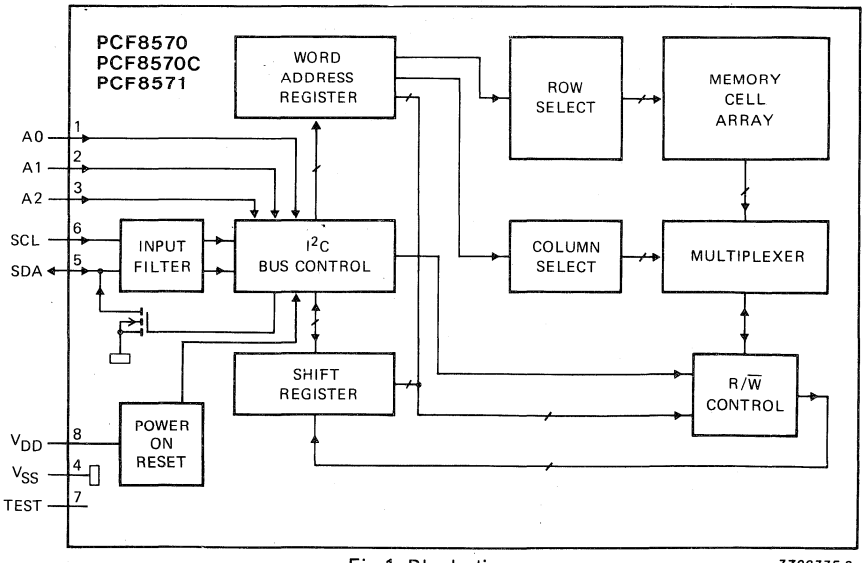


Fig.1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

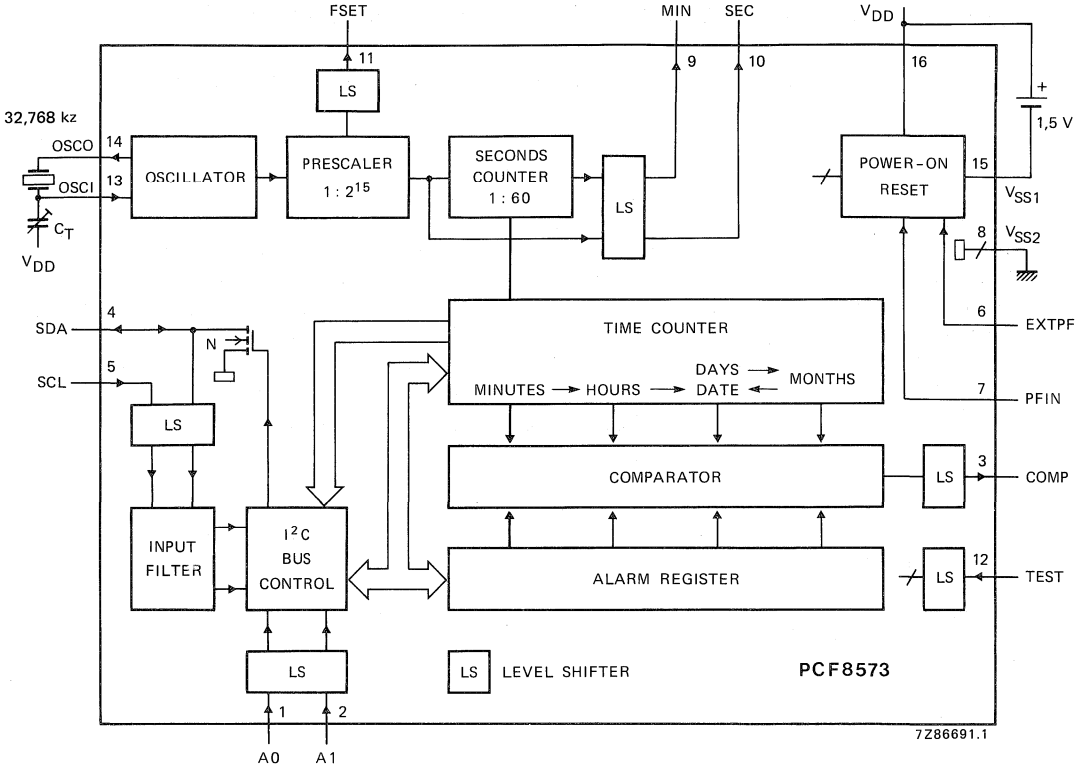


Fig.1 Block diagram.

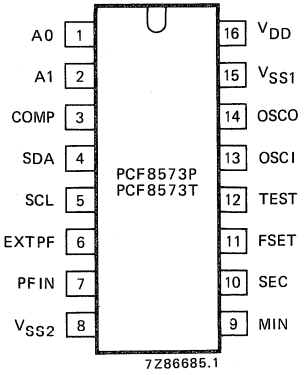


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage 2.5 V to 6 V
- Low stand-by current consumption max. 10 μA.
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

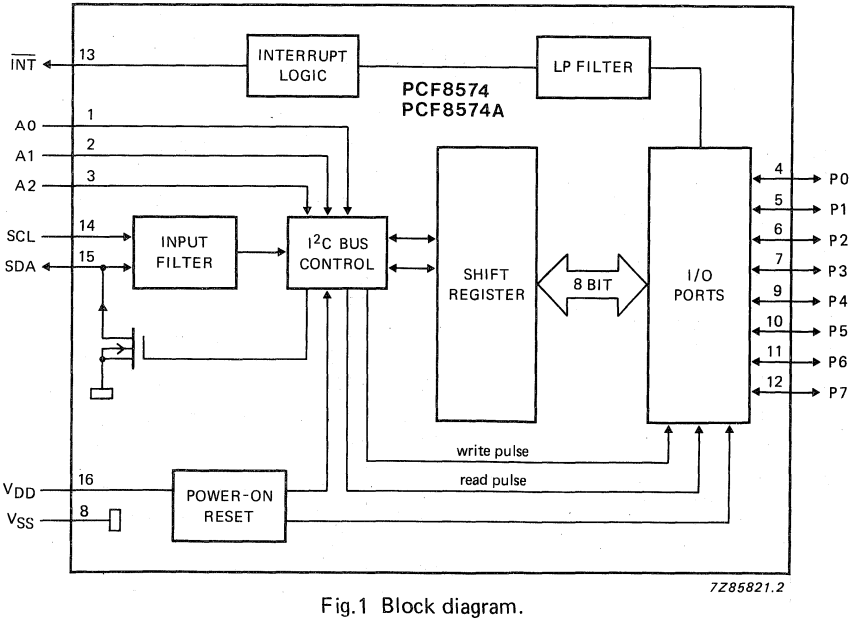


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

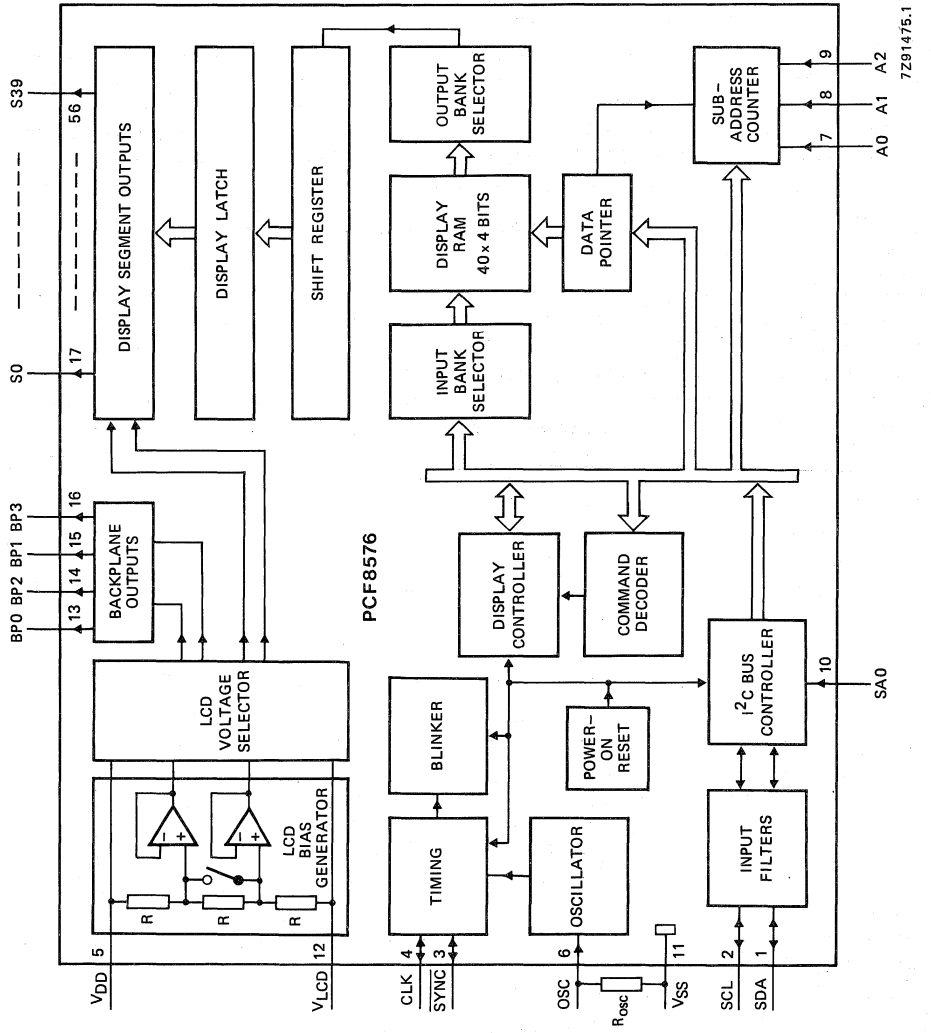


Fig.1 Block diagram; VSO56; SOT190.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

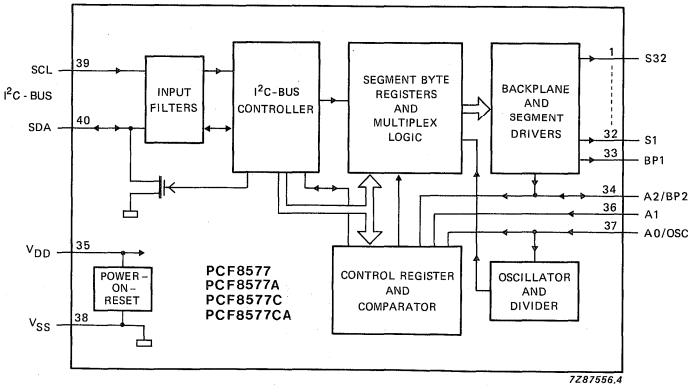


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP	:	40-lead DIL; plastic (SOT129).
PCF8577CP, PCF8577CAP	:	
PCF8577T, PCF8577AT	:	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577CT, PCF8577CAT	:	
PCF8577T, PCF8577AT	:	in blister tape.
PCF8577CT, PCF8577CAT	:	
PCF8577U/5	:	wafer unsawn.
PCF8577CU/5	:	
PCF8577U/10	:	chip on film-frame-carrier (FFC).
PCF8577CU/10	:	

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

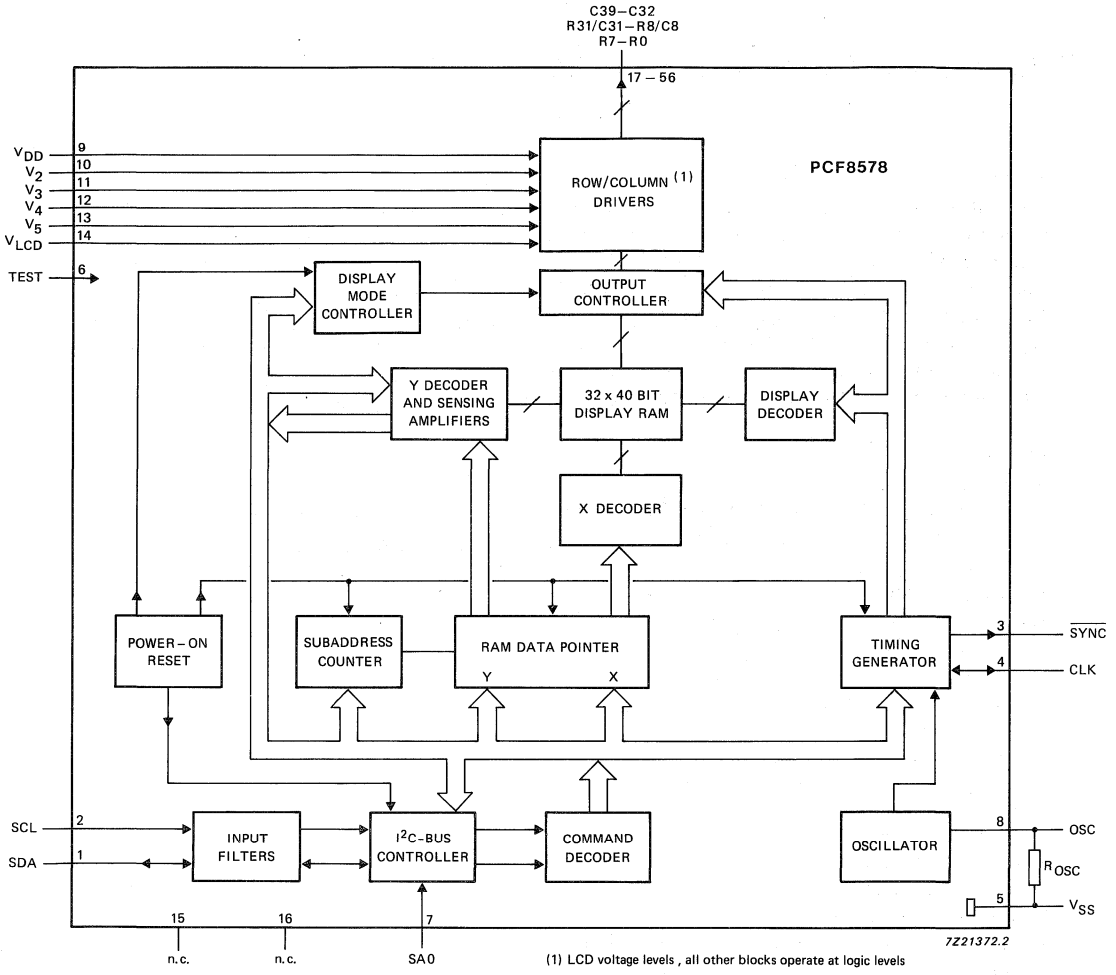


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

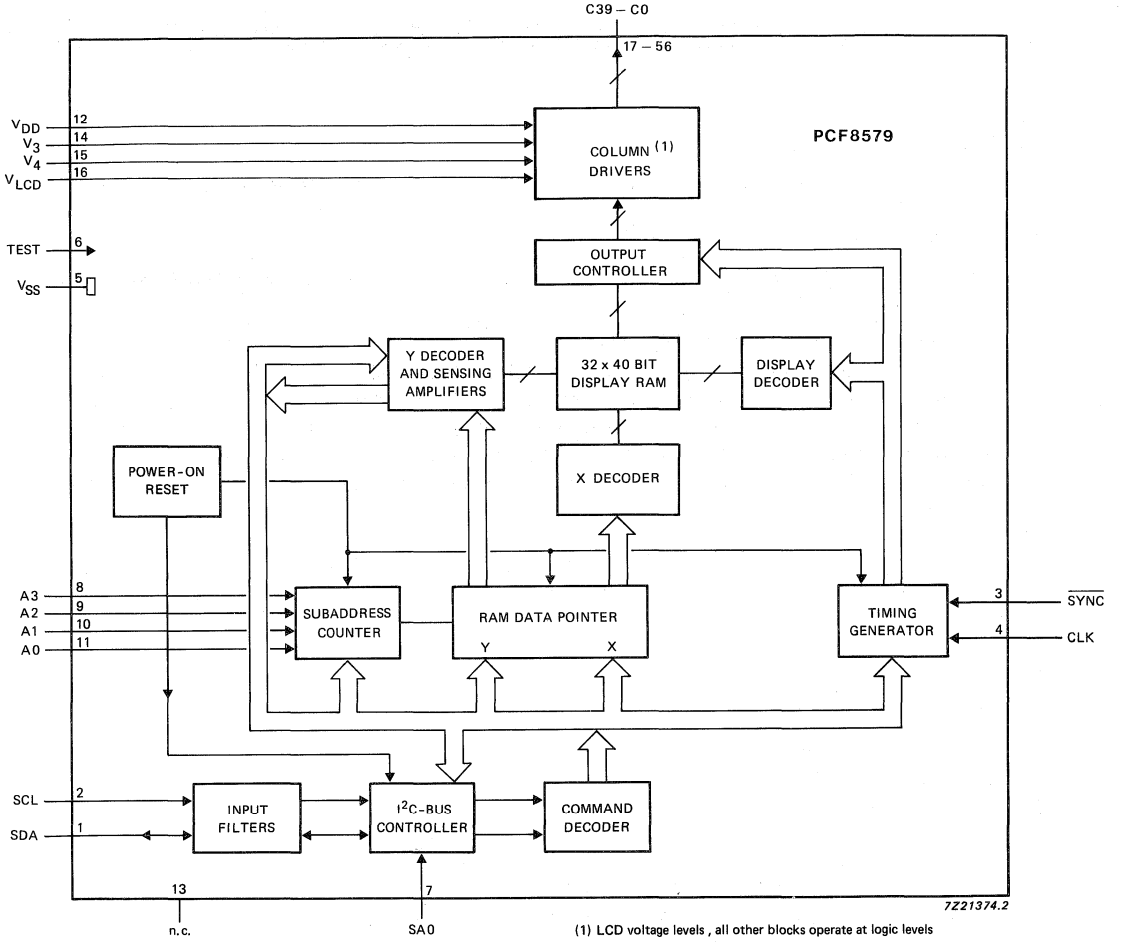


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

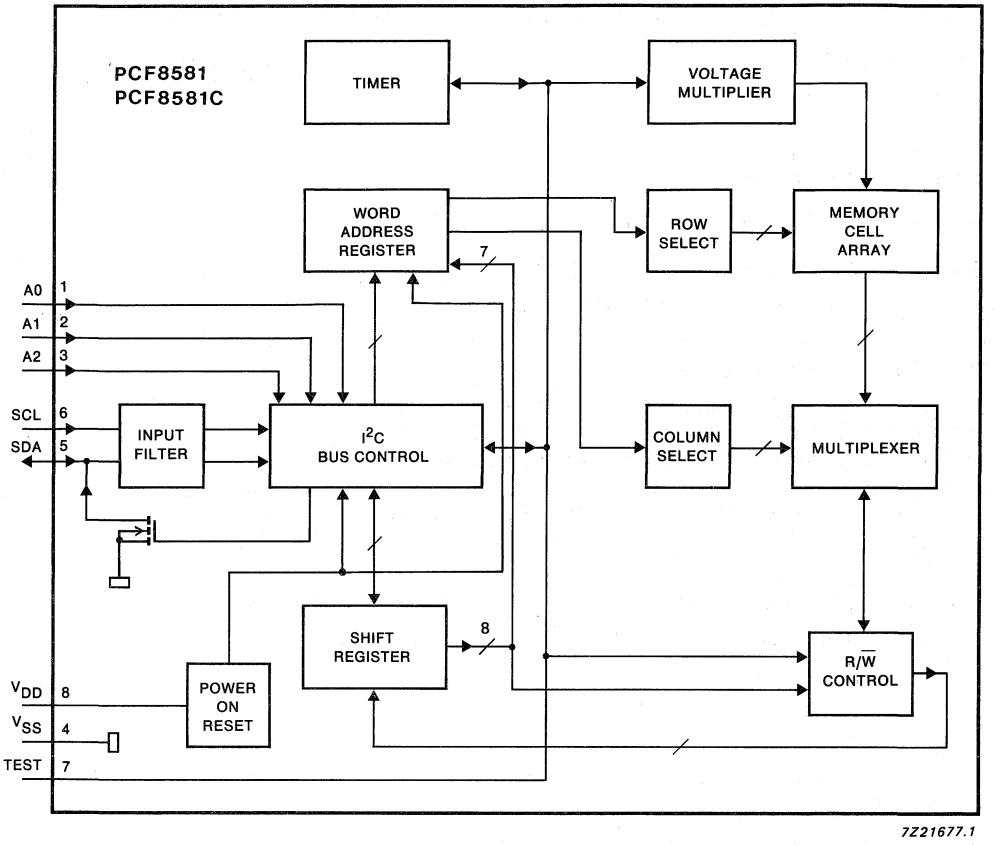


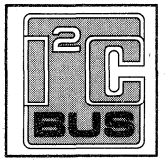
Fig.1 Block diagram.

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

FEATURES



- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V f_{scl} = 0 Hz; V_{DD} = 1 V	- -	50 10	µA µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

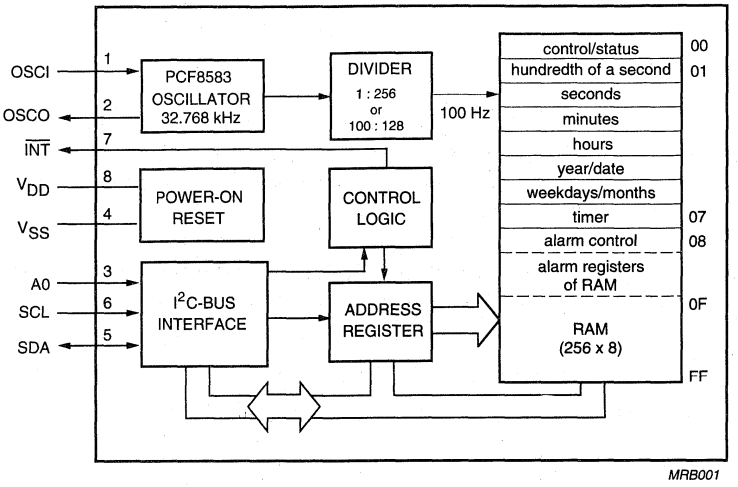


Fig.1 Block diagram.

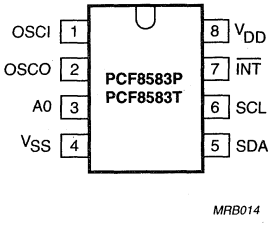


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

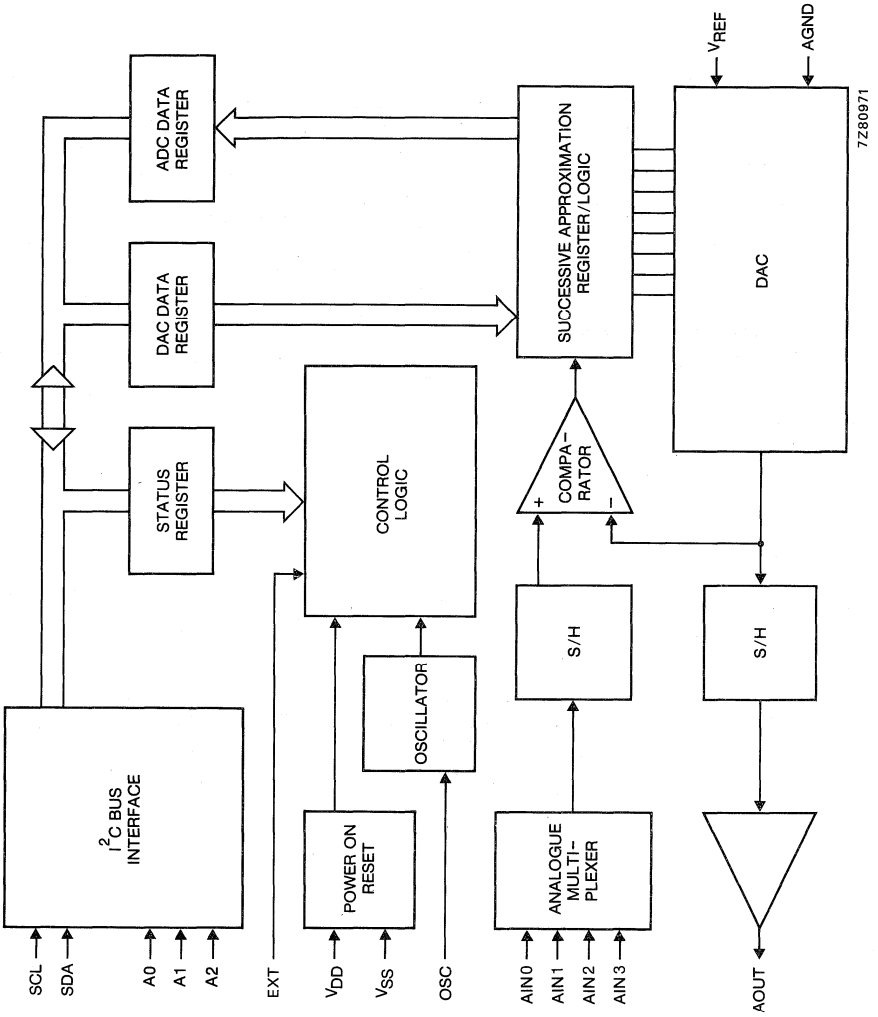


Fig. 1 Block diagram.

256 x 8-BIT CMOS EEPROMS with I²C-bus interface

PCx8582x-2 Family

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Low power CMOS; maximum active current 2 mA, maximum standby current 10 µA
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, PCF8572 and PCF8581
- Write operations

  byte write mode

  8-byte page write mode (minimizes total write time per byte)
- Read operations

  sequential read and random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- High reliability by using a redundant storage code
- Endurance 100 k; T_{amb} = +85 °C

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories. By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCx8582x-2 devices can be connected to the I²C-bus.
Chip select is accomplished by the three address inputs.

Timing of the Erase/Write cycle is achieved internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

An option exists for using an external clock for timing the length of an Erase/Write cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive suppy voltage		2.5	–	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA

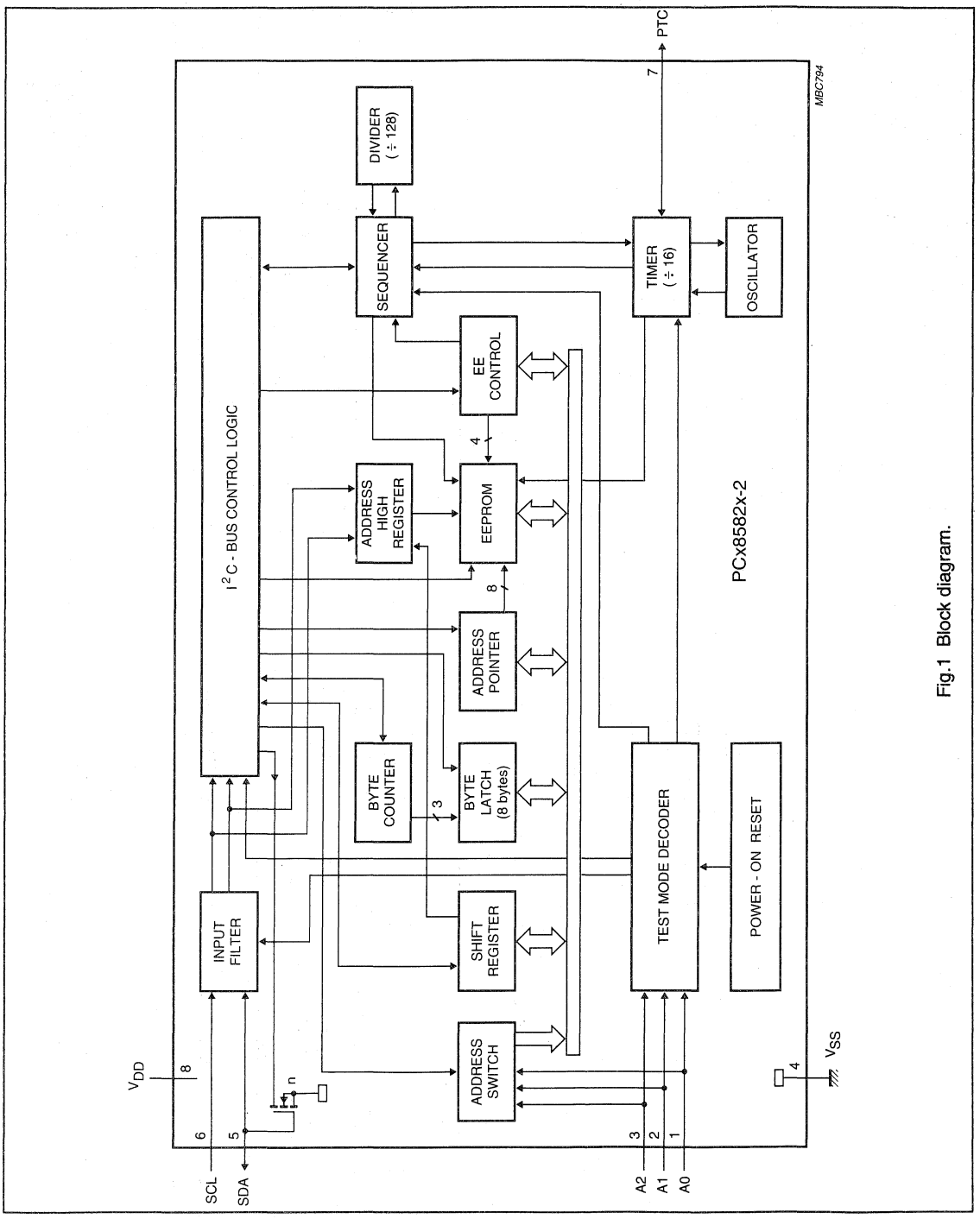


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8582x-2P	8	DIL	plastic	SOT97
PCx8582x-2T	8	SO8	plastic	SOT96A

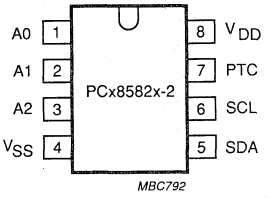


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data
SCL	6	serial clock
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		–	1	mA
I_O	output current		–	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582C-2; PCF8582E-2		−40	+85	°C
	PCD8582D-2		−25	+70	°C
	PCA8582F-2		−40	+125	°C

CHARACTERISTICS

PCF8582C-2; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCD8582D-2; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C
PCF8582E-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCA8582F-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage					
	PCF8582C-2		2.5	–	6.0	V
	PCD8582D-2		3.0	–	6.0	V
	PCF8582E-2; PCA8582F-2		4.5	–	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	200	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
	PCF8582E-2	$V_{DD\ max}$	–	–	2.0	mA
	PCF8582F-2	$V_{DD\ max}$	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	10	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	10	µA
PTC input						
V_{IH}	HIGH level input voltage		0.9 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.3 V_{DD}	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	±1	µA
f_{SCL}	clock frequency		0	–	100	kHz
C_i	input capacitance	$V_I = V_{SS}$	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA input/output						
V_{IL}	LOW level input voltage		−0.8	−	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	−	V_{DD}+0.8	V
V_{OL}	LOW level output voltage	I_{OH} = 3 mA; $V_{DD\ min}$	−	−	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	−	−	1	µA
C_i	input capacitance	$V_I = V_{SS}$	−	−	7	pF
Data retention time						
t_S	data retention time	T_{amb} = +55 °C	10	−	−	yrs

WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{DD} or V_{SS}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		−	7	−	ms
	external clock		4	−	10	ms
$N_{E/W}$	ERASE/WRITE cycles per byte					
	PCF8582C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	−	−	500 000	
	PCD8582D-2	T_{amb} = −25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	−	−	10 000	
		T_{amb} = −25 to +40 °C; $t_{E/W}$ = 5 ms	−	−	100 000	
	PCF8582E-2	T_{amb} = −40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	10 000	
		T_{amb} = +22 °C; $t_{E/W}$ = 5 ms	−	−	100 000	
	PCA8582F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	−	−	50 000	
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	−	−	500 000	

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes,
transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCx8582x-2 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCx8582x-2 this is fixed as 1010.

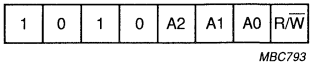


Fig.3 Slave address.

The next three significant bits address a particular device. A system could have up to eight PCx8582x-2 devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.
Address inputs must be connected either to V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCx8582x-2 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCx8582x-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte.
During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCx8582x-2 is capable of a eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCx8582x-2 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

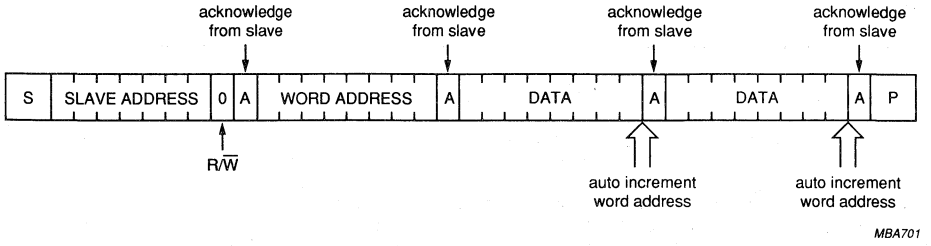


Fig.4 Auto increment memory word address; two byte write.

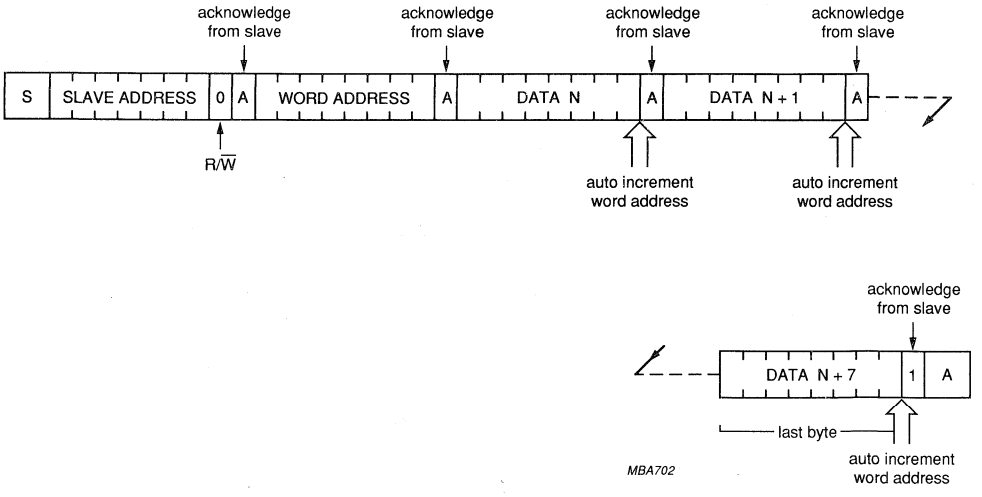


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

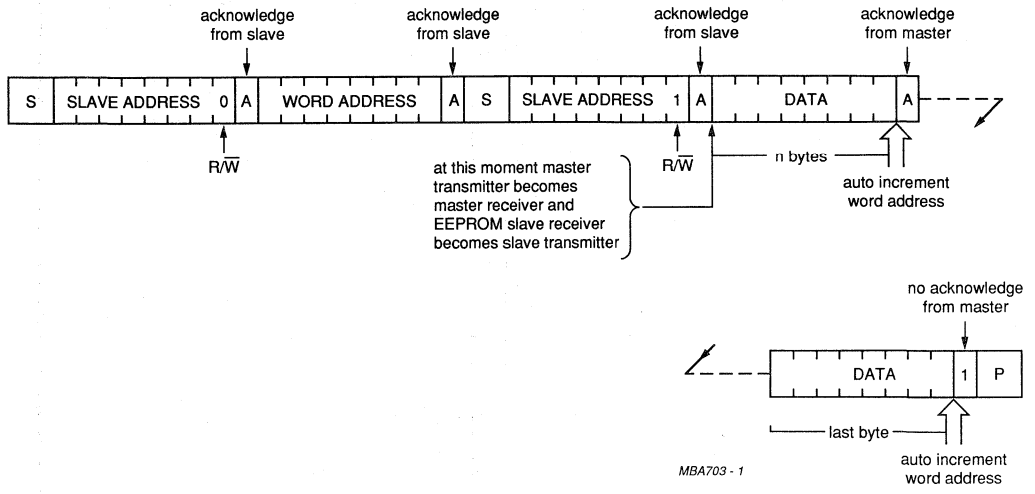


Fig.6 Master reads PCx8582x-2 slave after setting word address (WRITE word address; READ data).

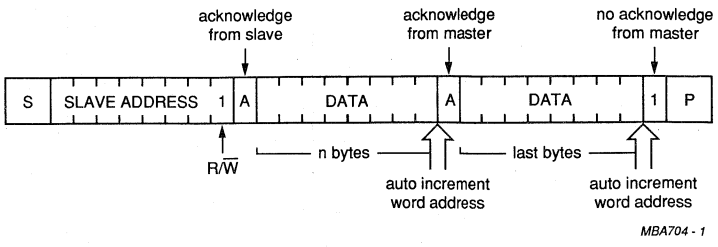


Fig.7 Master reads PCx8582x-2 immediately after first byte (READ mode).

I²C-BUS TIMING

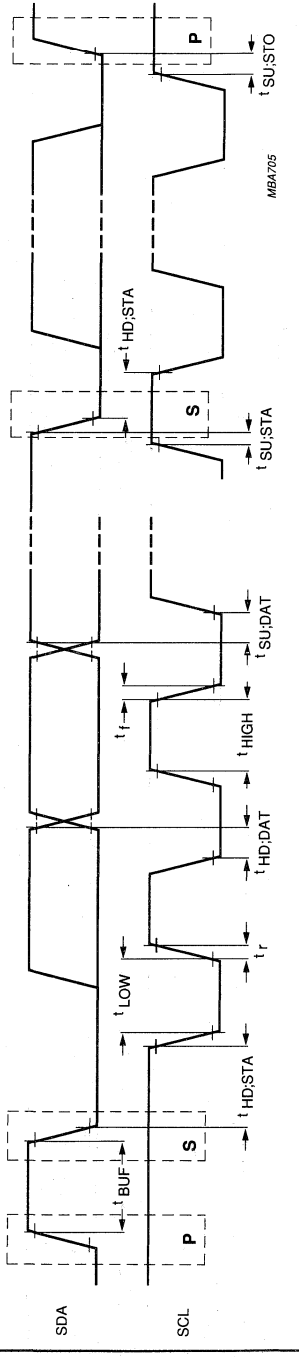


Fig.8 Timing requirements for the I²C-bus.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8569 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8 or 1:16. The device has 40 outputs and can drive 16 x 40 dots in a 16 row multiplexed LCD. Up to 16 PCF8569s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8568/78/79 family of LCD row/column drivers. Together the PCF8568, PCF8578 and PCF8569 form a general LCD dot matrix driver chip set, capable of driving displays of up to 20 480 dots. The PCF8569 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

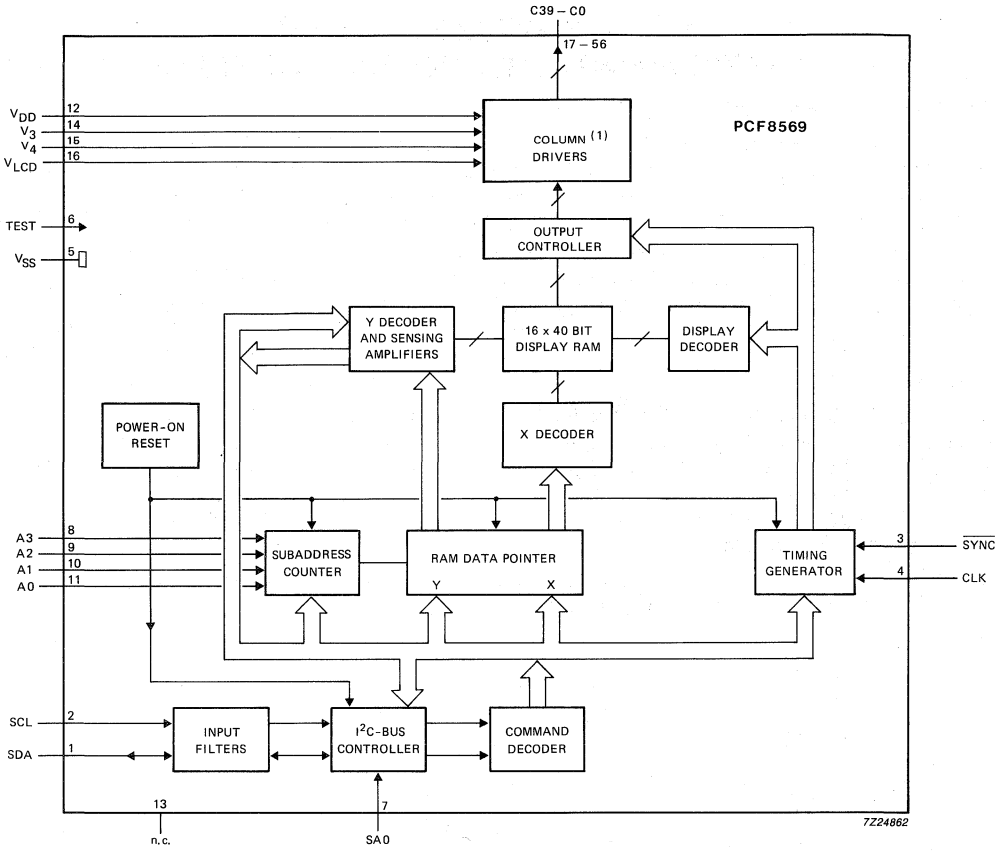
- LCD column driver
- Used in conjunction with the PCF8568 or PCF8578, this device forms part of a chip set capable of driving up to 20 480 dots.
- 40 column outputs
- Selectable multiplex rates; 1:8 or 1:16
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications
- 640-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack or 64-lead tab module

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8569T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8569V: 64-lead tape-automated-bonding (tab) module (SOT267).



(1) LCD voltage levels, all other blocks operate at logic levels.

Fig.1 Block diagram (pin numbers shown for VSO56; SOT190).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 X 8-BIT/256 X 8-BIT STATIC RAMS WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2.5 V to 6 V
- Low data retention voltage min. 1.0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

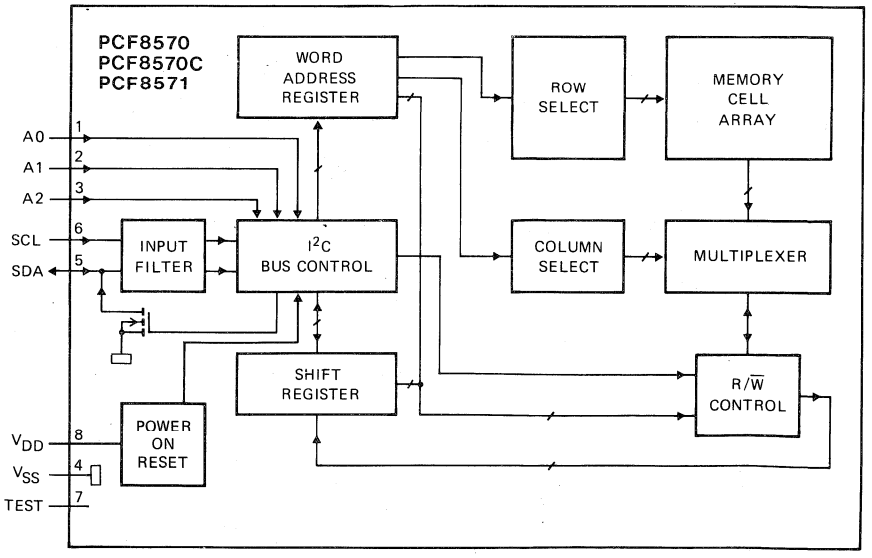


Fig.1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176C).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar with an I^2C-bus interface.
The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Information is transferred via a serial two-line bidirectional bus (I^2C). Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

Features

- Serial input/output I^2C-bus interface for minutes, hours, days and months
- Additionai pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32.768 kHz)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range					
clock (pin 16 to pin 15)	$V_{DD}-V_{SS1}$	1.1	–	6.0	V
I^2C interface (pin 16 to pin 8)	$V_{DD}-V_{SS2}$	2.5	–	6.0	V
Crystal oscillator frequency	f_{osc}	–	32.768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

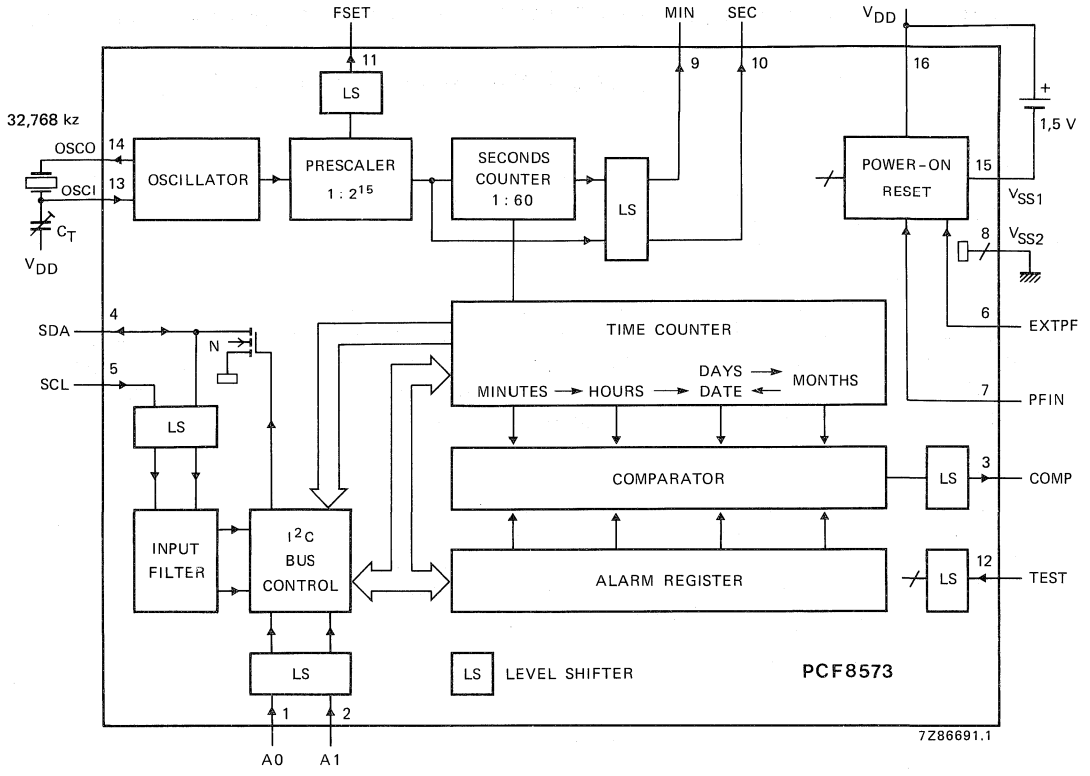


Fig.1 Block diagram.

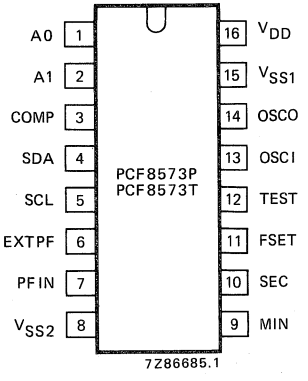


Fig.2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C-bus
5	SCL	serial clock line	I^2C-bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

REMOTE 8-BIT I/O EXPANDER FOR I²C-BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C-bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C-bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C-bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig.9.

Features

- Operating supply voltage — 2.5 V to 6 V
- Low stand-by current consumption — max. 10 μA.
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C-bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

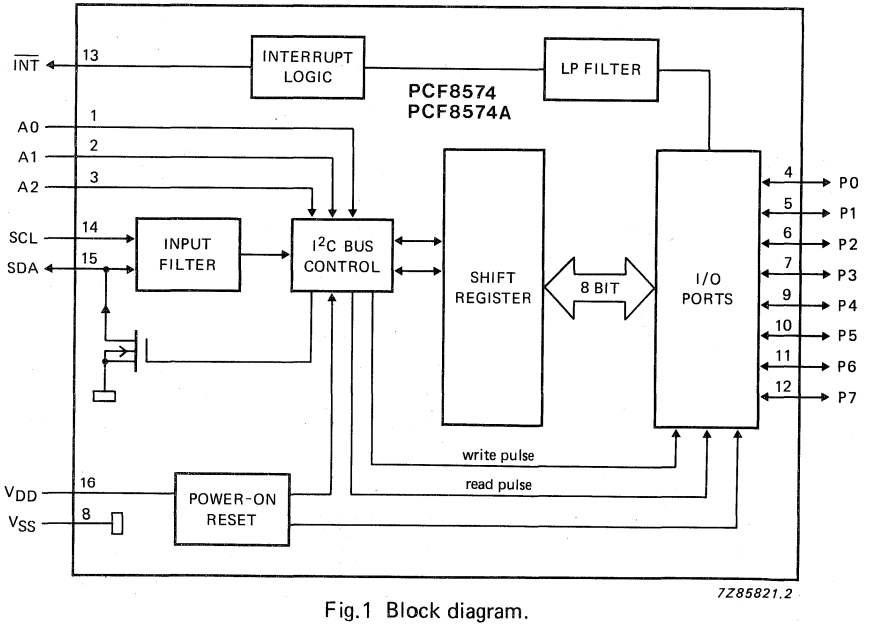


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24-segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO56) or 64-lead tape-automated-bonding (TAB) module (SOT267A)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray.
PCF8576U/10: chip-on-film frame carrier (FFC).
PCF8576V: 64-lead tape-automated-bonding module (SOT267A).

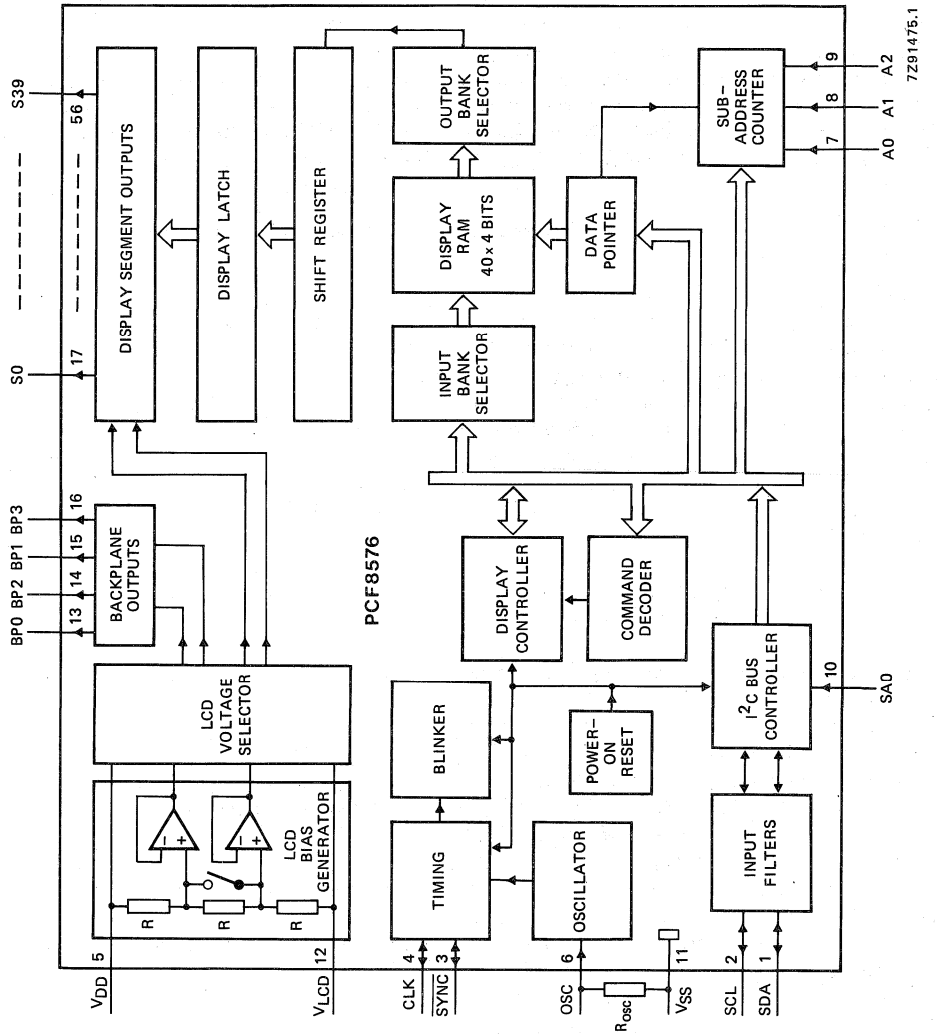


Fig.1 Block diagram; VSO56; SOT190.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD DIRECT / DUPLEX DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).
The PCF8577 and PCF8577C differ from the PCF8577A and PCF8577CA only in their slave addresses.
The PCF8577C/77CA is a low-voltage version of the PCF8577/77A.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Opering supply voltage:
  PCF8577/77A: 2.5 to 9 V
  PCF8577C/77CA: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A/CA)
- Power-on reset blanks display

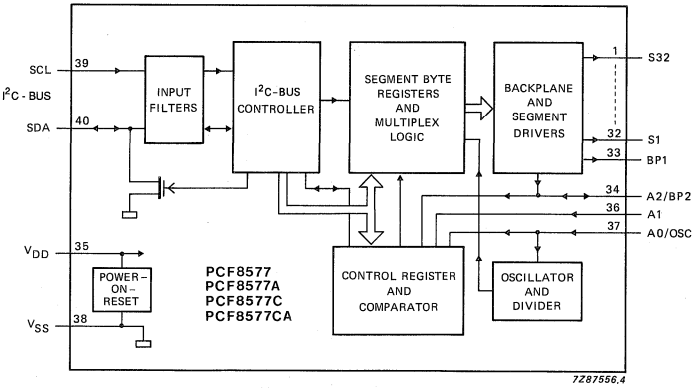


Fig.1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP PCF8577CP, PCF8577CAP	40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	40-lead mini-pack; plastic (VSO40; SOT158A).
PCF8577T, PCF8577AT PCF8577CT, PCF8577CAT	in blister tape.
PCF8577U/5 PCF8577CU/5	wafer unsawn.
PCF8577U/10 PCF8577CU/10	chip on film-frame-carrier (FFC).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40,960 dots possible)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578V: 64-lead tape-automated-bonding module (SOT267A).
PCF8578U: chip with bumps on-tape.

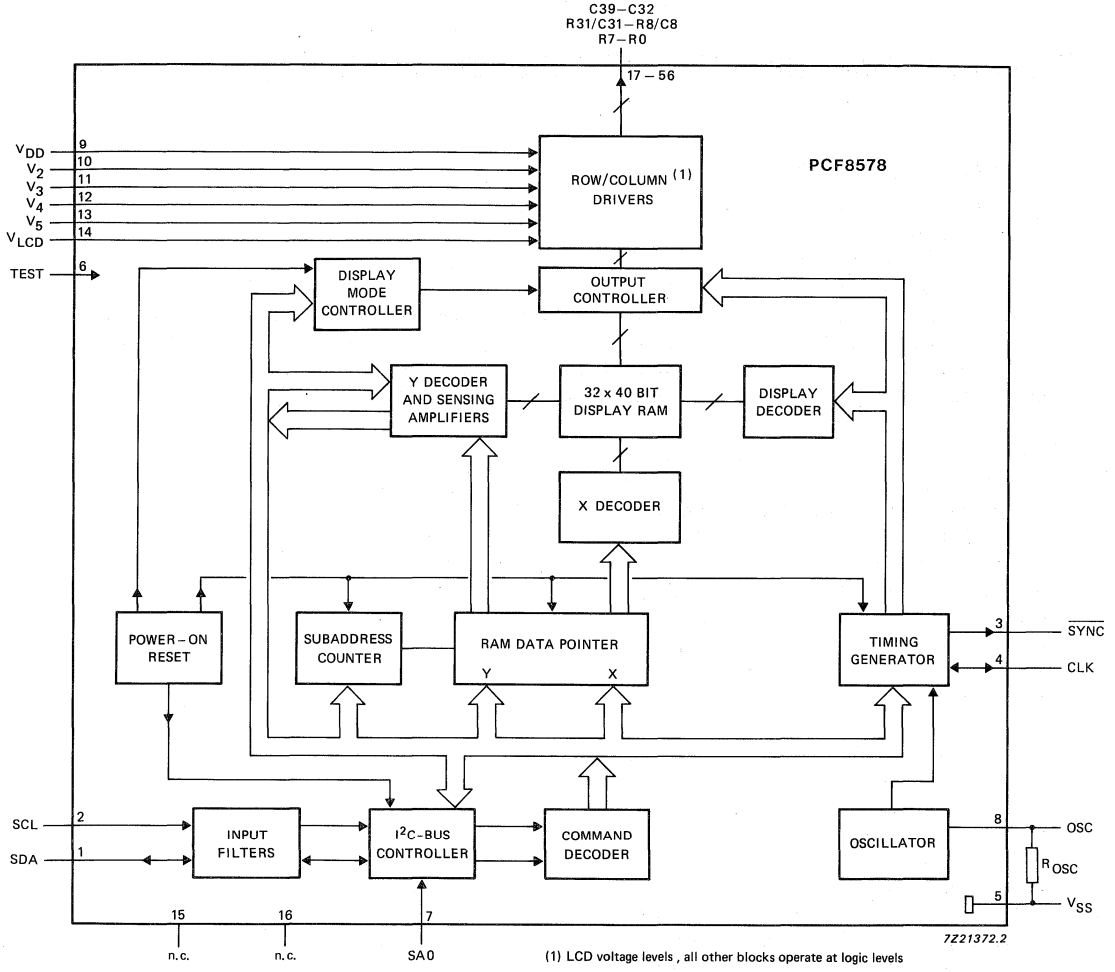


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC12 OR DATASHEET

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I^2C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2.5 V to 6.0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579V: 64-lead tape-automated-bonding module (SOT267A).
PCF8579U: chip with bumps on-tape.

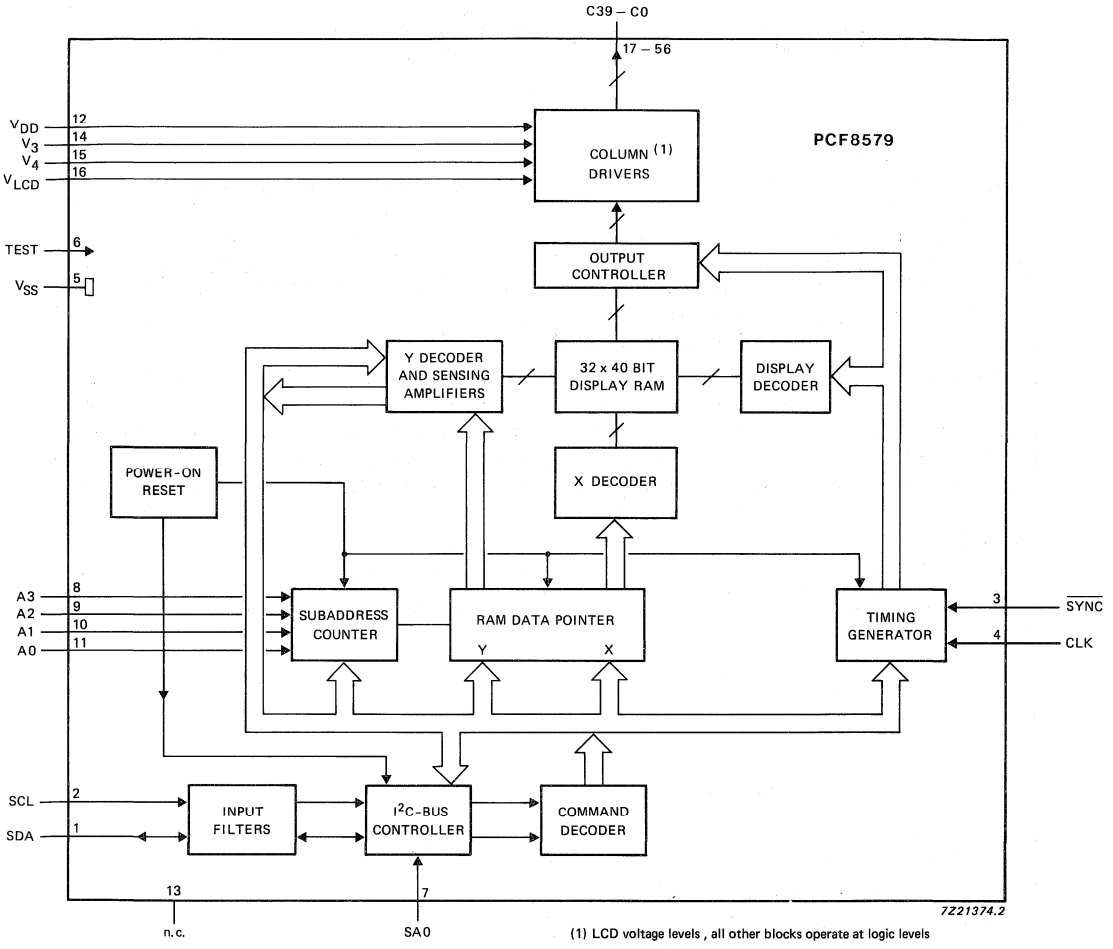


Fig.1 Block diagram.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC10 OR DATASHEET

128 x 8-BIT EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8581 and PCF8581C are low-power CMOS EEPROMs with standard and wide operating voltage:
4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C).

In the following text, the generic term "PCF8581" is used to refer to both types in all packages except where specified.

The PCF8581 is organized as 128 words by 8-bits.

Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. All bytes can be read in a single operation. Up to eight bytes can be written in one operation, reducing the total write time per byte. Three address pins A0, A1 and A2 are used to define the hardware address, allowing the use of up to eight devices connected to the bus without additional hardware.

Features

- Operating supply voltage: 4.5 to 5.5 V (PCF8581); 2.5 to 6.0 V (PCF8581C)
- Integrated voltage multiplier and timer for writing (no external components required)
- Automatic erase before write
- Low standby current max. 10 μA
- Eight-byte page write mode
- Serial input/output bus (I^2C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- Designed for 10 000 write cycles per byte minimum
- 10 years minimum non-volatile data retention
- Infinite number of read cycles
- Pin and address compatibility to PCF8570, PCF8571 and PCF8582

PACKAGE OUTLINES

PCF8581P/PCF8581CP: 8-lead DIL; plastic (SOT97).
PCF8581T/PCF8581CT: 8-lead mini-pack (SO-8L; SOT176C).

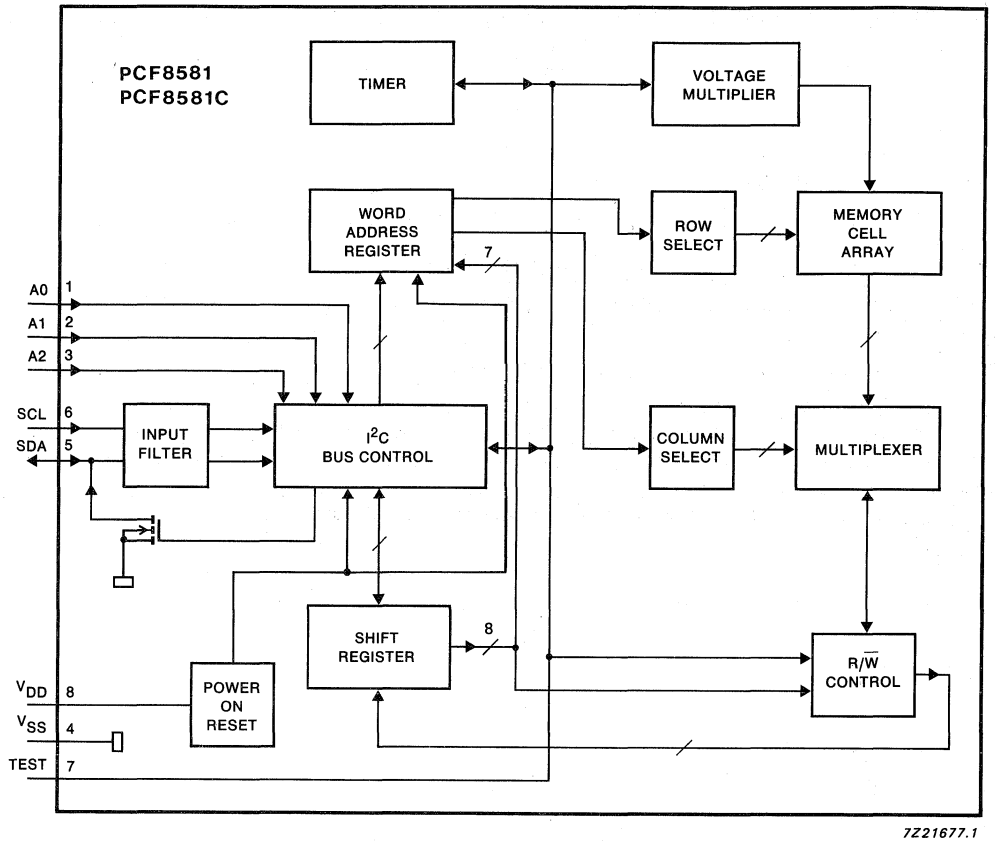


Fig.1 Block diagram.

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- Data retention voltage: 1.0 V to 6 V
- Operating current (f_{scl} = 0 Hz): max. 50 A
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address, READ: A1 or A3, WRITE: A0 or A2.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_{DD}	supply voltage operating range	I²C-bus active	2.5	6.0	V
V_{DD}	supply voltage operating range	I²C-bus inactive	1.0	6.0	V
I_{DD}	supply current operating mode	f_{scl} =100 kHz	-	200	µA
I_{DDO}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	-	50	µA
		f_{scl} = 0 Hz; V_{DD} = 1 V	-	10	µA
T_{amb}	operating ambient temperature range		–40	+85	°C
T_{stg}	storage temperature range		–65	+150	°C

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCF8583P	8	DIL	plastic	SOT97
PCF8583T	8	mini-pack	plastic	SO8L; SOT176C

Clock Calendar with 256 x 8-bit Static RAM

PCF8583

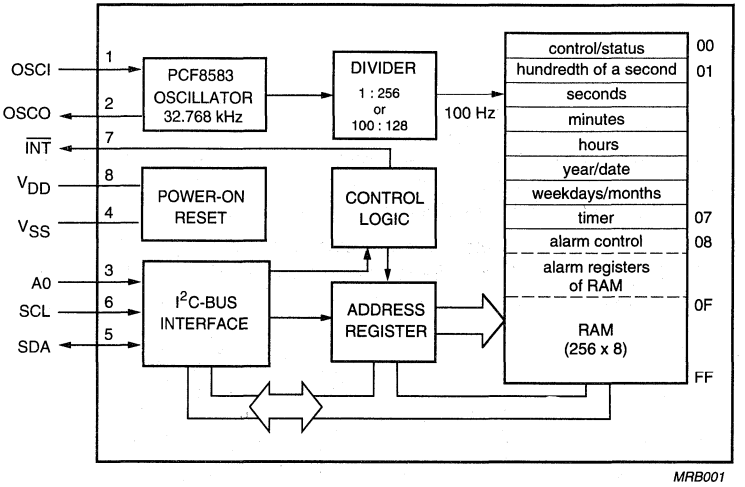


Fig.1 Block diagram.

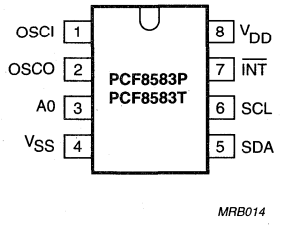


Fig.2 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC03 OR DATASHEET

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

Features

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

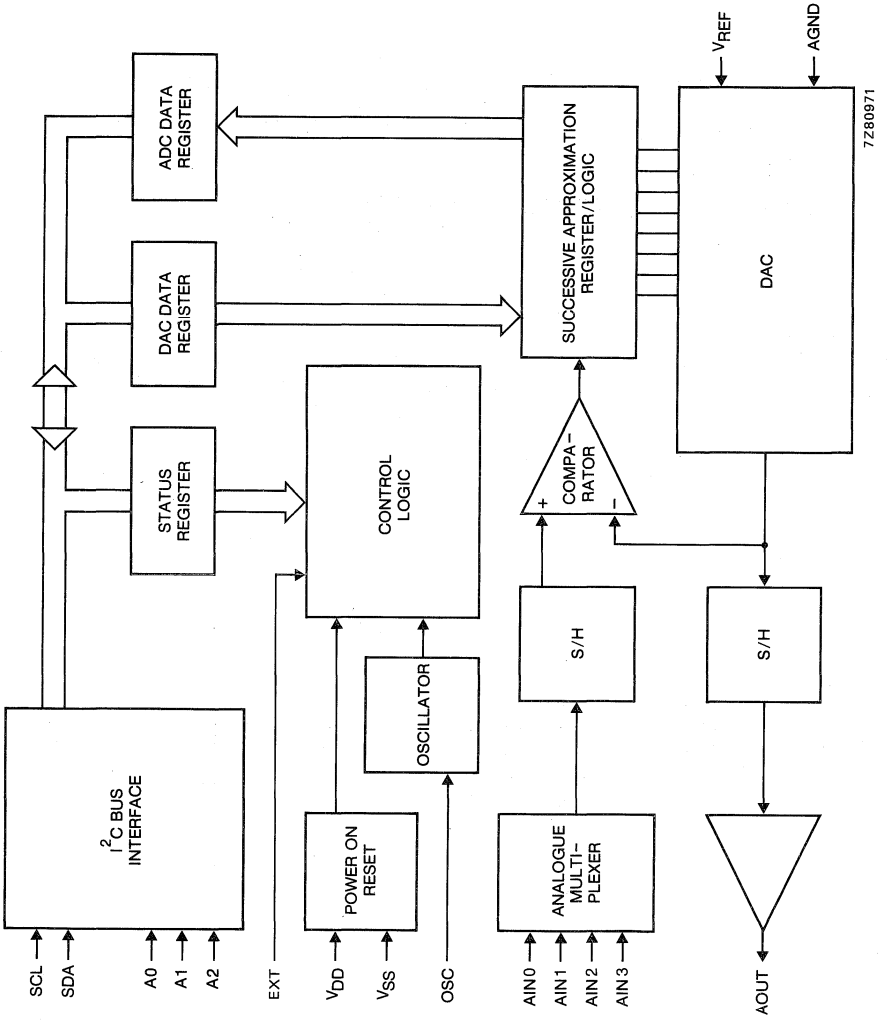


Fig. 1 Block diagram.

256 x 8-BIT CMOS EEPROMS with I²C-bus interface

PCx8582x-2 Family

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8-bits
- Only one power supply required
- On chip voltage multiplier
- Serial input/output bus (I²C)
- Low power CMOS; maximum active current 2 mA, maximum standby current 10 µA
- Power-on reset
- 10 years non-volatile data retention time
- Pin and address compatible to PCF8570, PCF8571, PCF8572 and PCF8581
- Write operations

  byte write mode

  8-byte page write mode (minimizes total write time per byte)
- Read operations

  sequential read and random read
- Extended supply voltage range (2.5 to 6.0 V)
- Internal timer for writing (no external components)
- High reliability by using a redundant storage code
- Endurance 100 k; T_{amb} = +85 °C

GENERAL DESCRIPTION

The 2 Kbit (256 x 8-bit) CMOS EEPROMS are floating gate electrically erasable programmable read only memories. By using an internal redundant storage code it is fault tolerant to single bit errors. This feature dramatically increases reliability compared to conventional EEPROM memories.

Power consumption is low due to the full CMOS technology used. The programming voltage is generated on-chip using a voltage multiplier.

As data bytes are received and transmitted via the serial I²C-bus, a package using eight pins is sufficient. Up to eight PCx8582x-2 devices can be connected to the I²C-bus.
Chip select is accomplished by the three address inputs.

Timing of the Erase/Write cycle is achieved internally, thus no external components are required. Pin 7 must be connected to either V_{DD} or left open-circuit.

An option exists for using an external clock for timing the length of an Erase/Write cycle.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive suppy voltage		2.5	–	6.0	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
		V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
		V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA

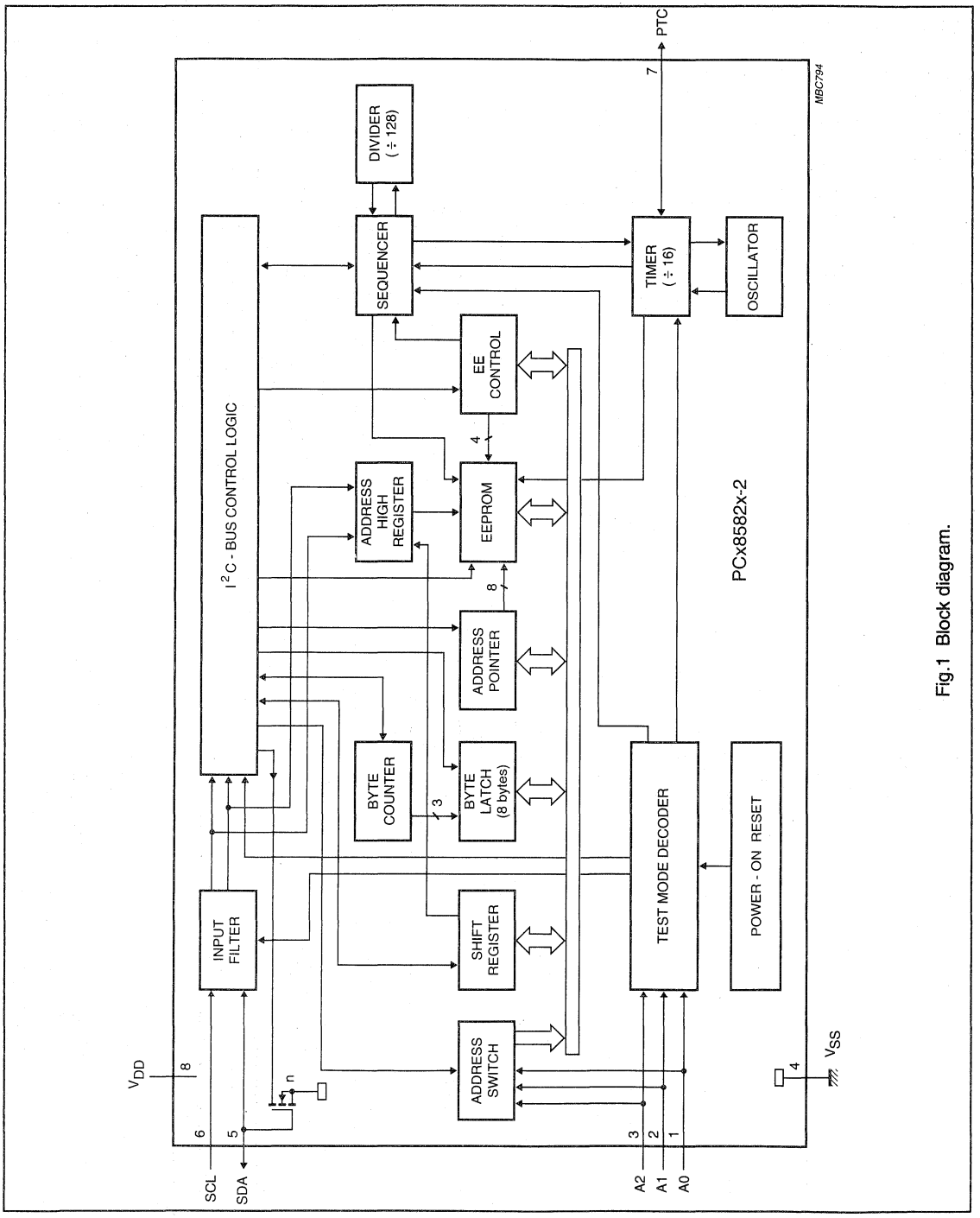


Fig.1 Block diagram.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
PCx8582x-2P	8	DIL	plastic	SOT97
PCx8582x-2T	8	SO8	plastic	SOT96A

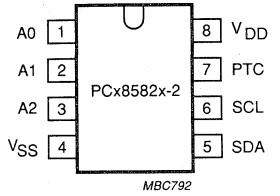


Fig.2 Pin configuration (SOT96A and SOT97).

PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
A2	3	address input
V_{SS}	4	negative supply voltage
SDA	5	serial data
SCL	6	serial clock
PTC	7	programming time control
V_{DD}	8	positive supply voltage

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage		−0.3	+7.0	V
V_I	voltage on any input	$\|Z_I\| > 500\ \Omega$	V_{SS}−0.8	V_{DD} + 0.8	V
I_I	current on any input pin		−	1	mA
I_O	output current		−	10	mA
T_{stg}	storage temperature range		−65	+150	°C
T_{amb}	operating ambient temperature range				
	PCF8582C-2; PCF8582E-2		−40	+85	°C
	PCD8582D-2		−25	+70	°C
	PCA8582F-2		−40	+125	°C

CHARACTERISTICS

PCF8582C-2; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCD8582D-2; V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = –25 to +70 °C
PCF8582E-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C
PCA8582F-2; V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage					
	PCF8582C-2		2.5	–	6.0	V
	PCD8582D-2		3.0	–	6.0	V
	PCF8582E-2; PCA8582F-2		4.5	–	5.5	V
I_{DDR}	supply current READ	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	60	µA
		V_{DD} = 6 V	–	–	200	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	200	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	200	µA
I_{DDW}	supply current ERASE/WRITE	f_{SCL} = 100 kHz				
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	0.5	mA
		V_{DD} = 6 V	–	–	2.0	mA
	PCF8582E-2	$V_{DD\ max}$	–	–	2.0	mA
	PCF8582F-2	$V_{DD\ max}$	–	–	2.0	mA
I_{DDO}	supply current STANDBY					
	PCF8582C-2; PCD8582D-2	V_{DD} = 3 V	–	–	3.5	µA
		V_{DD} = 6 V	–	–	10	µA
	PCF8582E-2	$V_{DD\ max}$	–	–	10	µA
	PCF8582F-2	$V_{DD\ max}$	–	–	10	µA
PTC input						
V_{IH}	HIGH level input voltage		0.9 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.1 V_{DD}	V
SCL input						
V_{IH}	HIGH level input voltage		0.7 V_{DD}	–	V_{DD}+0.8	V
V_{IL}	LOW level input voltage		–0.8	–	0.3 V_{DD}	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	–	–	±1	µA
f_{SCL}	clock frequency		0	–	100	kHz
C_i	input capacitance	$V_I = V_{SS}$	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA input/output						
V_{IL}	LOW level input voltage		−0.8	−	0.3 V_{DD}	V
V_{IH}	HIGH level input voltage		0.7 V_{DD}	−	V_{DD}+0.8	V
V_{OL}	LOW level output voltage	I_{OH} = 3 mA; $V_{DD\ min}$	−	−	0.4	V
I_{LO}	output leakage current	$V_{OH} = V_{DD}$	−	−	1	µA
C_i	input capacitance	$V_I = V_{SS}$	−	−	7	pF
Data retention time						
t_S	data retention time	T_{amb} = +55 °C	10	−	−	yrs

WRITE CYCLE LIMITS

Selection of the chip address is achieved by connecting the A0, A1 and A2 inputs to either V_{DD} or V_{SS}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{E/W}$	ERASE/WRITE cycle time					
	internal oscillator		−	7	−	ms
	external clock		4	−	10	ms
$N_{E/W}$	ERASE/WRITE cycles per byte					
	PCF8582C-2	T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	−	−	500 000	
	PCD8582D-2	T_{amb} = −25 to +70 °C; $t_{E/W}$ = 4 to 10 ms	−	−	10 000	
		T_{amb} = −25 to +40 °C; $t_{E/W}$ = 5 ms	−	−	100 000	
	PCF8582E-2	T_{amb} = −40 to +85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	10 000	
		T_{amb} = +22 °C; $t_{E/W}$ = 5 ms	−	−	100 000	
	PCA8582F-2	T_{amb} = 125 °C; $t_{E/W}$ = 4 to 10 ms	−	−	50 000	
		T_{amb} = 85 °C; $t_{E/W}$ = 4 to 10 ms	−	−	100 000	
		T_{amb} = 22 °C; $t_{E/W}$ = 5 ms	−	−	500 000	

I²C-BUS PROTOCOL

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The serial bus consists of two bidirectional lines: one for data signals (SDA), and one for clock signals (SCL).
Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy: both data and clock lines remain HIGH.

Start data transfer: a change in the state of the data line, from HIGH-to-LOW, while the clock is HIGH, defines the start condition.

Stop data transfer: a change in the state of the data line, from LOW-to-HIGH, while the clock is HIGH, defines the stop condition.

Data valid: the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes,
transferred between the start and stop conditions is limited to seven bytes in the ERASE/WRITE mode and eight bytes in the PAGE ERASE/WRITE mode. Data transfer is unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low-speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined.
The PCx8582x-2 operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

Each byte is followed by one acknowledge bit. This acknowledge bit is a HIGH level, put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse. The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.

The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse.

Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Fig.3). For the PCx8582x-2 this is fixed as 1010.

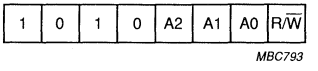


Fig.3 Slave address.

The next three significant bits address a particular device. A system could have up to eight PCx8582x-2 devices on the bus. The eight addresses are defined by the state of the A0, A1 and A2 inputs.

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read operation is selected.
Address inputs must be connected either to V_{DD} or V_{SS}.

WRITE OPERATIONS

Byte/word write

For a write operation the PCx8582x-2 requires a second address field. This address field is a word address providing access to any one of the 256 words of memory. Upon receipt of the word address the PCx8582x-2 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. The master can now terminate the transfer by generating a stop condition or transmit up to six more bytes of data and then terminate by generating a stop condition.

After this stop condition the ERASE/WRITE cycle starts and the bus is free for another transmission. Its duration is 10 ms per byte.
During the ERASE/WRITE cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

PAGE WRITE

The PCx8582x-2 is capable of a eight-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transmit eight data bytes within one transmission. After receipt of each byte the PCx8582x-2 will respond with an acknowledge.

After the receipt of each data byte the three low order bits of the word address are internally incremented. The high order five bits of the address remain unchanged. If the master transmits more than eight bytes prior to generating the stop condition, no acknowledge will be given on the ninth (and following) data bytes and the whole transmission will be ignored. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

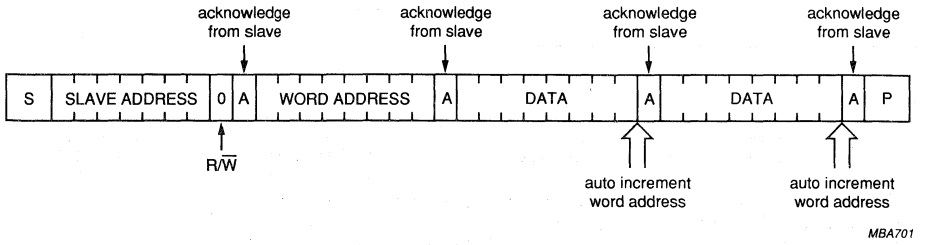


Fig.4 Auto increment memory word address; two byte write.

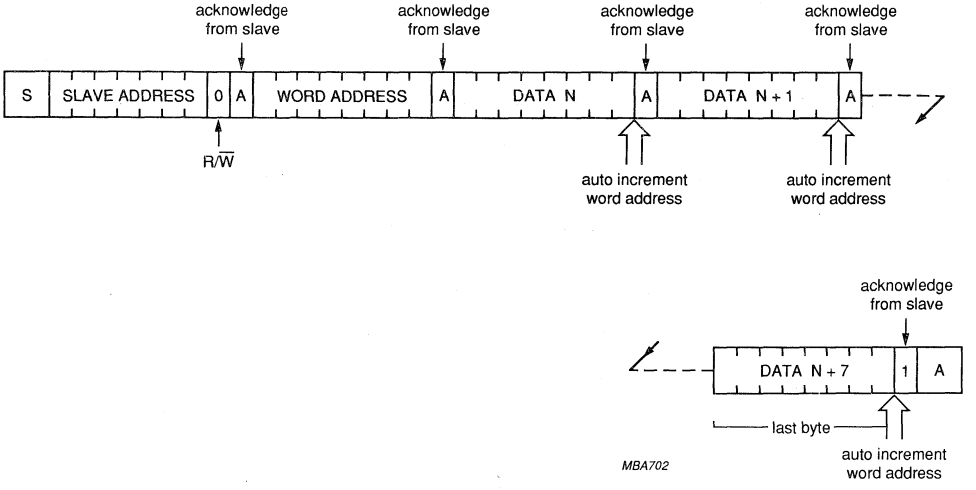


Fig.5 Page write operation; eight byte.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1. There are three basic read operations; current address read, random read and sequential read.

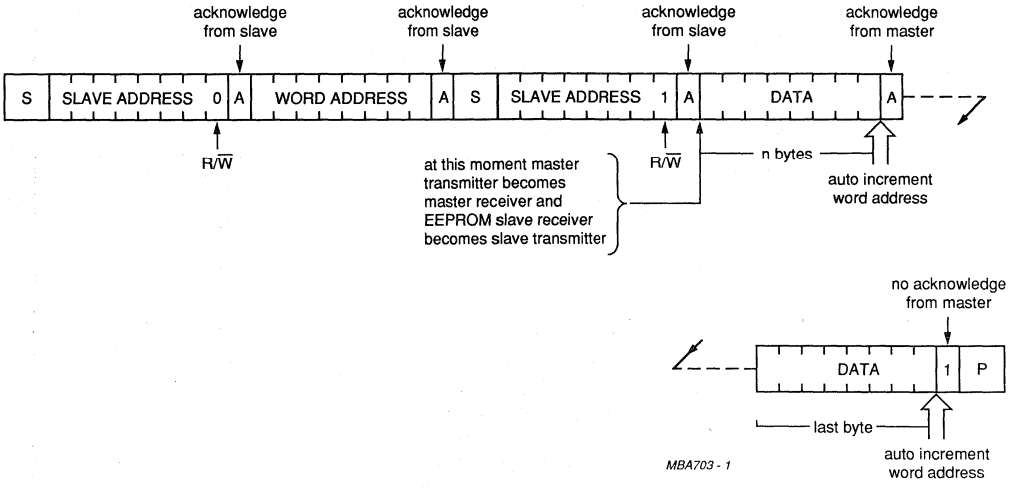


Fig.6 Master reads PCx8582x-2 slave after setting word address (WRITE word address; READ data).

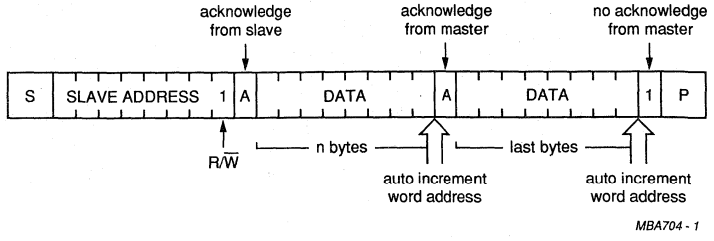


Fig.7 Master reads PCx8582x-2 immediately after first byte (READ mode).

I²C-BUS TIMING

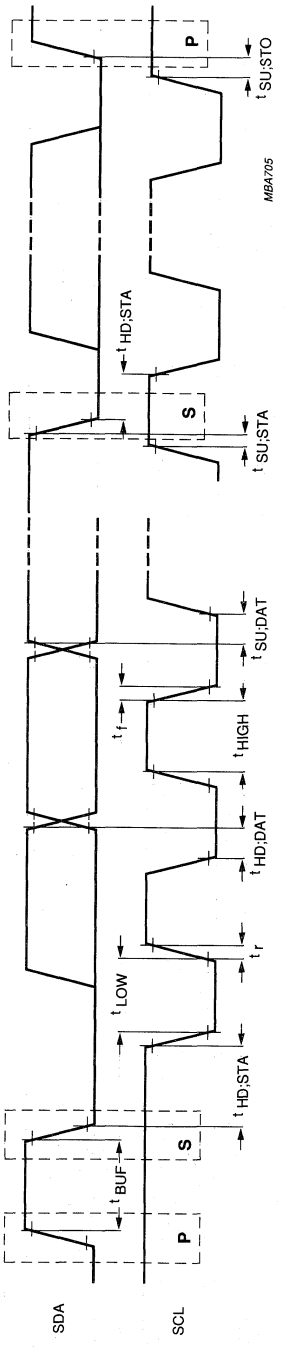
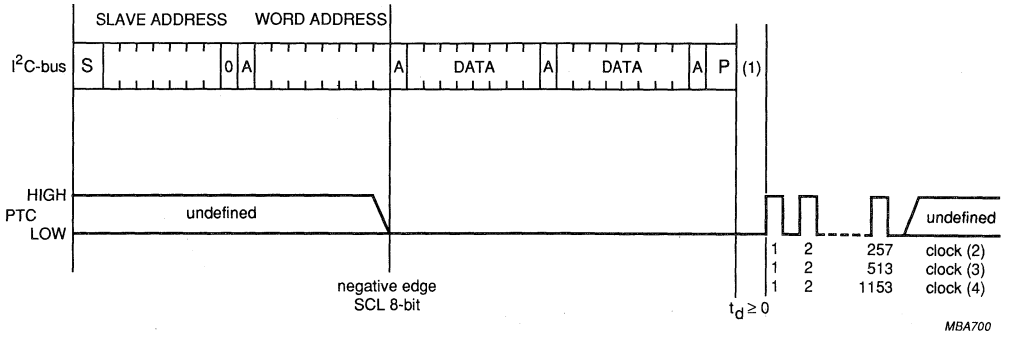


Fig.8 Timing requirements for the I²C-bus.



(1) If an external clock is chosen, this information is latched internally by setting pin 7 (PTC) LOW after transmission of the eight bit of the word address (negative edge of SCL). Thus the state of pin 7 may be previously undefined. Leaving pin 7 LOW causes a higher standby current.

(2) 1-byte programming.

(3) 2-byte programming.

(4) One page (8 byte) programming.

Fig.12 External clock.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 358 10011.

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}	3,6 to 12	V
	V_{CC2}	3,6 to 12	V
	V_{CC3}	V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ. 18	mA
	I_{CC3}	typ. 0,8	mA
Input frequency ranges			
at pin FAM	f_{FAM}	512 kHz to 32	MHz
at pin FFM	f_{FFM}	70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	> 4	MHz
Operating ambient temperature range	T_{amb}	−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102H).

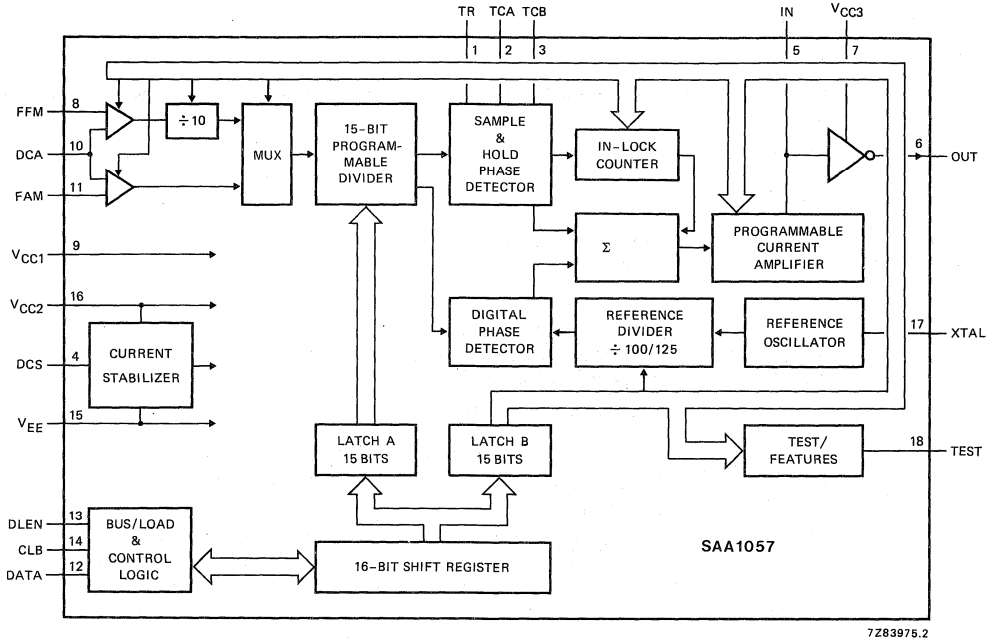


Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.
The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM — FM/AM selection; '1' = FM, '0' = AM

REFH — reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)

CP3, CP2, CP1, CP0 — control bits for the programmable current amplifier (see section Characteristics)

SB2 — enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically

SLA — load mode of latch A; '1' = synchronous, '0' = asynchronous

PDM1, PDM0 — phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM — bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on

T3 — test bit; must be programmed always '0'

T2 — test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin

T1 — test bit; must be programmed always '0'

T0 — test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

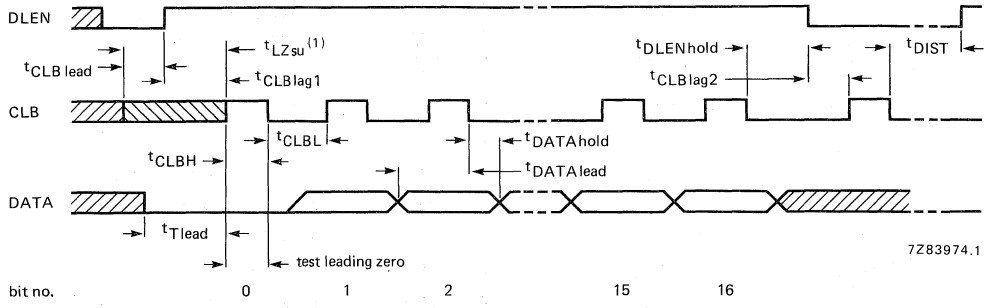


Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^2C bus is used for other devices on the same data and clock lines.

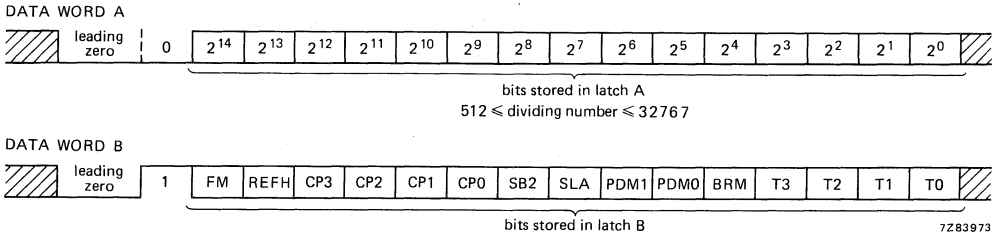


Fig. 3 Bit organization of data words A and B.

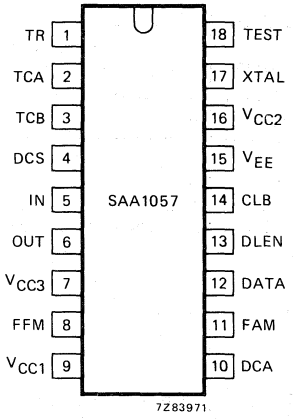


Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}	−0,3 to 13,2	V
Supply voltage; output amplifier	V_{CC3}	V_{CC2} to + 32	V
Total power dissipation	P_{tot}	max. 800	mW
Operating ambient temperature range	T_{amb}	−30 to + 85	°C
Storage temperature range	T_{stg}	−65 to + 150	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	I_{OUT} = 0
Operating ambient temperature	T_{amb}	−25	–	+80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	−30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	10	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device
Busy time asynchronous mode	t_{DIST}	0,3	–	–	ms	or next transmission to SAA1057 after word 'A' (see also note 5)
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	V_{CC2}–0,7	V	
Capacitance at TCA (external)	C_{TCA}	–	–	2,2	nF	REFH = '1'
	C_{TCA}	–	–	2,7	nF	REFH = '0'
Discharge time at TCA	t_{dis}	–	–	5	µs	REFH = '1'
	t_{dis}	–	–	6,25	µs	REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 | CP2 | CP1 | CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT}$ = 1 mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	I_{OUT} = 1 mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	I_{OUT} = 0,1 mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	V_{OUT} = ½ V_{CC3}
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at f_{ripple} = 100 Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	70	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	60	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

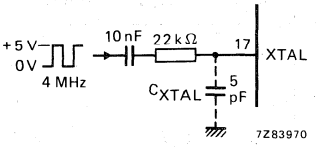


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2}+0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2}+0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.
5. The busy-time after word "A" to another device which has more clock pulses than the SAA1057 (> 17) must be the same as the busy-time for a next transmission to the SAA1057.
   When the other device has a separate DLEN or has less clock pulses than the SAA1057 it is not necessary to keep to this busy-time, 5 μs will be sufficient.

APPLICATION INFORMATION

Initialize procedure

Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

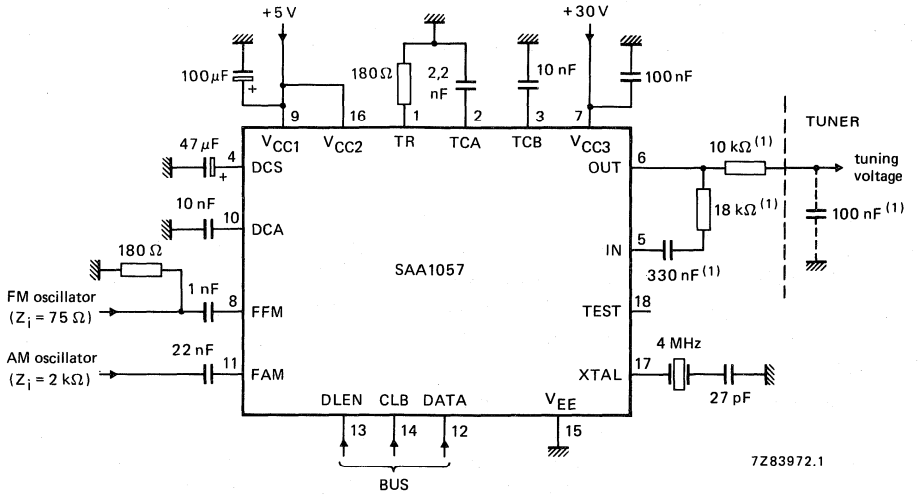
Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').

Transient times of the bus signals

When the SAA1057 is operating in a system with continuous activity on the bus lines, the transient times at the bus inputs should not be less than 100 ns. Otherwise the signal-to-noise ratio of the tuning voltage is reduced.



(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057PLL frequency synthesizer module.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

4-DIGIT LED-DRIVER WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The LED-driver is a bipolar integrated circuit made in an I²L compatible 18 volts process. The circuit is especially designed to drive four 7-segment LED displays with decimal point by means of multiplexing between two pairs of digits. It features an I²C-Bus slave transceiver interface with the possibility to program four different SLAVE ADDRESSES, a POWER RESET flag, 16 current sink OUTPUTS, controllable by software up to 21 mA, two multiplex drive outputs for common anode segments, an on-chip multiplex oscillator, control bits to select static, dynamic and blank mode, and one bit for segment test.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage	$V_{EE} = 0$ V	V_{CC}	4.5	5	15	V
Supply current all outputs OFF	$V_{CC} = 5$ V	I_{CC}*	7	9.5	14	mA
Total power dissipation						
24-lead DIL (SOT101B)		P_{tot}	–	–	1000	mW
24-lead DIL SO (SOT137A)		P_{tot}	–	–	500	mW
Operating ambient temperature range		T_{amb}	–40	–	+85	°C

* The positive current is defined as the conventional current flow into a device (sink current).

PACKAGE OUTLINE

SAA1064: 24-lead DIL; plastic with internal heat spreader (SOT101B).
SAA1064T: 24-lead mini-pack; plastic (SO-24; SOT137A).

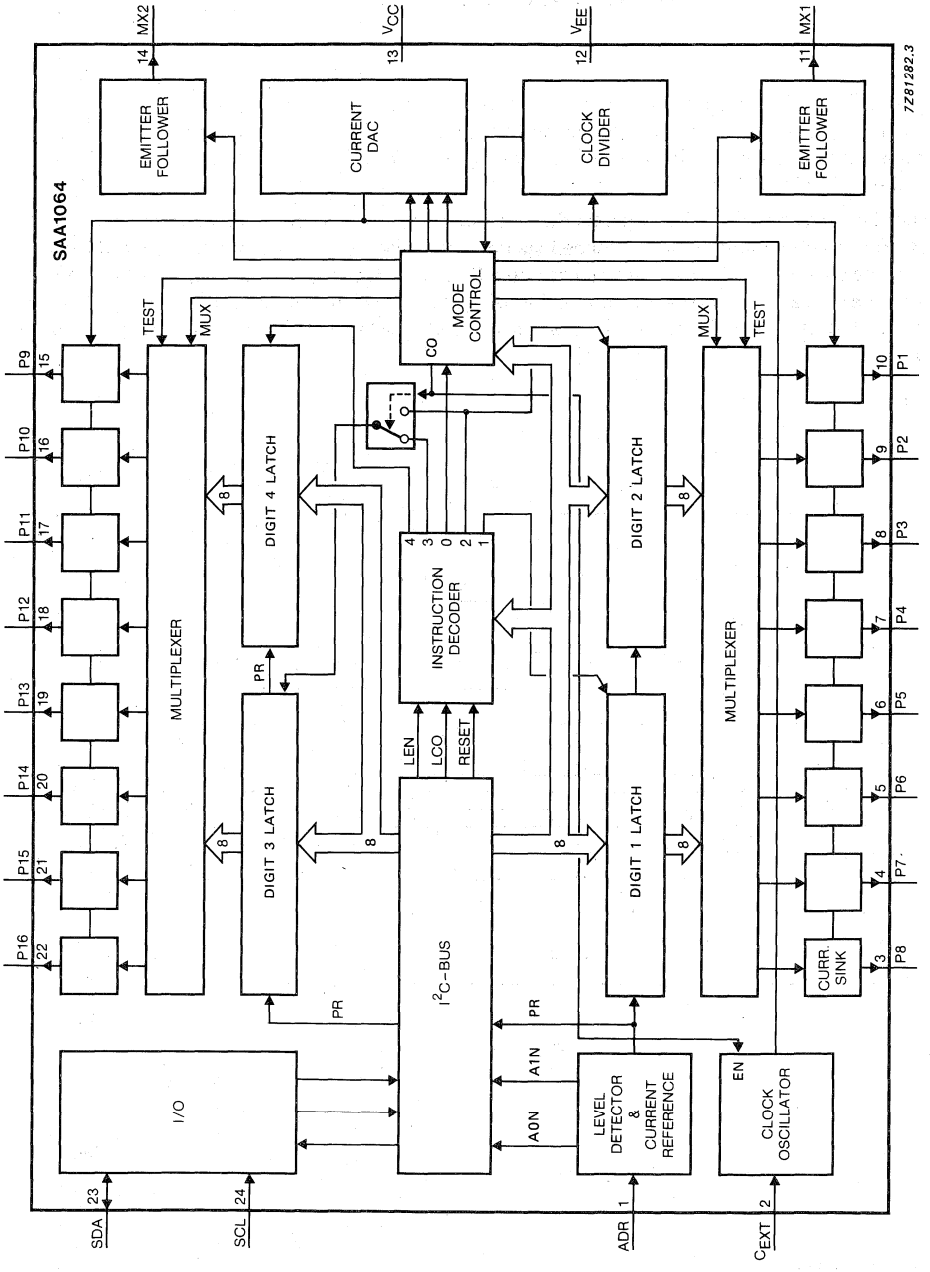


Fig.1 Block diagram.

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I²C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 85 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I²C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I²C bus. A subaddressing system allows the connection of up to three circuits on the same I²C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

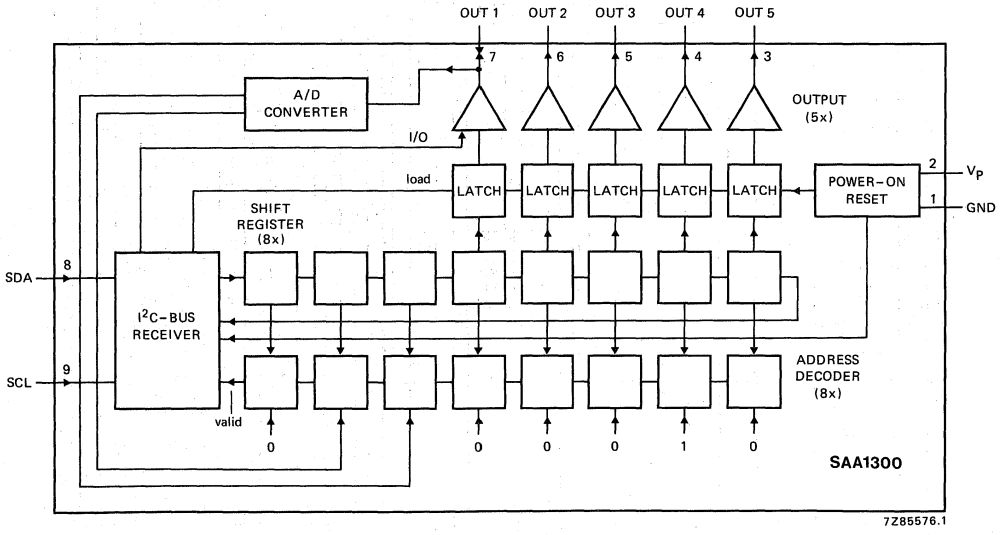


Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT142).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line (I^2C bus)
9	SCL	serial clock line (I^2C bus)

I^2C BUS INFORMATION

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

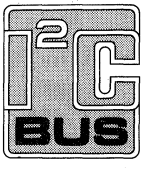
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 6,0	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	825	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	8	12	V
Supply current					
5 outputs LOW	I_{PL}	5	10	15	mA
5 outputs HIGH	I_{PH}	30	50	70	mA
Power-on reset level output stage in "OFF' condition	V_{PR}	–	3,5	3,8	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	3,0	–	5,5	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	$-I_{IH}$	–	–	10	μA
Input current LOW	I_{IH}	–	–	0,4	μA
Acknowledge sink current	I_{ACK}	2,5	–	–	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source: "ON"	I_{Oso}	+ 85	–	+ 150	mA
Maximum output current; source: "ON" T_{amb} = 80 °C	I_{Oso}	60	–	–	mA
Output voltage HIGH at I_{Oso} = 85 mA	V_{OH}	V_P–2	–	–	V
Output current; sink "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi} = –100 μA	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 10 mA	V_{OM}	V_P–0,5	–	–	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

* Outputs must not be driven simultaneously at maximum source current.

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED REMOTE CONTROL TRANSMITTER (LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3007 transmitter IC for infrared remote control systems has a capacity for 1280 commands arranged in 20 subsystem address groups of 64 commands each. The subsystem address may be selected by press-button or slider switches, or be hard-wired.

Commands are transmitted in patterns of pulses coded by the pulse spacing. The pulses can be infrared flashed (single pulse) or modulated. Flashed infrared transmissions require a wideband preamplifier at the receiver, but modulated transmissions allow a narrow band receiver to be used for improved noise rejection. The modulation frequency of the SAA3007 is 455 kHz which allows disturbance-free infrared operation in the presence of 10 - 100 kHz fluorescent lamps.

Features

- Flashed or modulated transmission modes
- Immune from fluorescent lamp disturbance in modulated mode
- Supply voltage range 2 V to 6,5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups
- Up to 64 commands per subsystem address

  } up to 1280 commands
- Requires few additional components

PACKAGE OUTLINES

SAA3007P: 20-lead DIL; plastic (SOT146).
SAA3007T: 20-lead mini-pack; plastic (SO20; SOT163A).

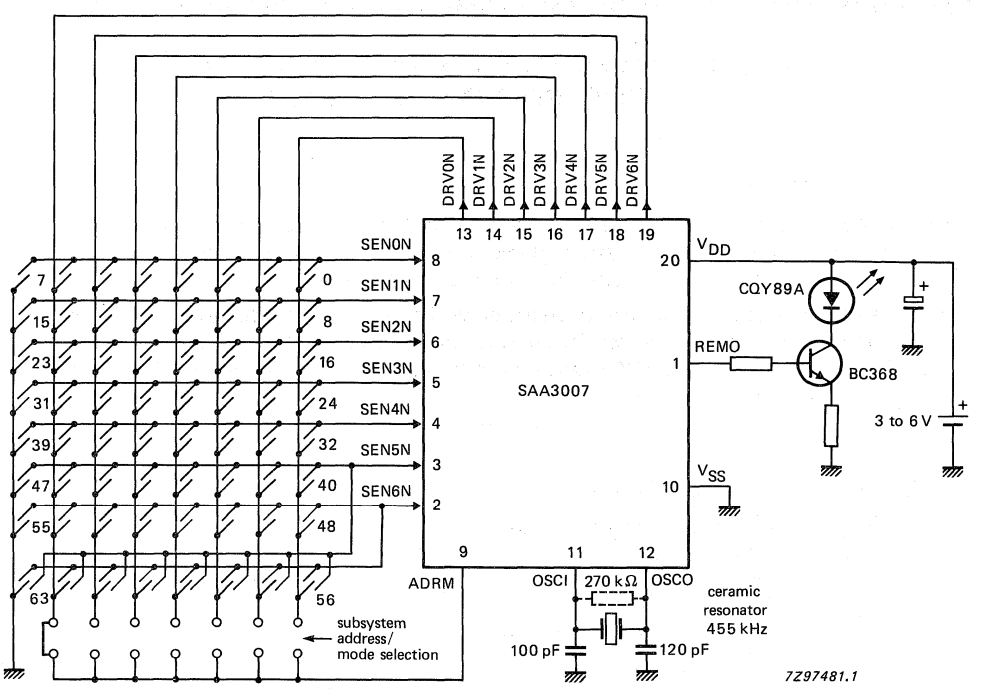


Fig. 1 SAA3007 application example.

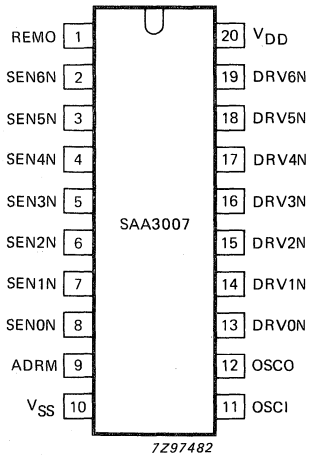


Fig. 2 Pinning diagram.

PINNING

1.	REMO	remote data output
2.	SEN6N	sense inputs from key matrix
3.	SEN5N	
4.	SEN4N	
5.	SEN3N	
6.	SEN2N	
7.	SEN1N	
8.	SEN0N	
9.	ADRM	address/mode control input
10.	V_{SS}	ground (0 V)
11.	OSCI	oscillator input
12.	OSCO	oscillator output
13.	DRV0N	drive outputs to key matrix
14.	DRV1N	
15.	DRV2N	
16.	DRV3N	
17.	DRV4N	
18.	DRV5N	
19.	DRV6N	
20.	V_{DD}	positive supply voltage

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED REMOTE CONTROL TRANSMITTER (RECS 80 LOW VOLTAGE)

GENERAL DESCRIPTION

The SAA3008 transmitter IC is designed for infrared remote control systems. It has a capacity for 1280 commands arranged in 20 sub-system address groups of 64 commands each. The subsystem address may be selected by press-button, slider switches or be hard-wired.

Commands are transmitted in patterns which are pulse distance coded. Modulated pulse transmissions allow a narrow-band receiver to be used for improved noise rejection. The modulation frequency of the SAA3008 is 38 kHz which is 1/12 of the oscillator frequency of 455 kHz (typical).

Features

- Modulated transmission
- Ceramic resonator controlled frequency
- Data-word-start with reference time of unique start pattern
- Supply voltage range 2 V to 6.5 V
- 40 mA output current capability
- Very low standby current ($< 4\ \mu A$ at $V_{DD} = 6$ V)
- Up to 20 subsystem address groups
- Up to 64 commands per subsystem address

} up to 1280 commands

- Requires few additional components

PACKAGE OUTLINES

SAA3008P: 20-lead DIL; plastic (SOT146).
SAA3008T: 20-lead mini-pack; plastic (SO20; SOT163A).

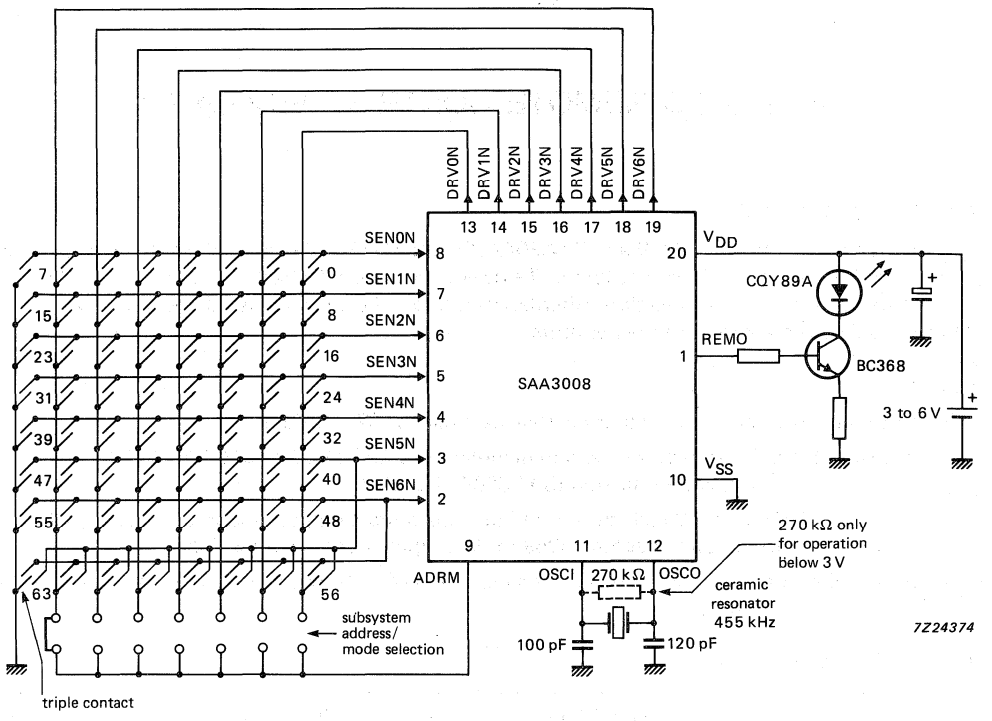


Fig.1 SAA3008 application example.

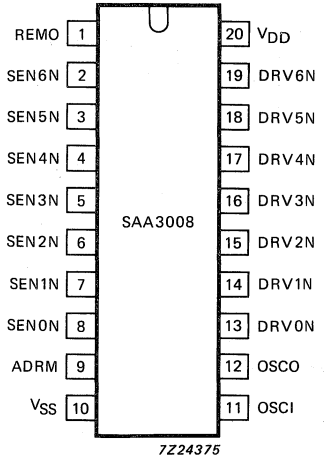


Fig.2 Pinning diagram.

PINNING

1	REMO	remote data output
2	SEN6N	sense inputs from key matrix
3	SEN5N	
4	SEN4N	
5	SEN3N	
6	SEN2N	
7	SEN1N	
8	SEN0N	
9	ADRM	address/mode control input
10	V_{SS}	ground (0 V)
11	OSCI	oscillator input
12	OSCO	oscillator output
13	DRV0N	drive outputs to key matrix
14	DRV1N	
15	DRV2N	
16	DRV3N	
17	DRV4N	
18	DRV5N	
19	DRV6N	
20	V_{DD}	positive supply voltage

INFRARED REMOTE CONTROL DECODERS

GENERAL DESCRIPTION

The main function of the SAA3009 and SAA3049 ICs is to check and convert the received coded data (RECS80/RC5) into latched binary outputs. The device address can be hard-wired for a particular address allowing several devices in one location. Alternatively, received data with any address can be accepted, the received data and address are then outputs.

Features

- Decodes 64 remote control commands with a maximum of 32 subaddresses
- Accepts RECS80 codes with pulse position modulation (SAA3004, SAA3007, SAA3008) or RC5 codes with biphase transmission (SAA3006, SAA3010)
- Available at SAA3009 with 8 high current (10 mA) open-drain outputs and internal pull-ups for direct LED drive via resistors or as SAA3049 for low supply current applications
- Adding circuitry for binary decoding allows a maximum of 2048 commands to be used, for example 1-of-16 decoder (HEF4515)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009	note 1	V_{CC}	4.5	5.0	5.5	V
SAA3049	note 2	V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009	note 1	I_{CC}	–	–	70	mA
SAA3049	note 2	I_{CC}	–	1.0	2.0	mA
Oscillator frequency		f_{osc}	–	4	–	MHz
Output sink current LOW (pins 1 to 8)						
SAA3009	note 3	I_{OL}	–	–	10	mA
SAA3049	note 4	I_{OL}	1.6	3.0	–	mA

Notes to the QUICK REFERENCE DATA

1. T_{amb} = 0 to + 70 °C.
2. T_{amb} = –40 to + 85 °C.
3. Open-drain with 20 to 50 kΩ internal pull-up resistor.
4. Open-drain without internal pull-up resistor at V_{CC} = 5 V ± 10%; V_O = 0.4 V.

PACKAGE OUTLINES

SAA3009P; SAA3049P: 20 lead DIL; plastic (SOT146).
SAA3049T: 20 lead mini-pack; plastic (SO20; SOT163A).

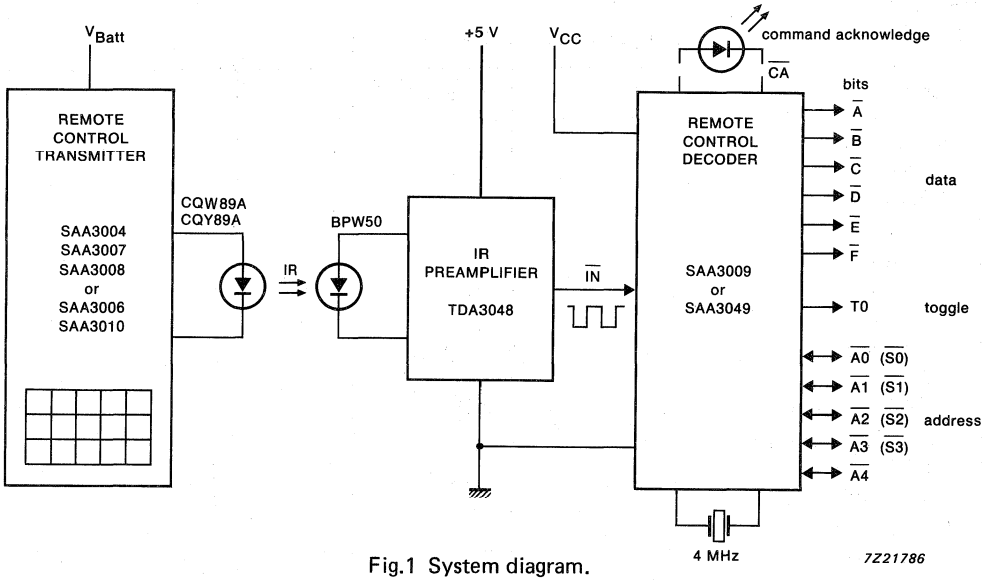


Fig.1 System diagram.

TRANSMITTERS (see individual data sheets for full specifications)

SAA3004 V_{Batt} = 4 to 11 V (max.); 7 x 64 = 448 commands (RECS80 code)

SAA3007 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3008 V_{Batt} = 2 to 6.5 V (max.); 20 x 64 = 1280 commands (RECS80 code)

SAA3006 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

SAA3010 V_{Batt} = 2 to 7.0 V (max.); 32 x 64 = 2048 commands (RC5 code)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage				
SAA3009	V_{CC}	−0.5	7.0	V
SAA3049	V_{CC}	−0.8	8.0	V
Input voltage (any pin)				
SAA3009	V_I	−0.5	7.0	V
SAA3049	V_I	−0.8	V_{CC} + 0.8	V
DC input/output current				
SAA3009 (pins 1 to 8)	$\pm I_I, \pm I_O$	–	20	mA
SAA3009 (all other pins)	$\pm I_I, \pm I_O$	–	10	mA
SAA3049 (any pin)	$\pm I_I, \pm I_O$	–	10	mA
Total power dissipation				
SAA3009	P_{tot}	–	1	W
SAA3049	P_{tot}	–	0.5	W
Operating ambient temperature range				
SAA3009	T_{amb}	0	+ 70	°C
SAA3049	T_{amb}	−40	+ 85	°C
Storage temperature range				
SAA3009	T_{stg}	−65	+ 150	°C
SAA3049	T_{stg}	−65	+ 150	°C

DEVELOPMENT DATA

CHARACTERISTICS

All voltages measured with respect to ground (V_{EE} = 0 V).

SAA3009: V_{CC} = 4.5 to 5.5 V; T_{amb} = 0 to + 70 °C unless otherwise specified
SAA3049: V_{CC} = 2.5 to 5.5 V; T_{amb} = −40 to + 85 unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
SAA3009		V_{CC}	4.5	5.0	5.5	V
SAA3049		V_{CC}	2.5	–	5.5	V
Supply current						
SAA3009		I_{CC}	–	–	70	mA
SAA3049		I_{CC}	–	0.8	2.0	mA
Input signals (pin 9)						
Input voltage HIGH						
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	active					
SAA3009		V_{IL}	0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Mode selection (pin 11)						
Input voltage HIGH	note 1					
SAA3009		V_{IH}	2.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW	note 2					
SAA3009		V_{IL}	−0.5	–	0.8	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Command received indicator and mode control (pin 19)	note 3					
Input voltage HIGH						
SAA3009		V_{IH}	3.0	–	V_{CC} + 0.5	V
SAA3049		V_{IH}	0.7 V_{CC}	–	V_{CC}	V
Input voltage LOW						
SAA3009		V_{IL}	−0.5	–	1.5	V
SAA3049		V_{IL}	0	–	0.3 V_{CC}	V
Crystal oscillator						
Oscillator frequency	note 4	f_{osc}	–	4	–	MHz

parameter	conditions	symbol	min.	typ.	max.	unit
SAA3009 OUTPUTS						
10 mA open-drain with internal pull-up resistor						
(pins 1 to 8)						
Output voltage HIGH	$I_{OH} = -50\ \mu A$	V_{OH}	2.4	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 10$ mA	V_{OL}	–	–	1.0	V
Output sink current LOW		I_{OL}	–	–	10	mA
5 mA open-drain without internal pull-up resistor						
(pins 18 and 19)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 5$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	5	mA
1.6 mA open-drain with internal pull-up resistor						
(pins 15, 16 and 17)						
Output voltage HIGH		V_{OH}	–	–	V_{CC}	V
Output voltage LOW	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output sink current LOW		I_{OL}	–	–	1.6	mA
SAA3049 OUTPUTS						
Open-drain without internal pull-up resistor	note 5					
Output sink current LOW	$V_{CC} = 5$ V ± 10%; $V_{OL} = 0.4$ V	I_{OL}	1.6	3.0	–	mA

DEVELOPMENT DATA

Notes to the characteristics

1. RECS80 decoder for transmitters SAA3004, SAA3007 or SAA3008; SAA3009 has an internal pull-up resistor.
2. RC5 decoder for transmitters SAA3006 or SAA3010.
3. With pin 19 = HIGH, then pins 7, 8, 15, 16 and 17 are address inputs.
   With pin 19 = LOW, then pins 7, 8, 15, 16 and 17 are 4 or 5 address received outputs.

   In Figs 4, 5 and 6 this HIGH/LOW switching is dependent on whether the transistor on pin 19 is fed via a series resistor or not. In both applications pin 19, which toggles several times (see Fig.3) while a valid command is acknowledged, can be used to activate (flash) an LED indicator.
4. A quartz crystal with a frequency of 4 MHz is recommended for the standard transmitter application.
4. Application as output requires connection of an external pull-up resistor.

CHARACTERISTICS (continued)

Reset (pin 14)

The simple circuit is shown in Figs 4, 5 and 6. The alternative reset circuit shown in Fig.2 protects against short term power supply transients by generating a reset.

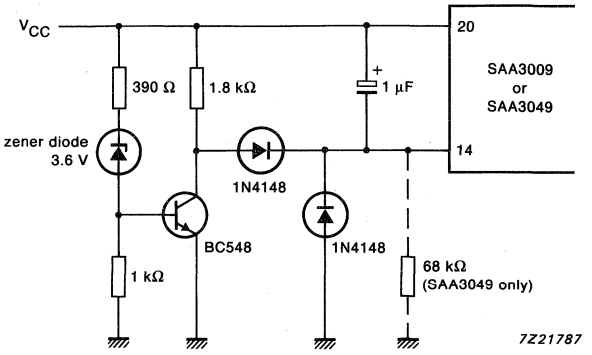


Fig.2 Proposed improved reset circuit.

Infrared signal input (pin 9)

This pin is sensitive to a negative-going edge.

Command received indicator (pin 19)

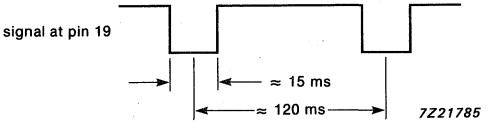
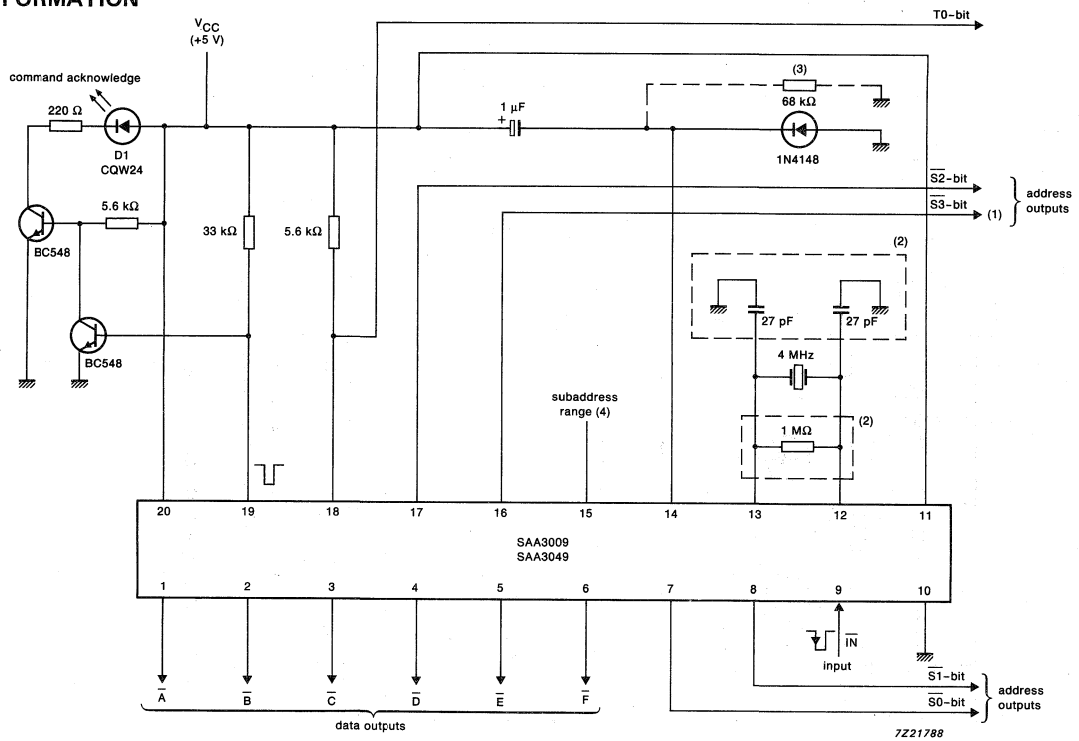


Fig.3 Output diagram of command acknowledge.

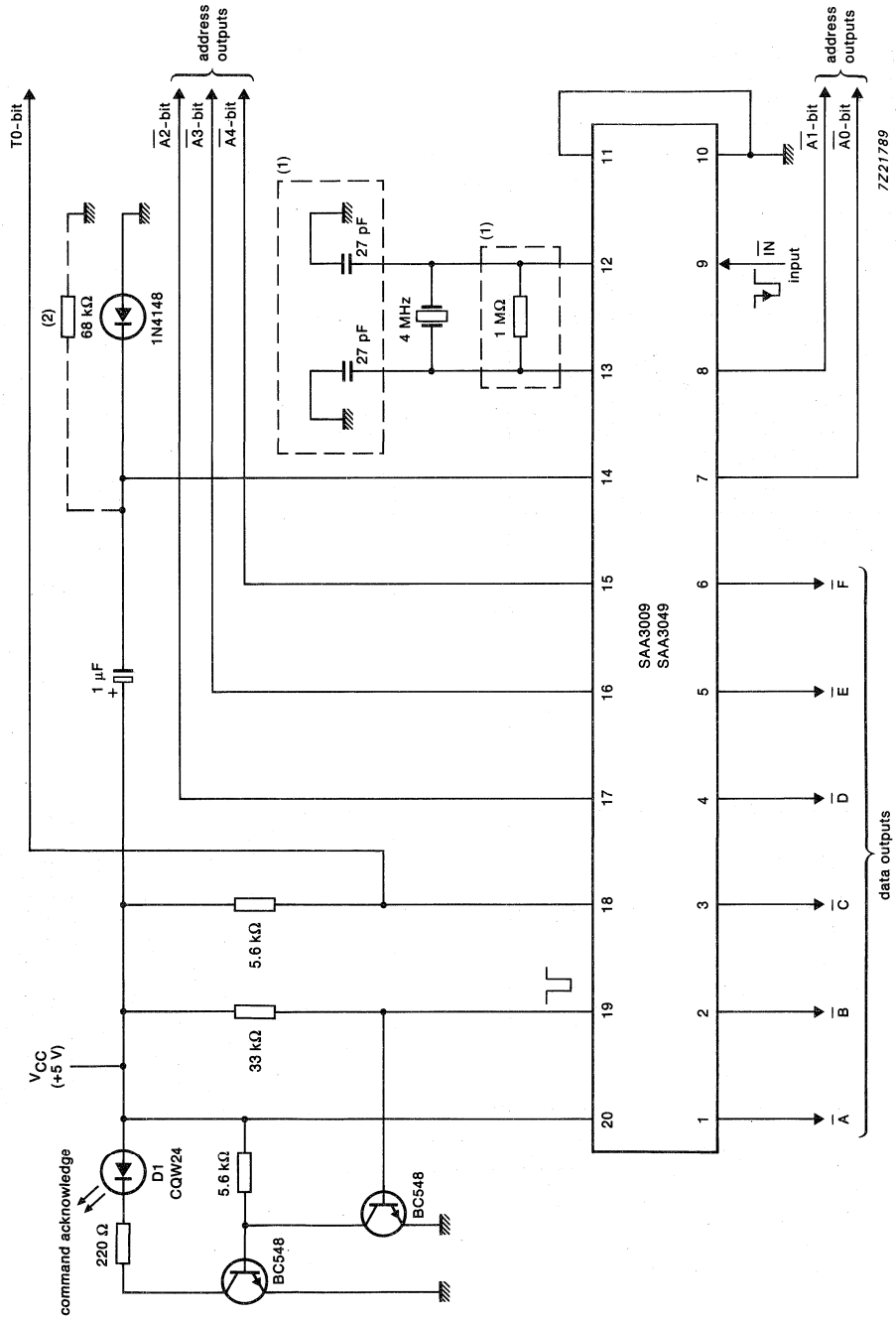
APPLICATION INFORMATION



(1) only for subaddress 8 to 20.
(2) only for SAA3009.
(3) only for SAA3049.
(4) subaddress range:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

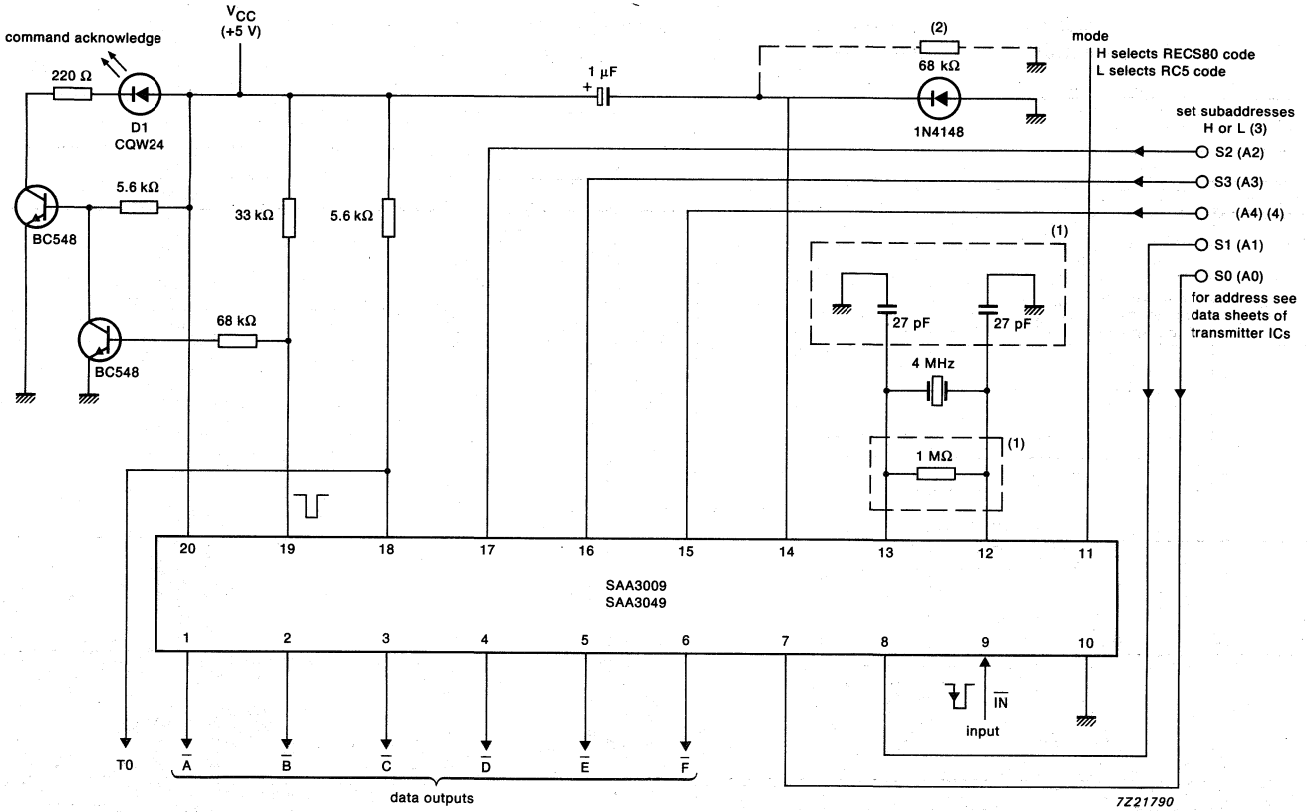
Fig.4 Remote control decoder with latched 11 (10) -bit parallel outputs (10 (9) -bits inverted) for use with transmitter types SAA3004, SAA3007 or SAA3008; pin 11 is HIGH for RECS80 code.

APPLICATION INFORMATION (continued)



(1) only for SAA3009.
(2) only for SAA3049.

Fig.5 Remote control decoder with latched 12-bit parallel outputs (11 bits inverted) for use with transmitter types SAA3006 or SAA3010; pin 11 is LOW for RC5 code.



(1) only for SAA3009.
(2) only for SAA3049.
(3) address inputs:
when LOW address input pin is connected to ground
when HIGH address input pin is open (SAA3009)
when HIGH address input pin is connected via pull-up resistor to V_{CC} (SAA3049)
(4) subaddress range RECS80 code:
when LOW (subaddress 8 to 20) pin 15 is connected to ground
when HIGH (subaddress 1 to 7) pin 15 is open (SAA3009)
when HIGH (subaddress 1 to 7) pin 15 is connected via pull-up resistor to V_{CC} (SAA3049)

Fig.6 Remote control decoder for up to 20 subaddresses with 6 + 1-bit parallel outputs (RECS80 code). Decoder is set for required subaddress by holding address pins HIGH or LOW. Pin 11 is HIGH for use with transmitter types SAA3004, SAA3007 or SAA3008 (RECS80 code). Pin 11 is LOW for use with transmitter types SAA3006 or SAA3010 (RC5 code). Remote control decoder for up to 32 subaddresses with 6 + 1-bit parallel outputs (RC5 code).

FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC02 OR DATASHEET

INFRARED REMOTE CONTROL TRANSMITTER RC-5

GENERAL DESCRIPTION

The SAA3010 is intended as a general purpose (RC-5) infrared remote control system for use where a low voltage supply and a large debounce time are expected. The device can generate 2048 different commands and utilizes a keyboard with a single pole switch for each key. The commands are arranged so that 32 systems can be addressed, each system containing 64 different commands. The keyboard interconnection is illustrated by Fig.3.

The circuit response to legal (one key pressed at a time) and illegal (more than one key pressed at a time) keyboard operation is specified in the section **"KEYBOARD OPERATION"**.

Features

- Low voltage requirement
- Biphase transmission technique
- Single pin oscillator
- Test mode facility

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range	V_{DD}	2	–	7	V
Input voltage range*	V_I	−0.5	–	V_{DD}+0.5	V
Input current	I_I	–	–	±10	mA
Output voltage range*	V_O	−0.5	–	V_{DD}+0.5	V
Output current	I_O	–	–	±10	mA
Operating ambient temperature range	T_{amb}	−25	–	85	°C

* V_{DD}+0.5 V must not exceed 9 V.

The use of this device must conform with the Philips Standard number URT-0421.

PACKAGE OUTLINES

28-lead DIL plastic; (SOT117).
28-lead mini-pack; plastic (SO28; SOT136A).

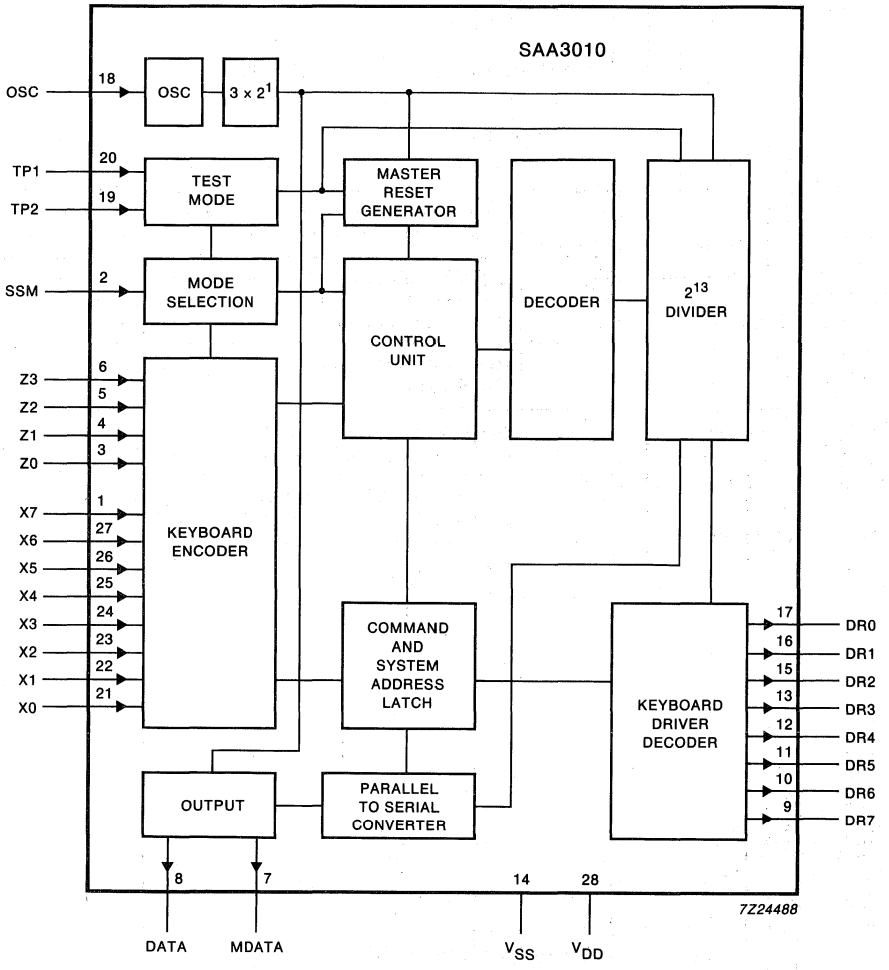


Fig.1 Block diagram.

Data sheet	
status	Preliminary specification
date of issue	March 1992

SAA6579T
Radio data system demodulator (RDS)

SUPERSEDES DATA OF JUNE 1991

FEATURES

- Anti-aliasing filter (2nd order)
- Integrated 57 kHz bandpass filter (8th order)
- Reconstruction filter (2nd order)
- Clocked comparator with automatic offset compensation
- 57 kHz carrier regeneration
- Synchronous demodulator for 57 kHz modulated RDS signals
- Selectable 4.332 / 8.664 MHz crystal oscillator with variable dividers
- Clock regeneration with lock on biphase data rate
- Biphase symbol decoder with integrate and dump functions
- Differential decoder
- Signal quality detector
- Subcarrier output

GENERAL DESCRIPTION

The integrated CMOS circuit SAA6579T is a RDS demodulator. It recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting.

The data signal RDDA and the clock signal RDCL are provided as outputs for further processing by a suitable decoder (microcomputer).

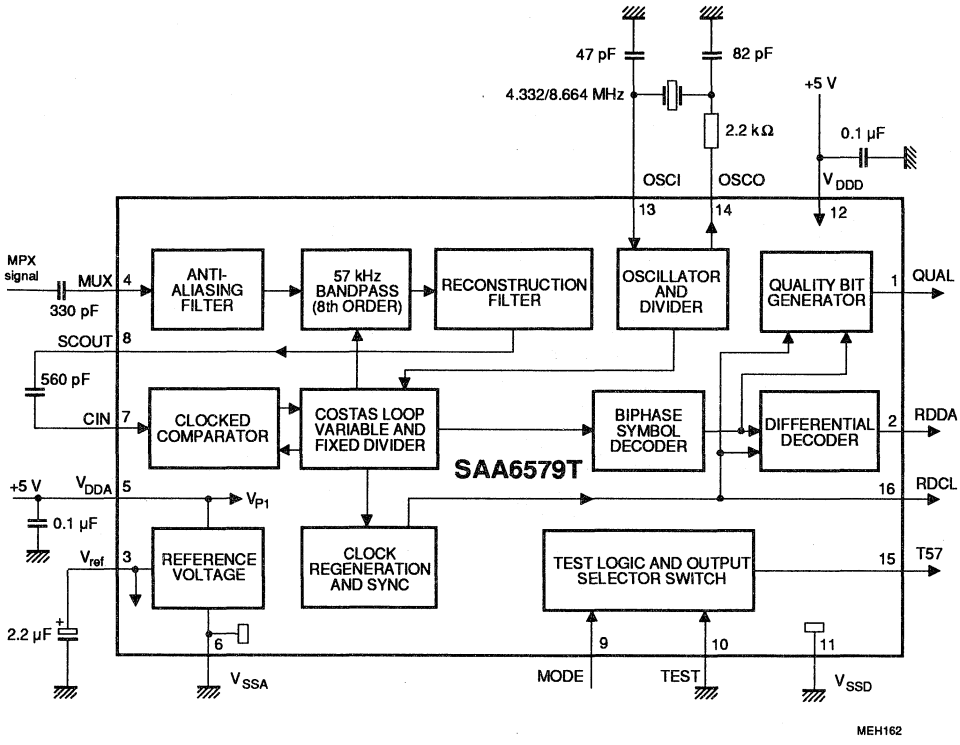
The operational functions of the device are in accordance with the CENELEC EN 50067.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)	3.6	5	5.5	V
V_{DDD}	digital supply voltage (pin 12)	3.6	5	5.5	V
I_{tot}	total supply current	–	6	–	mA
V_i	RDS input amplitude (RMS value, pin 4)	1	–	–	mV
$V_{o\,H}$	output level HIGH for signals RDDA, RDCL, QUAL and T57	4.4	–	–	V
$V_{o\,L}$	output level LOW for signals RDDA, RDCL, QUAL and T57	–	–	0.4	V
T_{amb}	operating ambient temperature	–40	–	85	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA6579T	16	mini-pack	plastic	SOT162A



Via the pin MODE two different crystal frequencies can be used:

MODE	x-tal clock
LOW	4.332 MHz
HIGH	8.664 MHz

Fig.1 Block diagram and application circuit.

Radio data system demodulator (RDS)

SAA6579T

PINNING

SYMBOL	PIN	DESCRIPTION
QUAL	1	quality indication output
RDDA	2	RDS data output
V_{ref}	3	reference voltage output (0.5 V_{DDA})
MUX	4	multiplex signal input
V_{DDA}	5	+5 V supply voltage for analog part
V_{SSA}	6	ground for analog part (0 V)
CIN	7	subcarrier input to comparator
SCOUT	8	subcarrier output of reconstruction filter
MODE	9	oscillator mode / test control input
TEST	10	test enable input
V_{SSD}	11	ground for digital part (0 V)
V_{DDD}	12	+5 V supply voltage for digital part
OSCI	13	oscillator input
OSCO	14	oscillator output
T57	15	57 kHz clock signal output
RDCL	16	RDS clock output

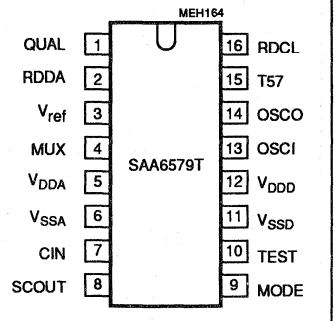


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The SAA6579T is a demodulator circuit for RDS applications. It contains a 57 kHz bandpass filter and a digital demodulator to regenerate the RDS data stream out of the multiplex signal (MPX).

Filter part

The MUX signal is band-limited by a second-order anti-aliasing-filter and fed through a 57 kHz bandpass filter (8th order bandpass filter with 3 kHz bandwidth) to separate the RDS signals. This filter is formed in switched capacitor technique and clocked by a clock frequency of 541.5 kHz derived from the 4.332/8.664 MHz crystal oscillator. Then the signal is fed to the reconstruction filter to smooth the sampled and filtered RDS signal before it is output on pin 8.

The signal is AC-coupled to the comparator (pin 7), which is clocked with a frequency of 228 kHz (synchronized by the 57 kHz of the demodulator).

Digital part

The synchronous demodulator (Costas loop block) with carrier regeneration demodulates the internal coupled, digitized signal. The suppressed carrier is recovered from the two sidebands (Costas loop). The demodulated signal is low-pass-filtered in such a way that the overall pulse shape (transmitter and receiver) approaches a co-sinusoidal form in conjunction with the following "Integrate and Dump" circuit.

The data-spectrum shaping is split into two equal parts and handled in the transmitter and in the receiver. Ideally, the data filtering should be equal in both of these parts. The overall data-channel-spectrum shaping of the transmitter and the receiver is approximately 100% roll-off.

The "Integrate and Dump" circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in form of biphase symbols being output from the integrate and dump circuit. The final stages of RDS data processing are the biphase symbol decoding and the differential decoding. After synchronization by data clock RDCL (pin 16) data appears on the RDDA output (pin 2).

The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of "good" data (QUAL = HIGH) or "corrupt" data (QUAL = LOW).

Timing

Fixed and variable dividers are applied to the 4.332/8.664 MHz crystal oscillator to generate the 1.1875 kHz RDS clock RDCL, which is synchronized by the incoming data. Which ever clock edge is considered (positive or negative going edge) the data will remain valid for 399 µs after the clock transition. The timing of data change is 4 µs before a clock change. Which clock transition (positive or negative going clock) the data change occurs in, depends on the lock conditions and is arbitrary (bit slip).

During poor reception it is possible that faults in phase occur, then the clock signal stays uninterrupted, and data is constant for 1.5 clock periods. Normally, faults in phase do not occur on a cyclic basis. If however, faults in phase occur in this way, the minimum spacing between two possible faults in phase depends on the data being transmitted. The minimum spacing cannot be less than 16 clock periods.

The quality bit changes only at the time of a data change.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134); ground pins 6 and 11 connected together.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	supply voltage (pin 5)	0	6	V
V_{DDD}	supply voltage (pin 12)	0	6	V
V_n	voltage on all pins, grounds excluded	−0.5	V_{DD}+0.5	V
T_{stg}	storage temperature range	−40	150	°C
T_{amb}	operating ambient temperature range	−40	85	°C
V_{ESD}	electrostatic handling* for all pins	±400	–	V
	electrostatic handling** for all pins	±3000	–	V

* Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

** Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

$V_{DDA} = V_{DDD} = 5$ V; $T_{amb} = +25$ °C and measurements taken in Fig.1 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	supply voltage range (pin 5)		3.6	5	5.5	V
V_{DDD}	supply voltage range (pin 12)		3.6	5	5.5	V
I_{tot}	total supply current	I_1+I_2	–	6	–	mA
V_{ref}	reference voltage (pin 3)	$V_{DDA} = 5$ V	–	2.5	–	V
MPX input (signal before the capacitor on pin 4)						
$V_{i\ MPX}$	RDS amplitude (RMS value)	$\Delta f = \pm 1.2$ kHz RDS; $\Delta f = \pm 3.5$ kHz ARI; see Fig.4	1	–	–	mV
	maximum input signal capability	f = 57 ±2 kHz	200	–	–	mV
	(peak-to-peak value)	f < 50 kHz	1.4	–	–	V
		f < 15 kHz	2.8	–	–	V
		f > 70 kHz	3.5	–	–	V
R_{4-6}	input resistance	f = 0 to 100 kHz	40	–	–	kΩ
G_{8-4}	signal gain	f = 57 kHz	17	20	23	dB
57 kHz bandpass filter						
f_o	centre frequency	$T_{amb} = -40$ to +85 °C	56.5	57.0	57.5	kHz
B	–3 dB bandwidth		2.5	3.0	3.5	kHz
G	stopband attenuation	$\Delta f = \pm 7$ kHz	31	–	–	dB
		f < 45 kHz	40	–	–	dB
		f < 20 kHz	50	–	–	dB
		f > 70 kHz	40	–	–	dB
R_8	output resistance (pin 8)	f = 57 kHz	0.5	10	18	Ω
Comparator input (pin 7)						
V_i	minimum input level (RMS value)	f = 57 kHz	–	1	10	mV
R_{CIN}	input resistance		70	110	150	kΩ
Oscillator input (pin 13)						
$V_{I\,H}$	input voltage HIGH	$V_{DDD} = 5.0$ V	4.0	–	–	V
$V_{I\,L}$	input voltage LOW	$V_{DDD} = 5.0$ V	–	–	1.0	V
I_I	input current	$V_{DDD} = 5.5$ V	–	–	±1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital demodulator and outputs QUAL, RDDA, T57, OSCO and RDCL (pins 1, 2, 14, 15 and 16)						
$V_{Q\,H}$	output voltage HIGH	I_Q = –20 µA; V_{DDD} = 4.5 V	4.4	–	–	V
$V_{Q\,L}$	output voltage LOW	I_Q = 3.2 mA; V_{DDD} = 5.5 V	–	–	0.4	V
f_{RDCL}	nominal clock frequency RDCL		–	1187.5	–	Hz
Δt_{RDCL}	jitter of RDCL		–	–	18	µs
f_{T57}	nominal subcarrier frequency T57	note 1	–	57.0	–	kHz
I_Q	output current	V_{DDD} = 4.5 V				
	OSCO (pin 14)	V_{14} = 0.4 V	1.5	–	–	mA
		V_{14} = 4.1 V	–1.6	–	–	mA
	QUAL, RDDA, T57, RDCL (pins 1, 2, 15, 16)	V_{14} = 0.4 V	5.9	–	–	mA
		V_{14} = 4.1 V	–5.3	–	–	mA
4.332 MHz crystal parameters						
XTAL	frequency f_o		–	4.33200	–	MHz
	maximum permitted tolerance		–	±50	–	10^{-6}
	adjustment tolerance of f_o	T_{amb} = +25 °C	–	–	±20	10^{-6}
	load capacitance	T_{amb} = –40 to +85 °C	–	–	±25	10^{-6}
			–	30	–	pF
	resonance resistance		–	–	60	Ω
8.664 MHz crystal parameters						
XTAL	frequency f_o		–	8.664	–	MHz
	maximum permitted tolerance		–	±50	–	10^{-6}
	adjustment tolerance of f_o	T_{amb} = +25 °C	–	–	±30	10^{-6}
	load capacitance	T_{amb} = –40 to +85 °C	–	–	±30	10^{-6}
			–	30	–	pF
	resonance resistance		–	–	60	Ω

Note to the characteristics

1. The signal T57 has a phase lead of 123 ° (±180 °) relative to the ARI carrier at output SCOUT.

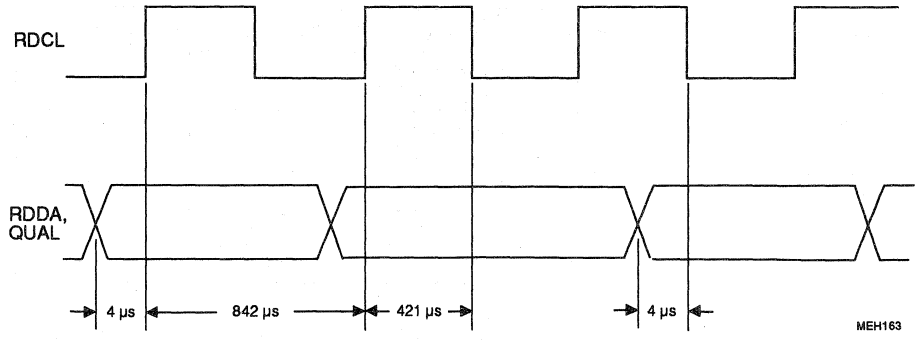


Fig.3 RDS timing diagram including a phase jump.

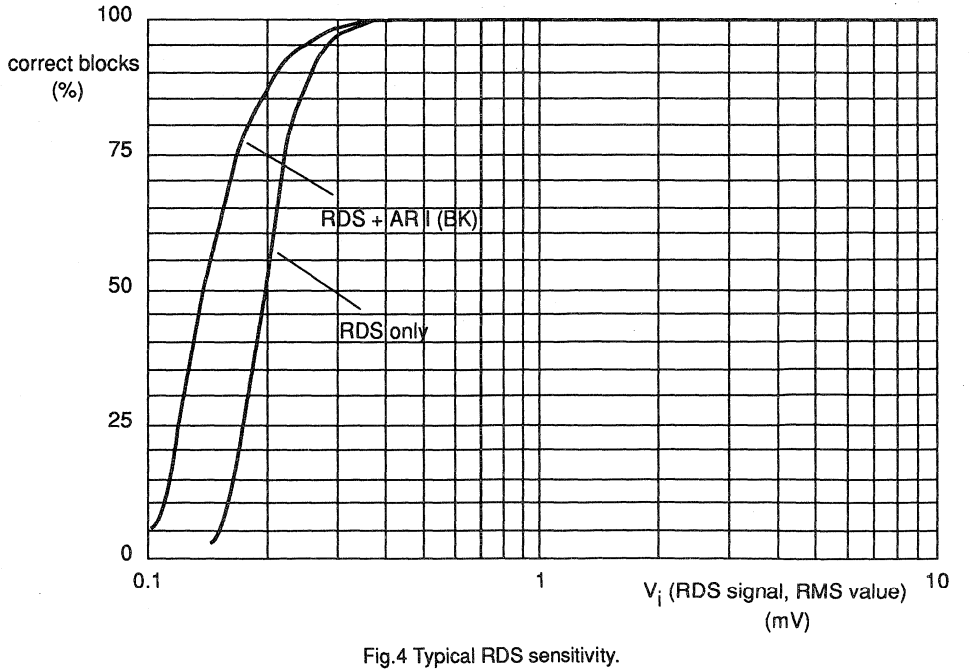


Fig.4 Typical RDS sensitivity.

DIGITAL FILTER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7220 is a stereo interpolating digital filter designed for the Compact Disc Digital Audio system. For descriptive purposes, the SAA7220 is referred to as the B-chip and the SAA7210 as the A-chip.

Features

- 16-bit serial data input (two's complement)
- Interpolated data replaces erroneous data samples
- −12 dB attenuation via the active LOW attenuation input control (ATSB)
- Smoothed transitions before and after muting
- Two identical finite impulse response transversal filters each with a sampling rate of four times that of the normal digital audio data
- Digital audio output of 32-bit words transmitted in biphase-mark code
- I²S data transfer between SAA7210, SAA7220 and 16-bit dual DAC (TDA1541)

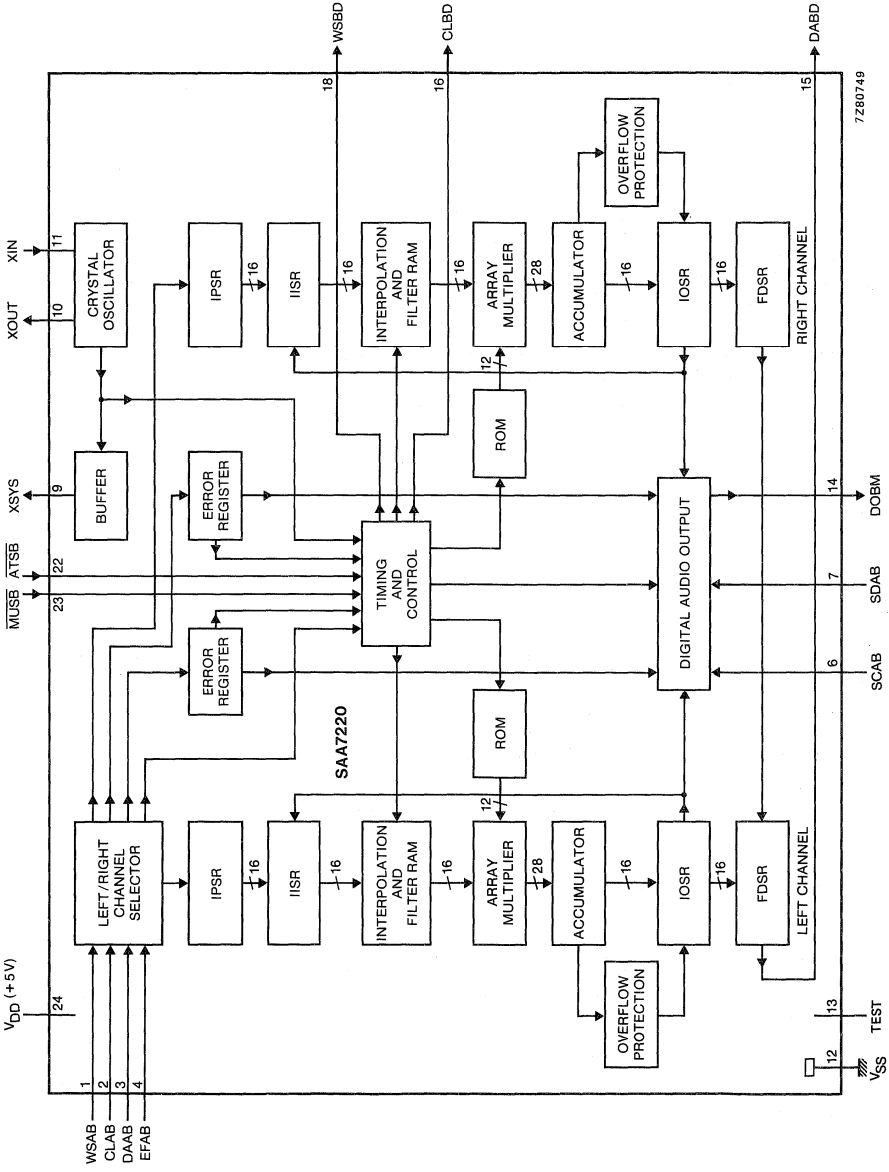
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 24)		V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)		I_{DD}	100	180	285	mA
Input voltage ranges						
WSAB, DAAB, EFAB, SDAB	note 2					
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$	note 3					
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD}+0,5	V
Output voltage ranges						
DABD, CLBD, WSBD						
Output voltage LOW	I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
DOBM						
Voltage across a 75 Ω load via attenuator (peak-to-peak value)	see Fig. 10	$V_{L(p-p)}$	0,4	–	0,6	V
Operating frequency XTAL		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating ambient temperature range		T_{amb}	−20	–	+ 70	°C

For explanation of notes see "Notes to the characteristics".

PACKAGE OUTLINE

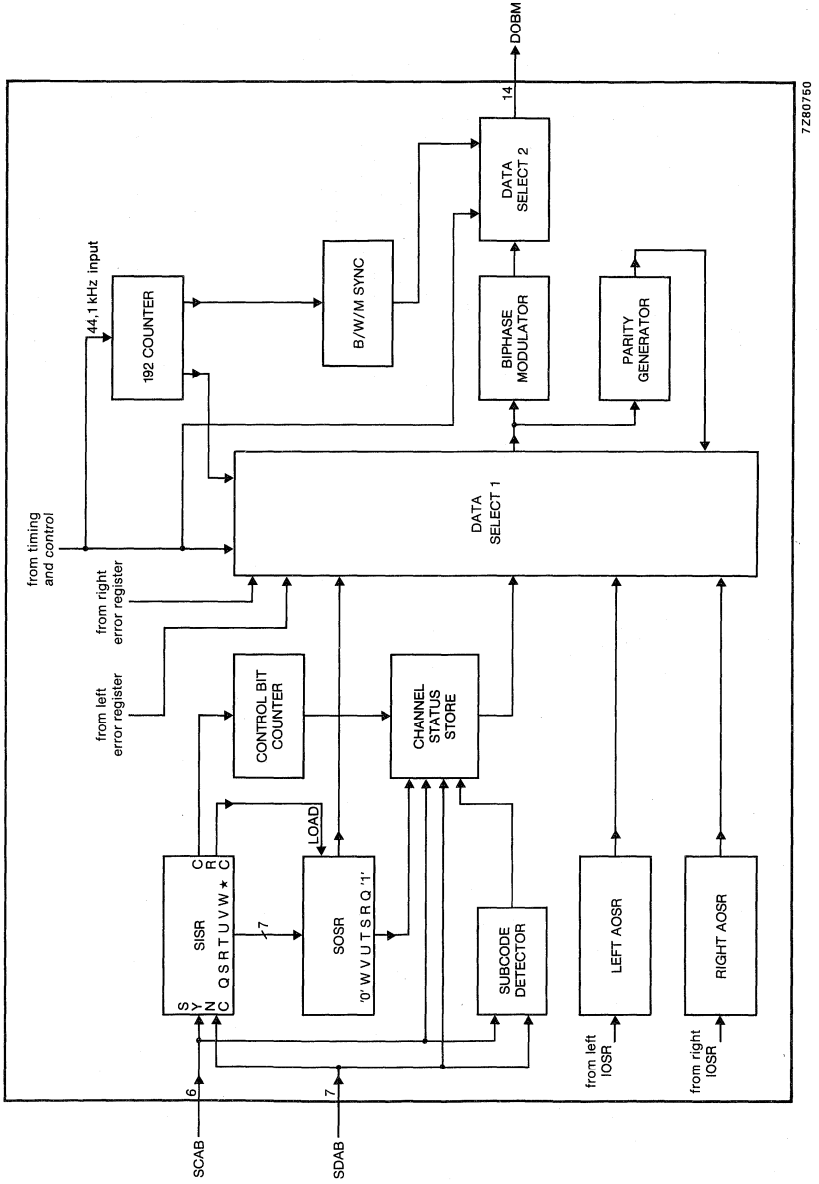
SAA7220P/A: 24-lead DIL; plastic (with internal heat spreader) (SOT101A).



Where:

IPSR = Input Shift Register
IISR = Intermediate Input Shift Register
IOSR = Intermediate Output Shift Register
FDSR = Filter Data Shift Register

Fig. 1 Digital filter block diagram.



Where:

SISR = Subcode Input Shift Register
SOSR = Subcode Output Shift Register
IOSR = Intermediate Output Shift Register
AOSR = Audio Output Shift Register
* = Subcode word error flag

Fig. 2 Digital audio output block diagram.

PINNING

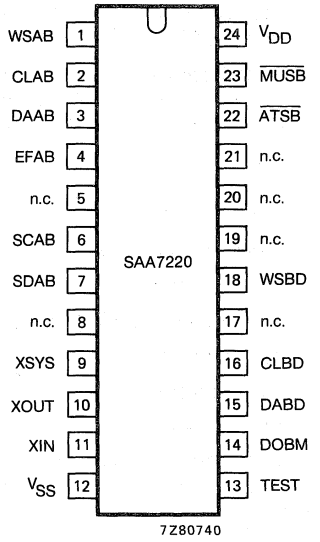


Fig. 3 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	WSAB	**Word Select:** input from A-chip.
2	CLAB	**Clock:** input from A-chip; has an internal pull-up.
3	DAAB	**Data:** input from A-chip.
4	EFAB	**Error Flag:** active HIGH input from A-chip indicating unreliable data. This input has an internal pull-down.
5	n.c.	not connected.
6	SCAB	**Subcode Clock:** a 10-bit burst clock 2,8224 MHz (typ.) input which synchronizes the subcode data. This input has an internal pull-up.
7	SDAB	**Subcode Data:** a 10-bit burst of data, including flags and sync bits serially input from the A-chip once per frame clocked by burst clock input SCAB (see Fig. 8). This input has an internal pull-down.
8	n.c.	not connected.
9	XSYS	**System clock output:** 11,2896 MHz (typ.) output to DAC and to A-chip as slave clock input.
10	XOUT	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
11	XIN	**Crystal oscillator input:** input from crystal oscillator or slave clock.

pin no.	mnemonic	description
12	V_{SS}	**Ground:** circuit earth potentional.
13	TEST	**Test input:** this input has an internal pull-down. In normal operation pin 13 should be open-circuit or connected to V_{SS}.
14	DOBM	**Digital audio output:** this output contains digital audio samples which have received interpolation, attenuation and muting plus subcode data. Transmission is by biphase-mark code.
15	DABD	**Data:** this output which is fed to the DAC, together with its clock (CLBD) and word select (WSBD) outputs, conforms to the I^2S format (see Fig. 7).
16	CLBD	**Clock:** output to DAC.
17	n.c.	not connected.
18	WSBD	**Word Select:** output to DAC.
19	n.c.	not connected.
20	n.c.	not connected.
21	n.c.	not connected.
22	$\overline{ATSB}$	**Attenuation:** when active LOW this control input provides −12 dB attenuation. This input has an internal pull-up.
23	$\overline{MUSB}$	**Mute:** active LOW control input with internal pull-up.
24	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).

FUNCTIONAL DESCRIPTION

General

The SAA7220 incorporates the following functions:

- Interpolation of data in error
- Attenuation
- Muting
- Finite impulse response transversal filtering with a four times increased sampling rate
- A digital audio output

Serial data formatted in two's complement (DAAB; pin 3) is clocked in by its bit clock (CLAB; pin 2) together with word select (WSAB; pin 1) and error flag (EFAB; pin 4) as shown in Fig. 1. After resynchronization with the internal clocks the data is separated into left and right channels and fed to two identical Input Shift Registers (IPSR). Internal timing and control loads the data into the interpolation RAM via the Intermediate Input Shift Register (IISR).

After interpolation, attenuation and muting the data is fed serially from the Intermediate Output Shift Register (IOSR) to the Audio Output Shift Register (AOSR) and to the IISR. From the IISR it is loaded into the filter RAM.

After filtering the data is passed to the Filter Data Shift Register (FDSR). From the FDSR it is transmitted serially to the data output (DABD; pin 15) together with the appropriate word select (WSBD; pin 18) and bit clock (CLBD; pin 16), in accordance with the I^2S bus specification. Data is again formatted in two's complement. Outputs DABD, WSBD and CLBD are strobed to maintain the correct timing relationship with the system clock output (XSYS) at pin 9 (see Fig. 13).

FUNCTIONAL DESCRIPTION (continued)

The subcode data (SDAB; pin 7) and 10-bit burst clock (SCAB; pin 6) are resynchronized to the internal clocks within the digital audio output block. SCAB clocks the data into the Subcode Input Shift Register (SISR; Fig. 2). Data is transferred to the Subcode Output Shift Register (SOSR) on receipt of all of the 10-bit burst clocks. The subcode data is then mixed with the data from the AOSR and the error flag to provide the output DOBM at pin 14. SISR is reset when no clocks are detected on the SCAB input.

Interpolation

When, for either left or right channel, unreliable samples are flagged between two correct samples, linear interpolation is used to replace the erroneous samples (up to a maximum of 8 consecutive errors).
When the error flag is set, the sample is replaced by a value calculated by the following formula:

$$S(n) = \frac{x}{x+1} \cdot S(n-1) + \frac{1}{x+1} \cdot S(n+x)$$

Where: S(n) = new sample value
x = number of successive erroneous samples following S (n−1)
S(n−1) = the preceding sample
S(n+x) = the first following correct sample

The value of x is detected (1 to 8) to determine the coefficients for the multiplications. Eight coefficient pairs are stored in the ROM. If x = 0 or $\geqslant$ 9 then S(n) will remain unchanged.

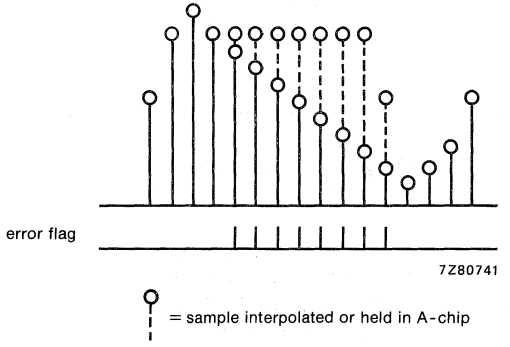


Fig. 4 Example of an eight sample linear interpolation.

Attenuation

Attenuation is controlled by the ATSB input at pin 22. When the input is active LOW the sample is multiplied by a coefficient that provides −12 dB attenuation. If the input is HIGH the multiplication factor is 1.

Mute

Mute is controlled by the MUSB input at pin 23. When the input is active LOW the value of the samples is decreased smoothly to zero following a cosine curve. 32 coefficients are used to step down the value of the data, each one being used 31 times before stepping onto the next. When MUSB is released (pin 23 HIGH) the samples are returned to the full level again following a cosine curve with the same coefficients being used in the reverse order.

Filtering

The SAA7220 incorporates two identical finite impulse response transversal filters with the equivalent of 120 taps, one filter for each stereo channel. The corresponding 120 coefficients are structured as 4 sections of 30 coefficients.
(Each ROM contains only 60 filter coefficients, the same 60 being used a second time, but in the reverse order, to make a total of 120.) Plots of the filter characteristics are shown in Fig. 16.

Data is stored in a 480-bit RAM (30 words x 16 bits). The 30 words are sequentially addressed 4 times to generate the 4 output samples.

When a new word is moved from the interpolation RAM to the filter RAM, the oldest word is discarded and all other words moved one position with respect to the ROM coefficients. The data storage effectively forms a 30 sample wide moving window on the input data. The samples move within this window at 5,6448 MHz and the window moves one sample every 22,6 μs.

An output word is formed by multiplying 30 samples from the filter RAM with 30 coefficients from the ROM using a 16 x 12 array multiplier. The result is added in an accumulator. At the end of the 30 multiplications the 16 MSB's are passed from the accumulator via the IOSR to the FDSR, and the accumulator is reset. Overflow protection is incorporated so that the output always limits cleanly in the event of accumulator overflow. Also, to simplify the design of the digital-to-analogue converter a d.c. offset of + 5% is added to the accumulator.

The filtered data is output in the I^2S format at a 5,6448 MHz bit rate and a sample rate of 176,4 kHz.

Digital audio output

Audio 16-bit samples and subcode data are formatted according to the Philips/Sony proposal; "Digital audio interface for domestic use" (Reference Philips 'Red Book' CD-DA standard specification).
The digital audio output (DOBM; pin 14) consists of 32-bit words transmitted in biphase-mark code. That is, two transitions for a logic 1 and one transition for a logic 0. The 32-bit words are transmitted in blocks of 384 words. Table 1 shows the information contained in each word.
The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns (B, M and W) indicate the following situations:

- Sync B; start of a block of 384 words, contains left sample (11101000)
- Sync M; word contains left sample, but is not a block start (11100010)
- Sync W; word contains right sample (11100100)

In the SAA7220 sync words are always preceded by 0. A typical biphase-mark code output is shown in Fig. 11.

Left and right samples are transmitted alternately.
Audio samples are available for digital audio output after interpolation, attenuation and muting, but before filtering.
Data held in the Subcode Output Shift Register (SOSR) is transmitted via the user data bit and is asynchronous with the block rate.

Digital audio output (continued)

Table 1 Composition of the 32-bit digital audio output word

bit number	description	information
1 to 4	sync	–
5 to 8	auxiliary	not used (always zero)
9 to 28	audio sample	bits 9 to 12 not used (always zero). bits 13 (LSB) to 28 (MSB) two's complement
29	audio valid	copy of the error flag
30	user data	used for subcode data
31	channel status	indication of control bits and category code
32	parity bit	even parity for all word bits excluding sync pattern

Channel status

The channel status bit is the same for both left and right words. Therefore a block of 384 words contains 192 channel status bits as shown in Table 2.

When there is no subcode the channel status will switch over to the general format. 'No subcode' is identified by the subcode detector when SCAB is a continuous HIGH or LOW.

Table 2 Channel status bit assignment

bit number	description	subcode provided	no subcode provided
1 to 4	control	copy of Q channel	bits 1 and 2 zero bit 3 image of SCAB bit 4 image of SDAB
5 to 8	reserved	always zero	always zero
9 to 16	category code	CD category bit 9 logic 1	general category all bits zero
17 to 192		always zero	always zero

If a subcode clock is provided but there is no subcode data (SDAB is a continuous HIGH or LOW) the control bits will be zero and the category code will be CD.

The SYNC bit and the cyclic redundancy check bit (CRC) in the subcode data from the A-chip to the B-chip have the format shown by Fig. 5. Typical subcode data input waveforms are shown by Fig. 8.

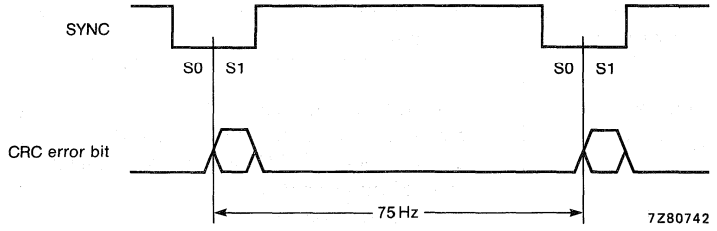


Fig. 5 Subcode data format for SYNC and CRC bits.

SYNC is active LOW and indicates the start of a subcode block, which contains 98 words including 2 sync words, S0 and S1.
CRC is always LOW except during SYNC S1 when:

- CRC = logic 1; previous Q block was true
- CRC = logic 0; previous Q block was false

Two 32-bit words are transmitted at the sample frequency of 44,1 kHz (2 x 32 x 44,1 kHz = 2,8224 Mbits/s data rate). An internal 5,6448 MHz clock (XSYS/2) is used in the biphase modulator.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0,5	–	+ 7,0	V
Maximum input voltage range	V_I	−0,5	–	V_{DD} + 0,5	V
Storage temperature range	T_{stg}	−55	–	+ 125	°C
Operating temperature range	T_{amb}	−20	–	+ 70	°C
Electrostatic handling*	V_{es}	−1000	–	+ 1000	V

Ensure no electrical connections are made to the underside or ends of the package as there is the possibility of making accidental connection to the lead frame and/or internal heat spreader of the device.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 24)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 24)	I_{DD}	100	180	285	mA
Inputs					
WSAB, DAAB					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
EFAB, SDAB (note 2)					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 50	μA
Input capacitance	C_I	–	–	7	pF
CLAB, SCAB, $\overline{ATSB}$, $\overline{MUSB}$ (note 3)					
Input voltage LOW (note 1)	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (note 1)	V_{IH}	2,0	–	V_{DD}+0,5	V
Input leakage current					
at V_I = 0 V	I_{LI}	−30	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA
Input capacitance	C_I	–	–	7	pF
Crystal oscillator (see Fig. 9)					
Input XIN					
Output XOUT (note 4)					
Mutual conductance at 100 kHz	G_m	1,5	–	–	mA/V
Small signal voltage gain ($A_v = G_m \times R_O$)	A_v	3,5	–	–	V/V
Input capacitance	C_I	–	–	10	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Output capacitance	C_O	–	–	10	pF
Input leakage current					
at V_I = 0 V	I_{LI}	−10	–	–	μA
at V_I = V_{DD}	I_{LI}	–	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
Slave clock mode					
Input voltage (note 5) (peak-to-peak value)	$V_{I(p-p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW (note 6)	V_{IL}	0	–	1	V
Input voltage HIGH (note 6)	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 7)	t_r	–	–	20	ns
Input fall time (note 7)	t_f	–	–	20	ns
Input HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%
Outputs (note 4)					
DABD, CLBD, WSBD					
Output voltage LOW at I_{OL} = 0,8 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at $-I_{OH}$ = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
XSYS (note 8)					
Output voltage LOW	V_{OL}	0	–	0,4	V
Output voltage HIGH	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
DOBM					
Voltage across a 75 Ω load via attenuator; see Fig. 10 (peak-to-peak value)	$V_{L(p-p)}$	0,4	–	0,6	V
D.C. offset voltage	V_{LDC}	–0,05	–	+ 0,05	V
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Inputs (see Fig. 12)					
SCAB, CLAB (note 9)					
SCAB clock frequency (burst clock)	f_{SCAB}	–	2,8224	–	MHz
CLAB clock frequency	f_{CLAB}	–	2,8224	–	MHz
or (note 10)	f_{CLAB}	–	1,4112	–	MHz
Clock LOW time	t_{CKL}	110	–	–	ns
Clock HIGH time	t_{CKH}	110	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
DAAB, WSAB, EFAB (note 11)					
Data set-up time	$t_{SU;DAT}$	40	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
SDAB (note 12)					
Subcode data set-up time	$t_{SU;SDAT}$	40	–	–	ns
Subcode data hold time	$t_{HD;SDAT}$	0	–	–	ns
Input rise time	t_r	–	–	20	ns
Input fall time	t_f	–	–	20	ns
Outputs (see Figs 13 and 14)					
WSBD (notes 9 and 13)					
Word select set-up time	$t_{SU;WS}$	40	–	–	ns
Word select hold time	$t_{HD;WS}$	0	–	–	ns
WSBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 13)					
Data set-up time	$t_{SU;DATD}$	40	–	–	ns
Data hold time	$t_{HD;DATD}$	0	–	–	ns
DABD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
CLBD (notes 9 and 13)					
Clock period	t_{CK}	161	177	197	ns
Clock LOW time	t_{CKL}	65	–	–	ns
Clock HIGH time	t_{CKH}	65	–	–	ns
Clock set-up time	$t_{SU;CLD}$	40	–	–	ns
Clock hold time	$t_{HD;CLD}$	0	–	–	ns
CLBD (note 9)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DABD (notes 9 and 14)					
Data set-up time	$t_{SU;DATBD}$	40	–	–	ns
Data hold time	$t_{HD;DATBD}$	60	–	–	ns

parameter	symbol	min.	typ.	max.	unit
Outputs (continued)					
WSBD (notes 9 and 14)					
Word select set-up time	$t_{SU;DATWSD}$	40	–	–	ns
Word select hold time	$t_{HD;DATWSD}$	60	–	–	ns
DOBM (note 15)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Data bit 0 (note 16)					
pulse width HIGH	$t_{HIGH(0)}$	336	354	372	ns
pulse width LOW	$t_{LOW(0)}$	336	354	372	ns
Data bit 1 (note 17)					
pulse width HIGH	$t_{HIGH(1)}$	172	177	182	ns
pulse width LOW	$t_{LOW(1)}$	172	177	182	ns
XSYS					
Output rise time (note 9)	t_r	–	–	20	ns
Output fall time (note 9)	t_f	–	–	20	ns
Output HIGH time at 2 V (relative to clock period)	t_{HIGH}	35	–	65	%

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

A Philips publication "I²S bus specification" is available on request.

Notes to the characteristics

1. Minimum V_{IL} and maximum V_{IH} are peak values to allow for transients.
2. Inputs EFAB and SDAB both have internal pull-downs.
3. Inputs CLAB, SCAB, $\overline{ATSB}$ and $\overline{MUSB}$ have internal pull-ups.
4. All outputs are short-circuit protected except crystal oscillator output.
5. If used in a.c. coupled mode.
6. $V_{IH} - V_{IL} \geqslant 1{,}6$ V.
7. Reference levels = 10% and 90%.
8. The output current conditions are dependent on the drive conditions. When a crystal oscillator is being used the output current capability is $I_{OL} = +0{,}8$ mA; $I_{OH} = -0{,}2$ mA. But if a slave input is being used the output currents are reduced to $I_{OL} = +0{,}2$ mA; $I_{OH} = -0{,}2$ mA.
9. Reference levels = 0,8 V and 2,0 V.
10. The signal CLAB can run at either 2,8 MHz (1/4 system clock) or 1,4 MHz (1/8 system clock) under typical conditions. It does not have a minimum or maximum frequency, but is limited to being 1/4 or 1/8 of the system clock frequency.
11. Input set-up and hold times measured with respect to clock input from A-chip (CLAB). Reference levels = 0,8 V and 2,0 V.
12. Input set-up and hold times measured with respect to subcode burst clock input from A-chip (SCAB). Reference levels = 0,8 V and 2,0 V.
13. Output set-up and hold times measured with respect to system clock output (XSYS).
14. Output set-up and hold times measured with respect to clock output (CLBD).
15. Output rise and fall times measured between the 10% and 90% levels; the data bit pulse width measured at the 50% level.
16. Data bit 0 pulse width times are typically system clock period ($1/f_{XTAL}$) x 4. Maximum and minimum values are ± 5% of this time. Values shown are for f_{XTAL} = 11,2896 MHz, but these will change accordingly if f_{XTAL} changes.
17. Data bit 1 pulse width times are typically system clock period ($1/f_{XTAL}$) x 2. Maximum and minimum values are ± 2,5% of this time. Values shown are for f_{XTAL} = 11,2896 MHz, but these will change accordingly if f_{XTAL} changes.

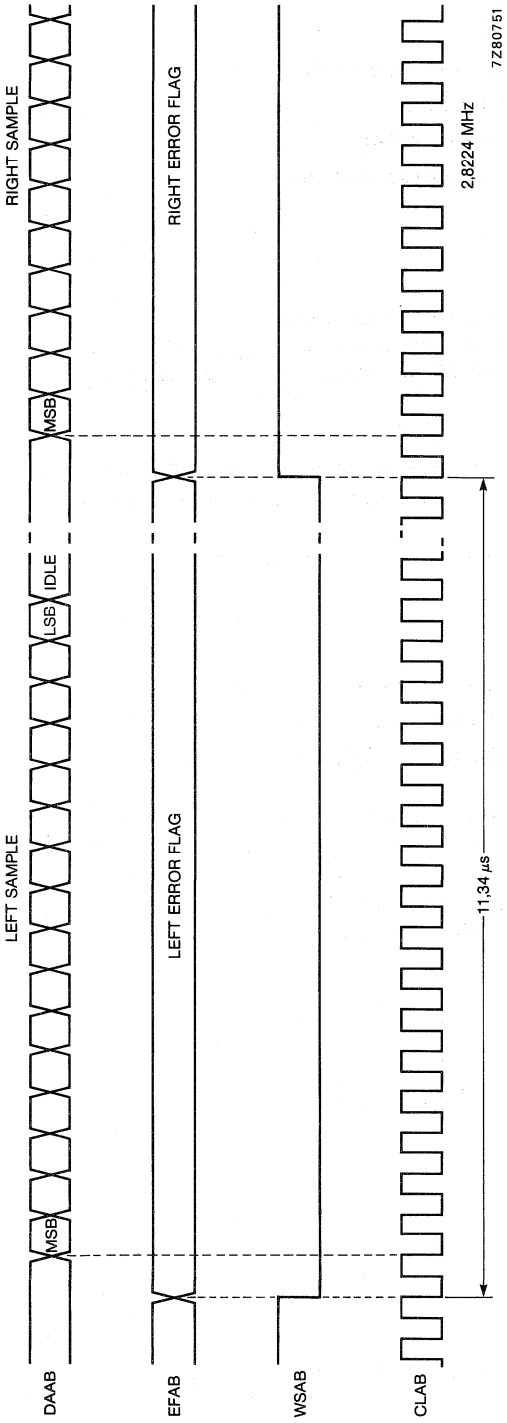


Fig. 6(a) Typical sample data input waveforms from A-chip at 2,8 MHz.

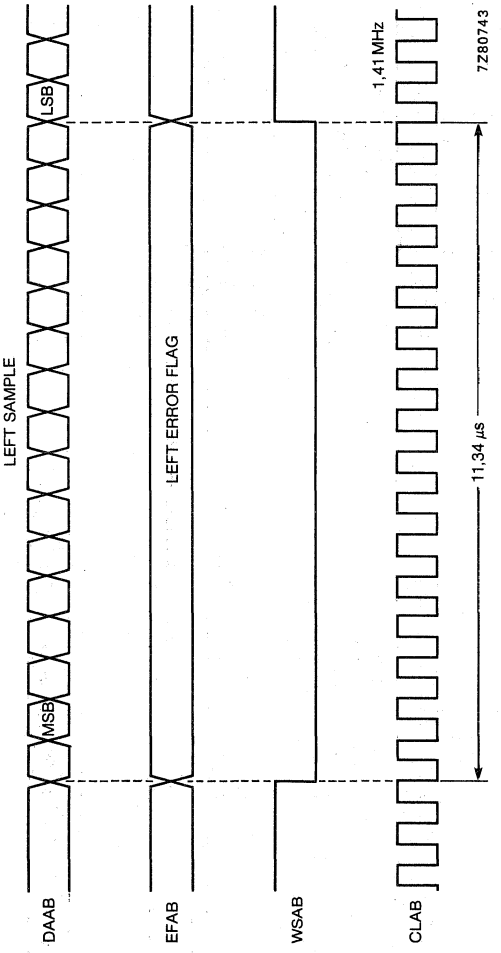


Fig. 6(b) Typical sample data input waveforms at 1,4 MHz.

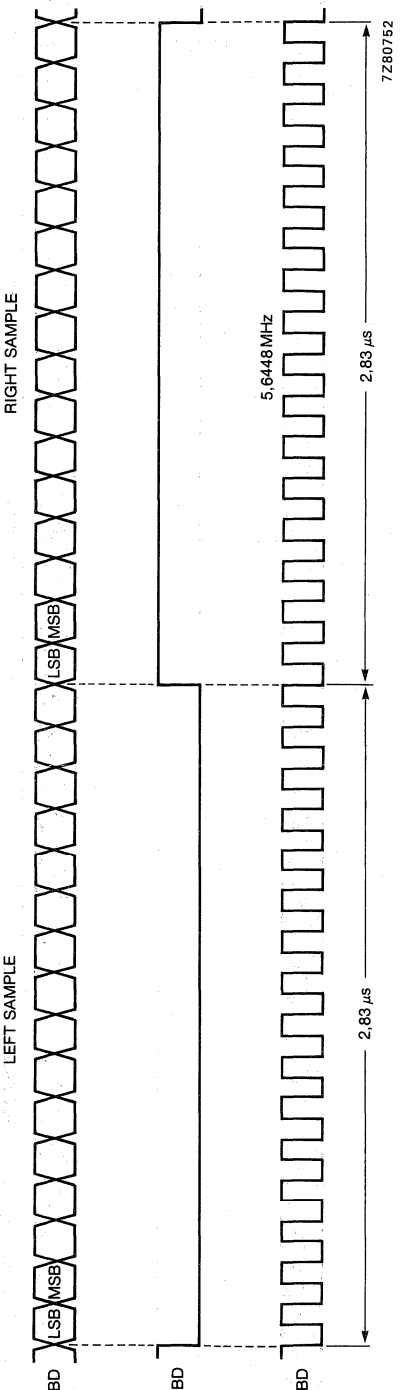
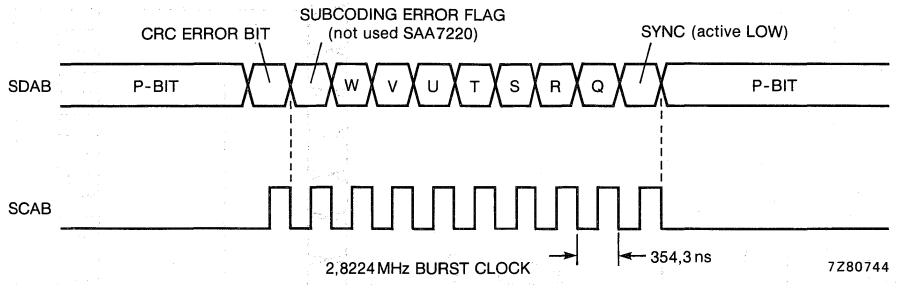
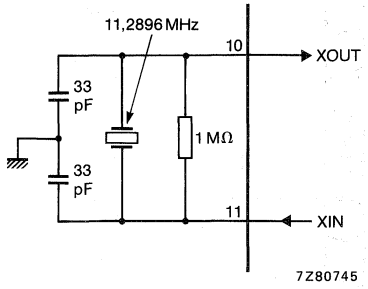


Fig. 7 Typical sample data output waveforms to DAC.



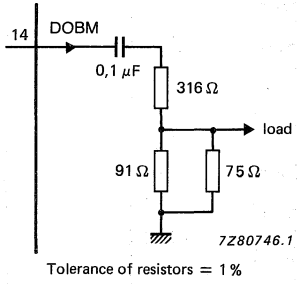
Subcode word frequency = 7,35 kHz.

Fig. 8 Typical subcode data input waveforms.



Oscillator catalogue no. 4322 143 05031

Fig. 9 Crystal oscillator circuit.



Tolerance of resistors = 1%

Fig. 10 Digital audio output load.

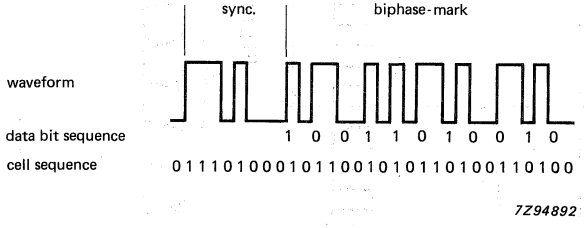


Fig. 11 Biphase-mark code.

TIMING

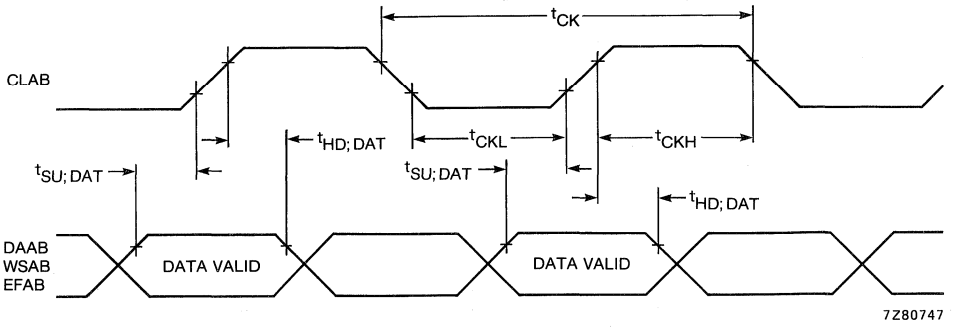


Fig. 12 Data input timings; reference levels = 0,8 V and 2,0 V.
(also applicable to subcode data input ($t_{SU;SDAT}$ and $t_{HD;SDAT}$).

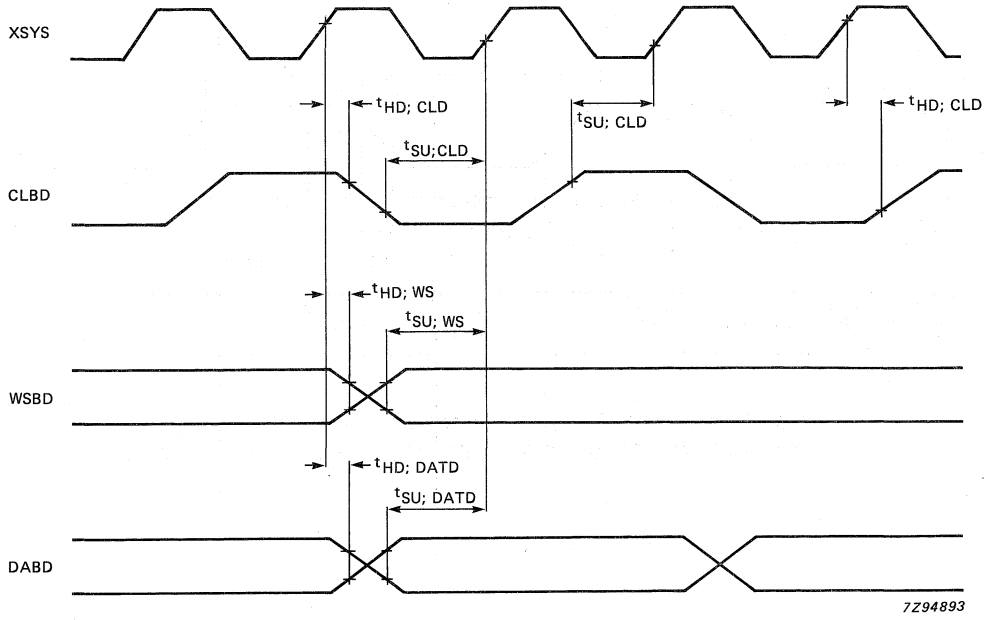


Fig. 13 Data output timings with respect to system clock output (XSYS); reference levels = 0,8 V and 2,0 V.

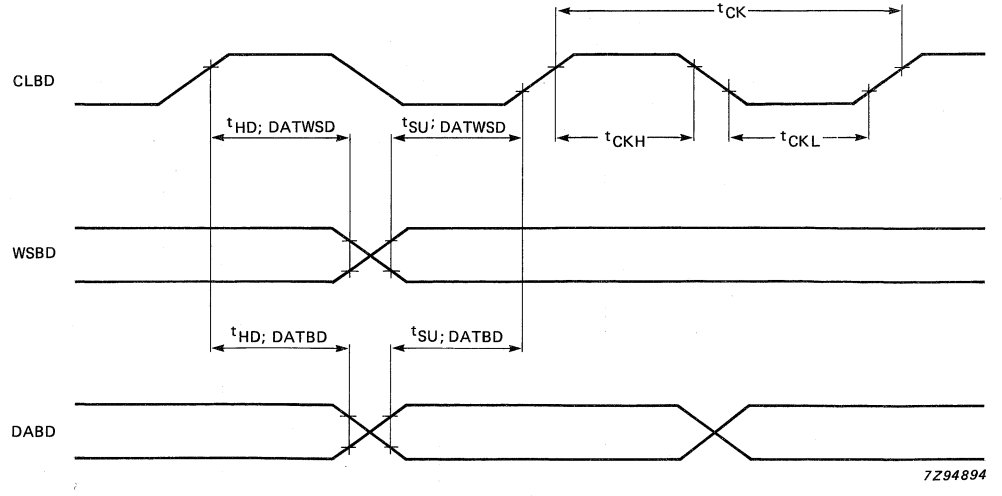


Fig. 14 Data output timings with respect to clock output (CLBD); reference levels = 0,8 V and 2,0 V.

APPLICATION INFORMATION

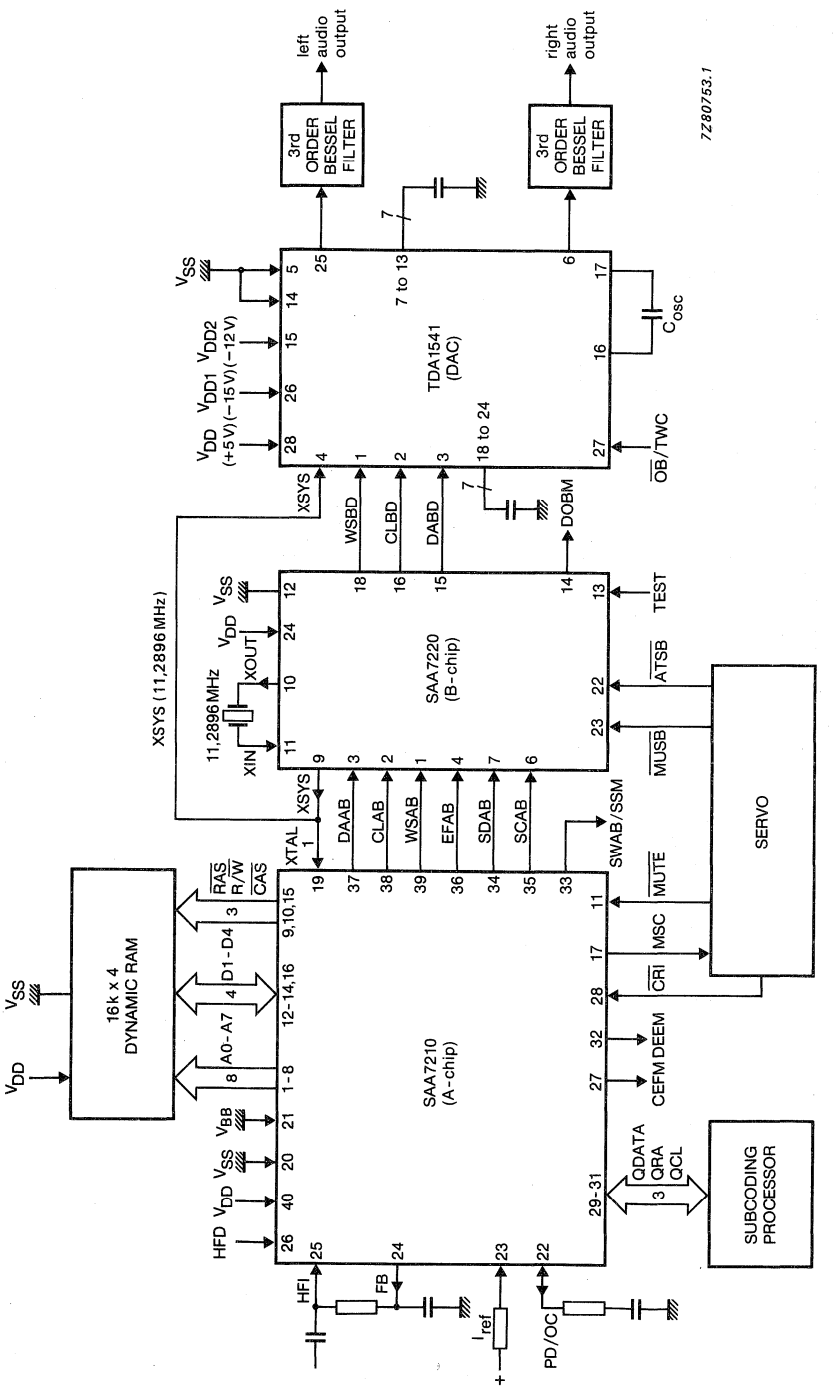
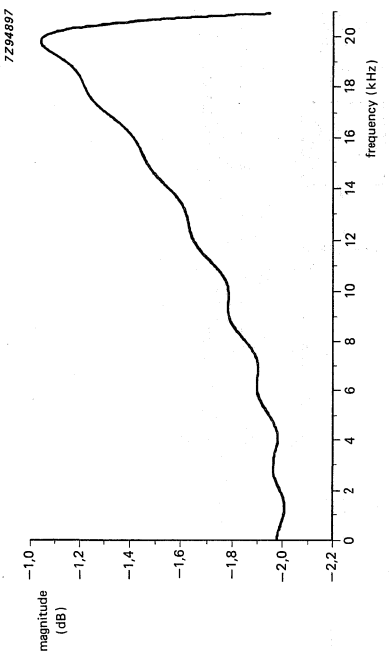
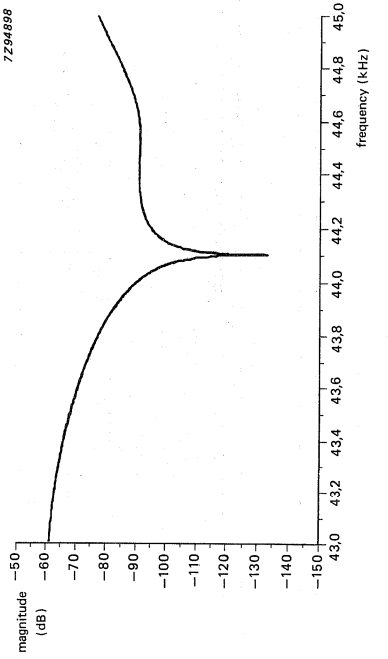
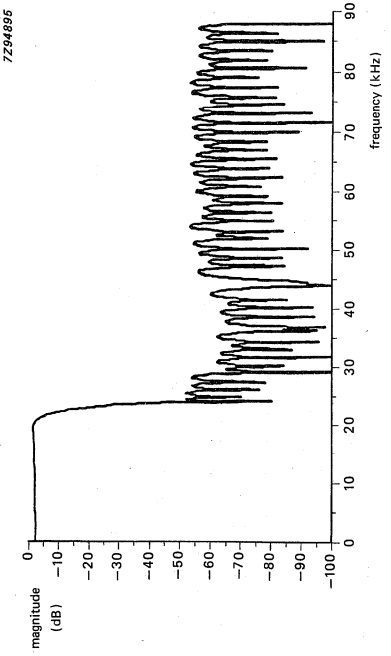


Fig. 15 System application diagram.







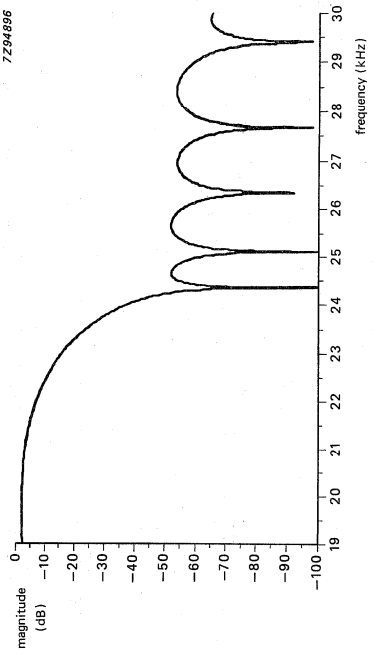


Fig. 16 Digital filter characteristics; magnitude as a function of frequency.

AUDIO DIGITAL INPUT CIRCUIT (ADIC)

GENERAL DESCRIPTION

The SAA7274 is an Audio Digital Input Circuit (ADIC) which converts digital audio signals in accordance with the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 into an equivalent binary value of data and control bits. The output function of this device is to convert the equivalent binary value of the data bits (for each channel) into a serial digital audio signal which conforms to the I²S format.

Features

- I²S bus output
- Biphase audio signal (Satellite radio, compact disc and DAT)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_{DD}	4.5	–	5.5	V
Inputs	except IBIFA					
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	V_I = 0 V	$-I_I$	–	–	1	μA
	V_I = 5.5 V	I_I	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
Output voltage HIGH		V_{OH}	V_{DD}–0.5	–	–	V
Output voltage LOW		V_{OL}	–	–	0.4	V
Operating ambient temperature range		T_{amb}	–40	–	+70	°C

PACKAGE OUTLINES

SAA7274P: 24-lead DIL; plastic (SOT101A).
SAA7274T: 24-lead mini-pack; plastic (SO24; SOT137A).

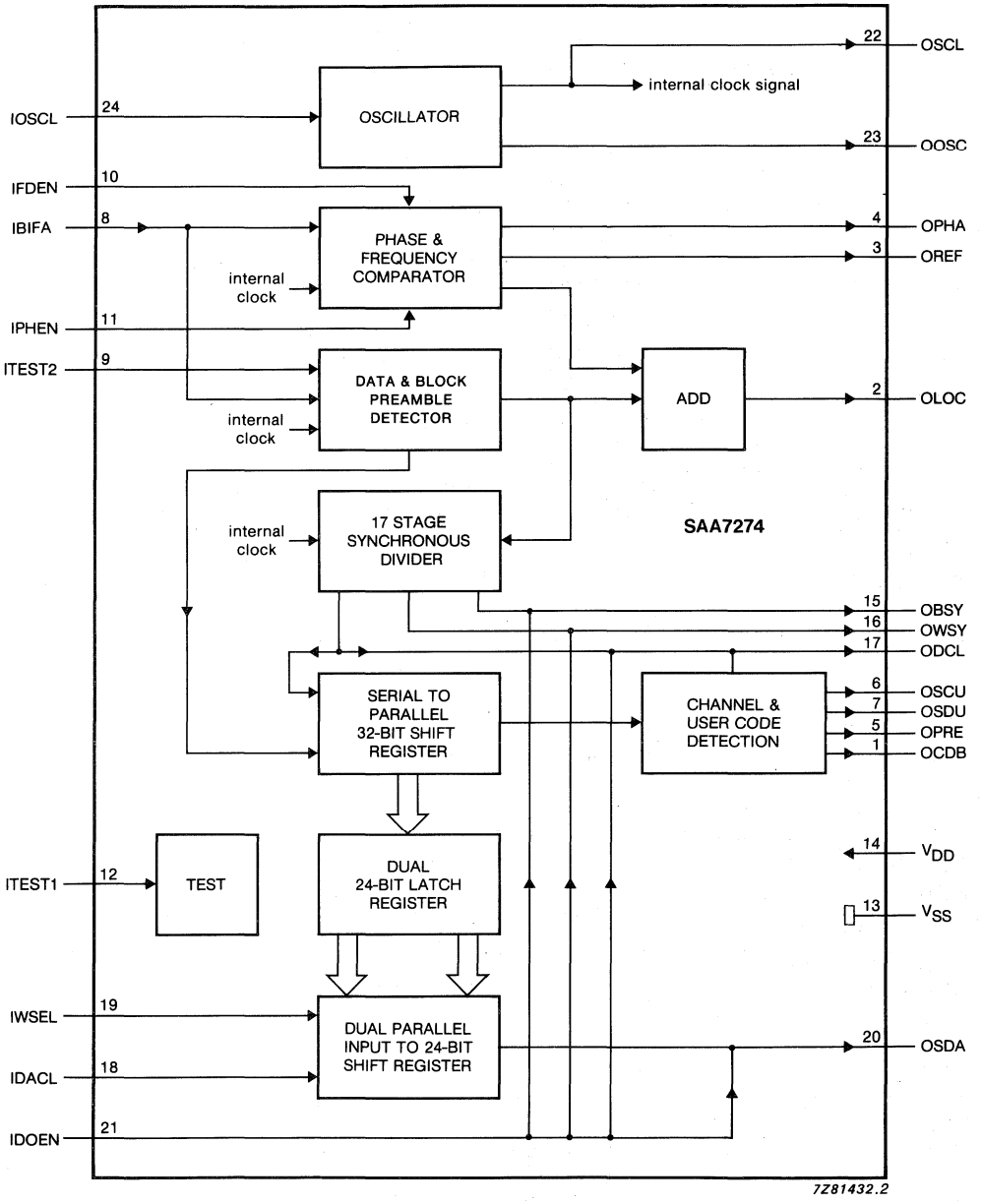


Fig.1 Block diagram.

PINNING

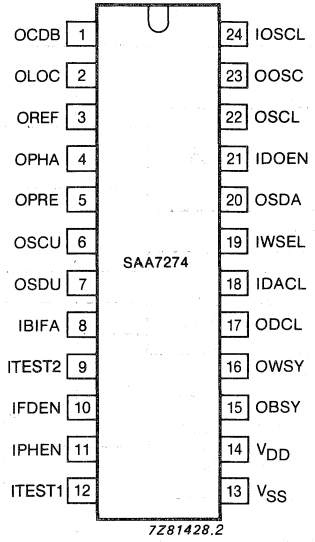


Fig.2 Pinning diagram.

Power supply

V_{DD}	positive supply voltage (5 V)
V_{SS}	ground (0 V)

Inputs (CMOS protection)

IBIFA	biphase input signal (min. 1 MHz; max. 3.1 MHz)
IFDEN	frequency detector enable
IPHEN	phase-locked loop edge selector
ITEST1	test input enable
ITEST2	test input enable
IDACL	data clock input signal (max. 5 MHz)
IWSEL	word select input signal (max. 50 kHz)
IDOEN	output enable
IOSCL	clock oscillator input (min. 8 MHz; max. 12.5 MHz)

Outputs (CMOS push-pull)

OCDB	control data bits (max. 400 kHz)
OLOC	out-of-lock signal
OREF	phase reference signal (max. 6.2 MHz)
OPHA	phase output signal (max. 6.2 MHz)
OPRE	pre-emphasis level
OSCU	user clock/copy-bit signal (max. 3.1 MHz)
OSDU	user data/pre-emphasis (max. 3.1 MHz)
OSCL	system clock output (min. 8 MHz; max. 12.5 MHz)
OOSC	clock oscillator output (min. 8 MHz; max. 12.5 MHz)

Outputs (3-state push-pull)

OBSY	block synchronization output signal (1/49152 system clock)
OWSY	word clock output signal (1/256 system clock)
ODCL	data clock output signal (1/4 system clock)
OSDA	data output signal (max. 2.5 MHz)

FUNCTIONAL DESCRIPTION

Main function

The biphase input signal must conform to the IEC/EBU standards, IEC tech. com. No. 84, secr. 50, Jan. 1987 format, as well as satisfying the following conditions:

- number of channels: 2
- transmission code: biphase mark
- synchronization method: biphase violation
- number of data bits: 24, starting with the LSB
- number of control bits: 4
- preamble values:

preceding cell	0	1
block preamble	11101000	00010111

The main function performs the following tasks:

- Provides the output function with the equivalent binary value of the data bits separately for each of the two channels. These values are available until new information is received.
- Generates an out-of-lock output signal (OLOC) which is HIGH when the frequency of the biphase input signal is equal to 1/4 of the system clock frequency and when the block preambles are detected in the biphase input signal.
- If the biphase input signal is not present after 32 clock pulses and also whenever the biphase input signal and IOSCL/4 drift away from each other by more than 32 clock pulses, then the output OSCU is forced HIGH and output OSDU, OPRE, OLOC, OCDB and OSDA are forced LOW.
- Generates a data clock output signal (ODCL) with a frequency of 1/4 of the system clock. When a block preamble is detected in the biphase input signal ODCL is synchronized to a LOW value.
- Generates a word clock output signal (OWSY) with a frequency of 1/256 of the system clock. When a block preamble is detected in the biphase input signal OWSY is synchronized to a LOW value.
- Generates a block synchronization output signal (OBSY). This signal is HIGH during 4 system clock periods and has a frequency of 1/49152 of the system clock. The signal is synchronized with the block preambles of the biphase input signal.
- Generates a phase output signal (OPHA) and a phase reference signal (OREF). If the frequency of the biphase input signal (IBIFA) equals 1/4 of the system clock frequency ($f_{IOSCL}/4$) then the IC generates OPHA and OREF as shown in Fig.3.
  If the frequency of the biphase input signal (IBIFA) is greater or less than 1/4 of the system clock frequency then the IC generates OPHA and OREF as shown in Fig.4.

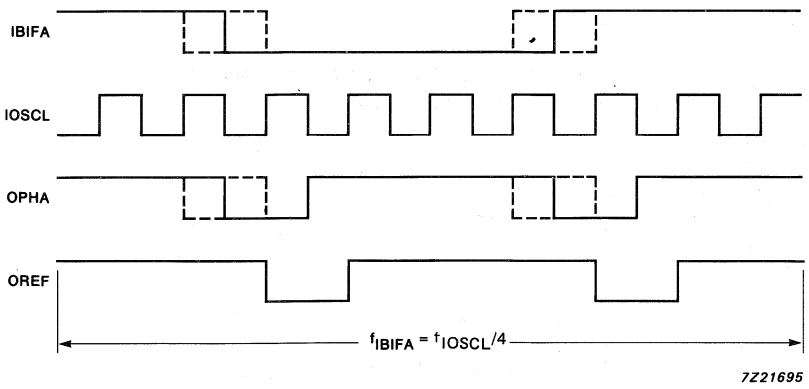


Fig.3 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} = f_{IOSCL}/4$.

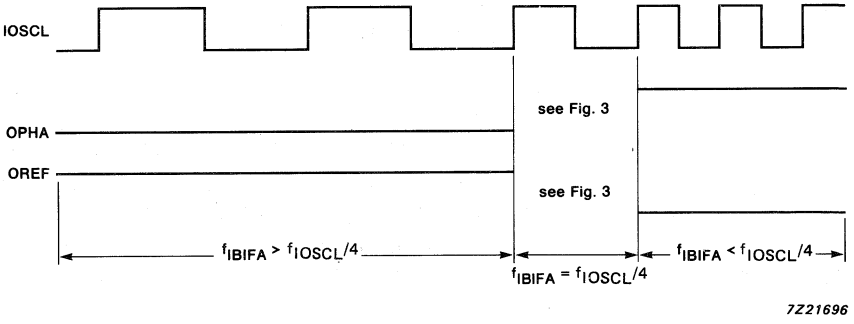


Fig.4 Generation of phase output signal (OPHA) and phase reference signal (OREF); $f_{IBIFA} \neq f_{IOSCL}/4$.

Output function

The output function performs the following tasks:

- Provides the data output (OSDA) with the data bits from each channel in the following order:

MSB . . . . . LSB 0 0 0 0 0 0 0 0

- Outputs the data of the right and left channel. When word select input signal (IWSEL) is HIGH the data of the right channel is output and when LOW the data of the left channel is output.
- Delivers serial data to the OSDA output, if IDOEN = HIGH. This occurs on each negative transition of the data clock input signal (IDACL). Following a status change at the word select input (IWSEL), the data (MSB first) is output on the first negative transition of IDACL. If the number of clock pulses in a word exceeds 24, then the following bits will be internally set to zero.

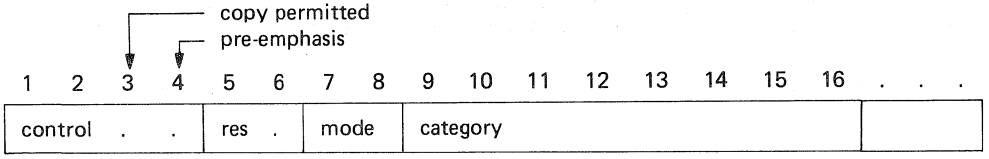
FUNCTIONAL DESCRIPTION (continued)

- Generates the following subcodes:

  series 1, 0 0 U1 T1 S1 R1 Q1 1 0 0
  series 2, CRC 0 V1 U1 T1 S1 R1 Q1 1 0
  series 3, 0 0 W1 V1 U1 T1 S1 R1 Q1 1
  and after receiving the next user byte:
  series 4, 0 0 W2 V2 U2 T2 S2 R2 Q2 1 etc.

- If the value of the category bits, bits 9 to 16 of the input signal, = 10000000 (compact disc format) and the value of the mode bits, bits 7 and 8, = 00, the user data output (OSDU) will deliver the bits of the subcode following the specified lay-out (above). The subcode starts only after receipt of at least 16 zero bits. Simultaneously a user clock signal (OSCU) consisting of 10 clock pulses is present. The output signal starts when a subcode is completed and is clocked on the negative transition of OSCU. The first data word of each subcode frame is output 3 times in succession with the data pattern shifted each time as outlined for series 1 through series 3 in the layout given above. The CRC performs a check on the 96 Q bits of the preceding subcode. If CRC is correct then the CRC bit = 1.

- Channel status:



  If the value of the category bits **does not** equal 10000000 (compact disc format) and the value of the mode bits equals 00 (mode 0), then:

  output OSDU indicates the status of bit 4 (pre-emphasis) of the channel status and output OSCU indicates the status of bit 3 (copy permitted) of the channel status provided the control bits conform to the 2-channel audio signal format.

- Uses the output pre-emphasis (OPRE) to indicate the status of bit 4 of the channel status for a 2-channel audio signal.

- Outputs the 4 control bits of the biphase input signal (IBIFA) represented by V, U, C and P at OCDB. The output delivers the bits in the same sequence during the next word, each bit continues for 32 clock pulses.

Additional input and output signals

The following input and output signals are available from this circuit:

- Phase output signal (OPHA) and phase reference signal (OREF) for use in a phase-locked loop (PLL). The OPHA signal is a result of the difference between the frequency and phase of the biphase input signal and the system clock. OREF signal provides the reference signal for the PLL.
- Input signal IFDEN enables the frequency detector. The frequency detection as present in the 2 signals OPHA and OREF can be enabled by making this signal LOW.
- Data clock output signal (ODCL), which has a frequency of 1/4 of the system clock frequency.
- Word clock output signal (OWSY), which has a frequency of 1/256 of the system clock frequency.
- Block synchronization output signal (OBSY), which has a frequency of 1/49152 of the system clock.
- ODCL, OWSY and OBSY will be synchronized to the block preambles in the biphase input signal IBIFA.

- Outputs ODCL, OWSY, OBSY and OSDA are enabled via a 3-state mode with a HIGH level on input IDOEN.
- IPHEN input selects dual or single edge detection of the input signal IBIFA in the phase detector. A low level selects the single-edge detection mode.
- Out-of-lock signal (OLOC). This output is continuously LOW or random HIGH/LOW if the PLL is out-of-lock, or no block preambles and present in the biphase input signal IBIFA. It is continuously HIGH if the PLL is in lock.
- User data/pre-emphasis output signal (OSDU). After receiving a category code of mode 0 from a non-compact disc source this signal outputs the pre-emphasis bit of the channel status bits in the biphase input signal. If the category code of mode 0 is from a compact disc source then the user data bits from the subcode channel including the CRC check on the 96 preceding Q bits are output.
- User clock/copy bit output signal (OSCU). After receiving a category code of mode 0 from a non-compact disc source then the copy bit of the channel status bits in the biphase input signal is output. If the category code of mode 0 is from a compact disc source then 10 clock pulses for the 'user data' are output.
- Pre-emphasis level output signal (OPRE), which indicates the value of the pre-emphasis bit of the channel status bits after receiving the two-channel audio fromat in the biphase input signal (IBIFA).
- Control data bits output signal (OCDB), which contains the 4 control bits of each word of the biphase input signal.
- The inputs ITEST1 and ITEST2 are used for device tests at the factory only, for normal operation they have to be connected to V_{SS}.

Clock oscillator

The clock oscillator of the circuit can be formed by connecting a crystal or a ceramic resonator between the oscillator input and output pins.

The circuit can also be driven by an external signal source applied to the oscillator input. The oscillator output is buffered and available at pin OSCL. The internal circuitry is driven via an inverter, which is connected to the output OSCL. This allows all the output signals (especially ODCL, OWSY and OBSY) to change their state after a pulse from OSCL, independent of the capacitive load of the OSCL pin. All output signals of the circuit are triggered on the positive transition of the OSCL signal.

Application note

If the capacitive load is higher than specified in **AC CHARACTERISTICS**, a buffer circuit can be used. A suitable device is the PC74HC126 (3-state quad buffer/line driver). The input IDOEN to the SAA7274 must be made HIGH and the original 3-state enable signal must be connected to the OE inputs of the PC74HC126 (pins 1, 4, 10 and 13). Because the capacitive load of the SAA7274 is very low, the loss of speed is limited.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0.5	7.0	V
Input voltage	note 1	V_I	−0.5	V_{DD}+0.5	V
Maximum input current		I_{IM}	−	±10	mA
Maximum output current		I_{OM}	−	±10	mA
Maximum supply current		I_{SS}, I_{DD}	−	±50	mA
Total power dissipation		P_{tot}	−	500	mW
Storage temperature range		T_{stg}	−55	+150	°C
Operating ambient temperature range		T_{amb}	−40	+70	°C

Note

1. Input voltage should not exceed 7 V.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = −40 to + 70 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply current	note 1	I_{DD}	–	–	250	μA
	note 2	I_{DD}	–	10	–	mA
Inputs						
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	V_{DD}	V
Input voltage LOW		V_{IL}	0	–	0.3 V_{DD}	V
Input current	$V_{SS} \leqslant V_I \leqslant V_{DD}$	$\pm I_I$	–	–	1	μA
Input capacitance		C_I	–	4	6	pF
Outputs						
OSCL						
Output voltage HIGH	$-I_{OH}$ = 8 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 8 mA	V_{OL}	–	–	0.4	V
OCDB, OLOC, OREF, OPHA, OPRE, OSCU, OSDU, OSDA						
Output voltage HIGH	$-I_{OH}$ = 2 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 2 mA	V_{OL}	–	–	0.4	V
OBSY, OWSY, ODCL, OOSC						
Output voltage HIGH	$-I_{OH}$ = 1.5 mA	V_{OH}	V_{DD}−0.5	–	–	V
Output voltage LOW	I_{OL} = 1.5 mA	V_{OL}	–	–	0.4	V
OSDA, ODCL, OWSY, OBSY						
Output leakage current	3-state	$\|I_{LO}\|$	–	–	15	μA

Notes to the DC characteristics

1. All inputs at V_{DD} or V_{SS}, except ITEST2 on V_{SS}, all outputs open circuit.
2. f_{OSCL} = 11.3 MHz.

AC CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V.
T_{amb} = −40 to + 70 °C.
Load capacitance (C_L): OSCL = 50 pF; OWSY, ODCL and OSDA = 30 pF (see application note); all other outputs = 20 pF.
Clock frequency $f_{IOSCL} = \leqslant 12.5$ MHz.
IOSCL timing pulse LOW, $t_{LOW} \geqslant 37$ ns; rise and fall times t_r and $t_f = \leqslant 10$ ns.
Delay times are specified from clock input = 50% V_{DD} to output = 50% V_{DD}; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Set-up and hold times						
IWSEL to IDACL	see Fig.5					
Data set-up time		t_{SU}	1	–	–	*
Data hold time		t_{HD}	–	–	1	*
Propagation delays						
IOSCL to OSCL		t_p	–	–	25	ns
IDACL to OSDA		t_p	–	–	60	ns
OSCL to OWSY and ODCL		t_p	5	–	50	ns
Rise and fall times						
OSCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	10	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	15	ns
OWSY and ODCL						
Rise and fall time	TTL levels = 0.4 to 2 V	t_r, t_f	–	–	15	ns
Rise and fall time	CMOS levels = 10 to 90% V_{DD}	t_r, t_f	–	–	25	ns

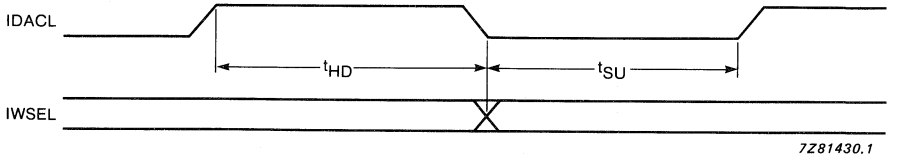
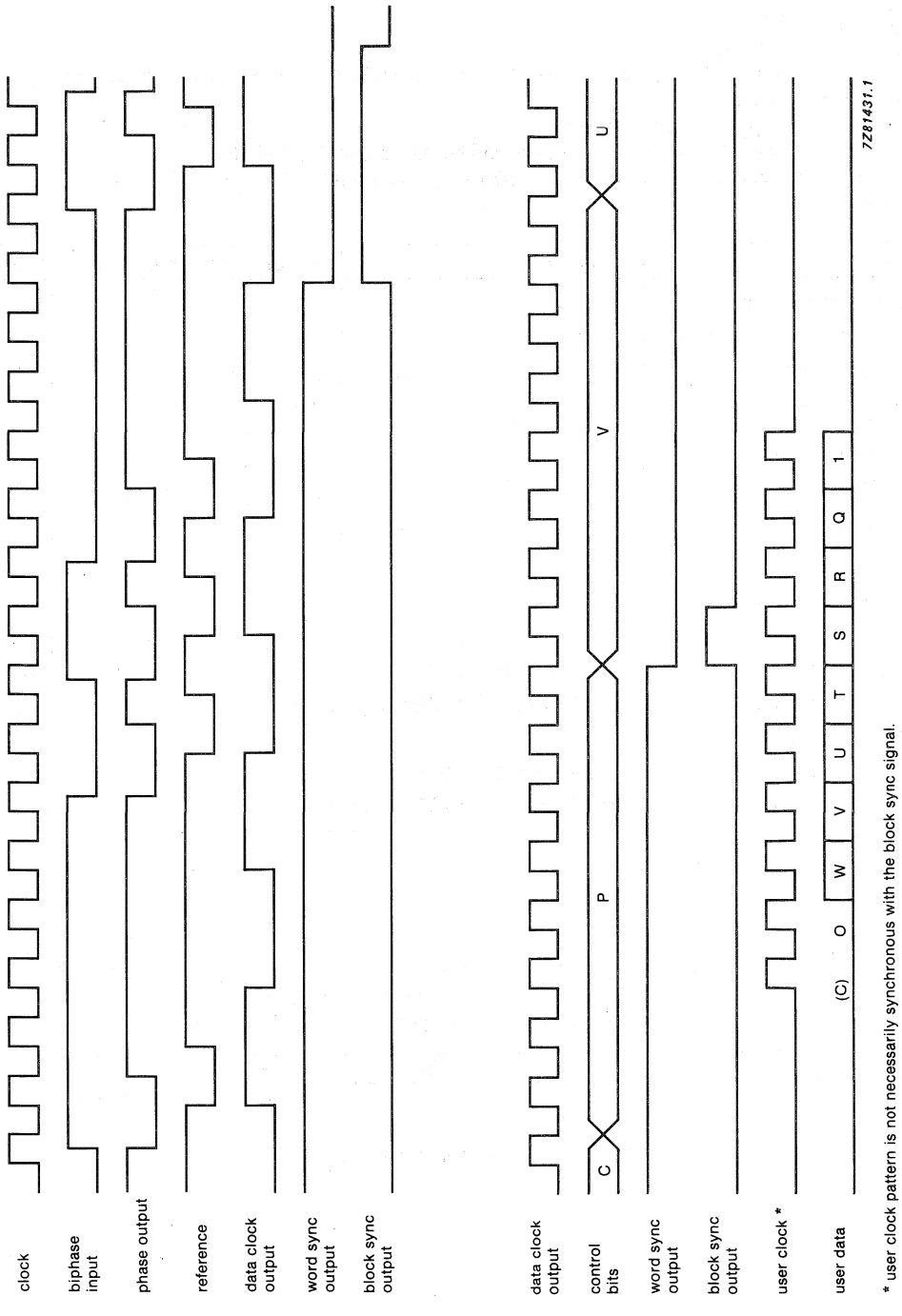


Fig.5 Set-up and hold time diagram.

* Clock periods of OSCL.



* user clock pattern is not necessarily synchronous with the block sync signal.

Fig.6 Timing diagram.

CMOS DECODER FOR COMPACT DISC SYSTEMS

GENERAL DESCRIPTION

The SAA7310 (CD3A) incorporates the functions of demodulator, subcoding processor, motor speed control, error corrector and concealment in one CMOS chip. The device accepts data from the disc and outputs serial data via the Inter IC signal bus (I^2S) directly to a digital-to-analogue converter (such as the stereo CMOS dual DAC; SAA7320). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering. The SAA7310 is available in both 40-pin DIL and 44-pin QFP packages.

Features

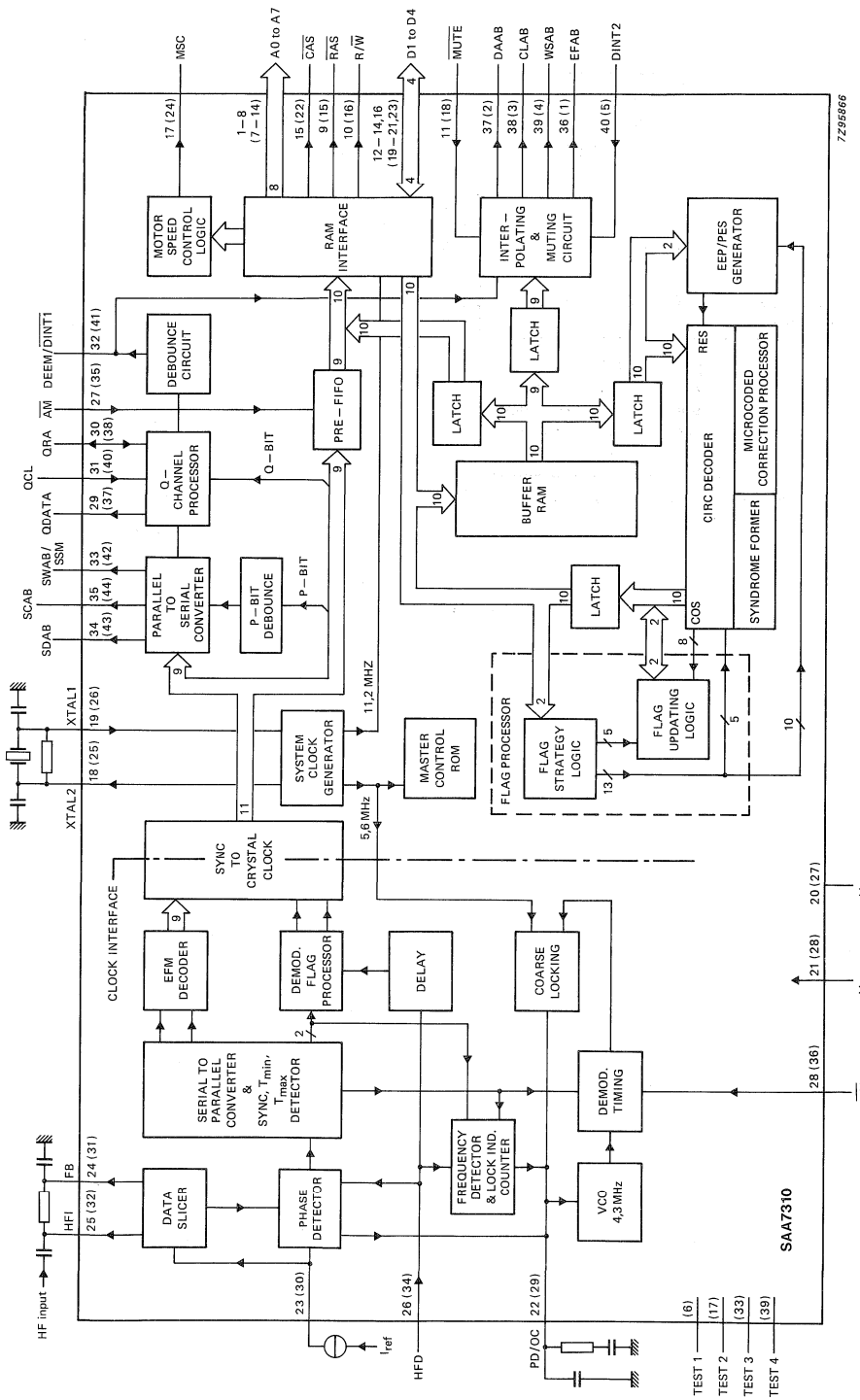
- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Adaptive CIRC error correction enabling 4 erroneous symbols per frame (32 symbols) to be corrected
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange
- Bidirectional data bus to external RAM (16 K x 4 bits) with 64-frame FIFO capacity
- Demodulator PLL requiring virtually no peripheral components
- Replacement for the CD2A
- Low power consumption (typ. 175 mW)
- Track loss correction by additional muting
- Non-digital audio interface application (such as CD-ROM or CD-I)
- 2-package option
- −40 to +85 °C operating temperature range

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	35	50	mA
Data slicer input voltage (peak-to-peak value)	$V_{I(p-p)}$	0,5	–	2,5	V
Oscillator operating frequency					
XTAL	f_{XTAL}	10,16	11,2896	12,42	MHz
VCO (PLL locked on to data)	f_{VCO1}	2,54	4,3218	6,21	MHz
Output current (each output)	I_O	−10	–	+ 10	mA
Operating ambient temperature	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINES

SAA7310P : 40-lead DIL; plastic (SOT-129).
SAA7310GP : 44-lead QFP; plastic (SOT-205A).



Pins in parenthesis relate to 44-pin QFP package.

Fig. 1 Block diagram.

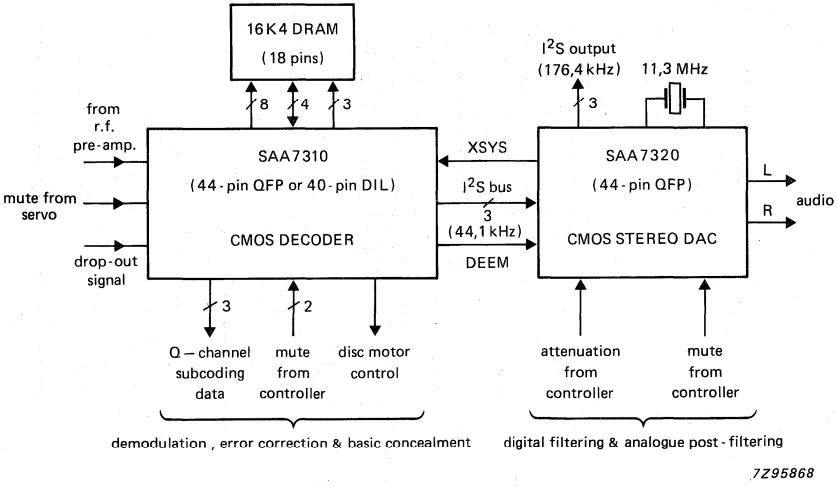


Fig. 2 (a) Block diagram of SAA7310 as used with SAA7320.

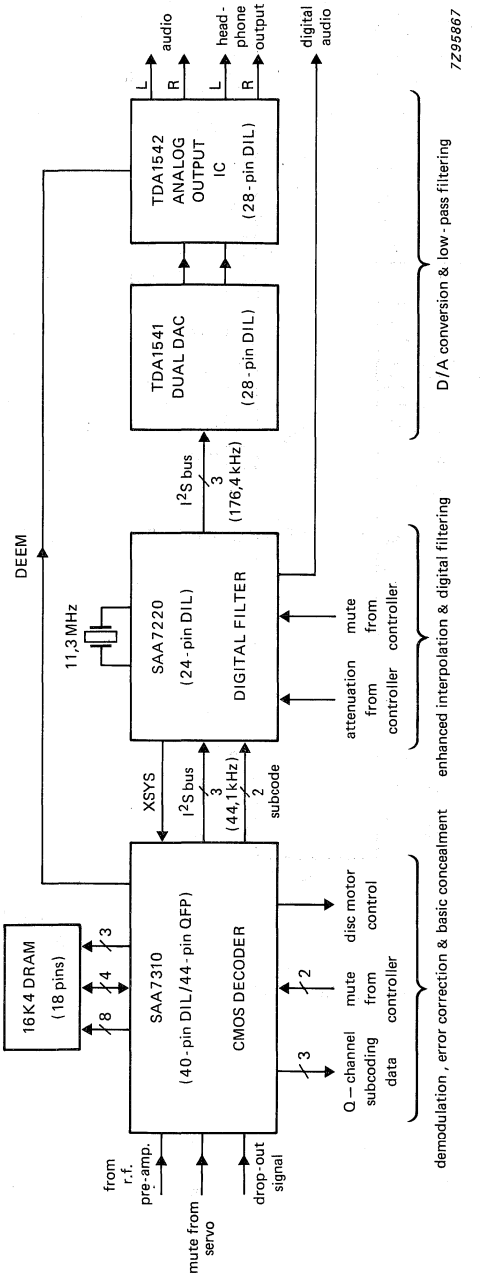


Fig. 2 (b) Block diagram of SAA7310 as used with SAA7220.

PINNING

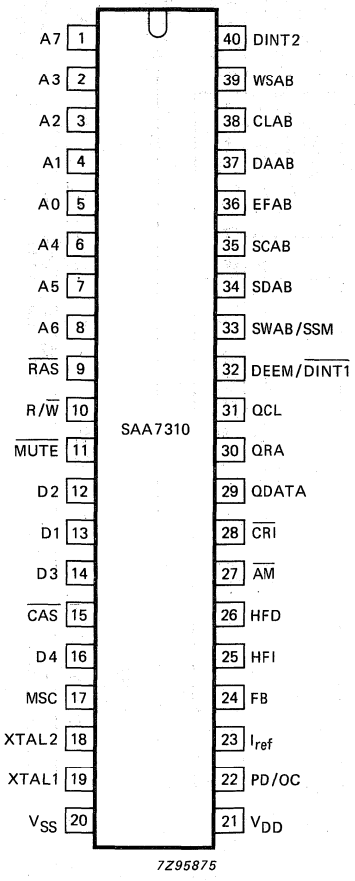


Fig. 3 Pinning diagram; for 40-lead DIL package.

PINNING (continued)

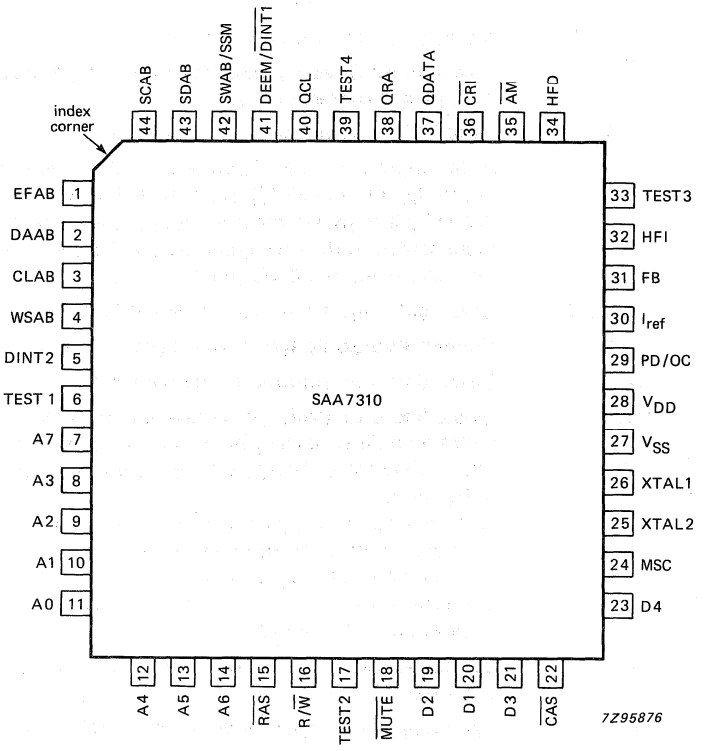


Fig. 4 Pinning diagram; for 44-lead QFP package.

Pin functions

pin no. DIL	pin no. QFP	mneumonic	description
1 - 8	7 - 14	A0 - A7	**Address:** address outputs to external RAM.
9	15	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	16	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	18	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB, pin 37 (2), is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first 'good' value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12 - 14	19 - 21	D1 - D3	**Data:** data inputs/outputs to external RAM.
15	22	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	23	D4	**Data:** data input/output to external RAM.
17	24	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (42) (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continuous 50% duty factor.
18	25	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	26	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	27	V_{SS}	**Ground:** circuit earth potential.
21	28	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).
22	29	PD/OC	**Phase Detector output/ Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	30	I_{ref}	**Current reference:** external reference input to the phase detector and data slicer. This input is required to minimize the spread in the charge pump output of the phase detector and data slicer.
24	31	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input HFI at pin 25 (32) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD at pin 26 (34) is LOW, this output goes to a high impedance state.

Pin functions (continued)

pin no. DIL	pin no. QFP	mneumonic	description
25	32	HFI	**High-Frequency Input:** level detector input to the data slicer. A differential signal of between 0,5 and 2,5 V (peak-to-peak value) is required to drive the data slicer correctly. When a T_{max} violation is detected or when HFD is LOW, this input is biassed directly to its threshold voltage
26	34	HFD	**High-Frequency Detector:** when HIGH this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer. An internal voltage clamp of 3 V (typ.) requires the HFD input to be fed via a high impedance. This input has an internal pull-up of 50 kΩ (typ.).
27	35	$\overline{AM}$	**Additional Mute:** This pin is normally held HIGH. Should track loss occur the pin should be taken LOW and then the data is forced LOW at the pre-FIFO stage. The muted data will then be corrected after de-interleaving. **Note** With DINT2, DEEM/$\overline{DINT1}$, FB set to logic 0 and SDAB, SCAB set to logic 1, this pin becomes the demodulator clock output (CEFM) of the SAA7210 (CD2A).
28	36	$\overline{CRI}$	**Counter Reset Inhibit:** when LOW this input signal allows the divide-by-588 master counter in the DEMOD timing to run-free. This input has an internal pull-up of 50 kΩ (typ.).
29	37	QDATA	**Q-channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol).
30	38	QRA	**Q-channel Request input/Acknowledge output:** the output has an internal pull-up of nominally 10 kΩ. (see subcoding microprocessor handshaking protocol).
31	40	QCL	**Q-channel Clock:** clock input generated by the microprocessor when it detects a QRA LOW signal.
32	41	DEEM/$\overline{DINT1}$	**De-emphasis output and data interpolated input:** signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit in DEEM mode. When using the CD3A in a non-digital audio application this pin should be set HIGH (with DINT2 set LOW) to prevent data being interpolated. **Note** This pin should **only** be used in its input mode when DINT2 is LOW.
33	42	SWAB/SSM	**Subcoding Word clock output and Start/Stop Motor input:** open drain output which is sensed during each HIGH period and if externally forced LOW a motor-stop condition will be decoded and fed to the motor control logic circuit. When allowed to return HIGH, the motor will start. This open-drain output has an internal pull-up of 10 kΩ (typ.).

Pin functions

pin no. DIL	pin no. QFP	mneumonic	description
34	43	SDAB	**Subcoding Data:** a 10-bit burst of data, including flags and sync bits, is output serially once per frame clocked by burst clock output SCAB (see Fig. 6).
35	44	SCAB	**Subcoding Clock:** a 10-bit burst clock 2,8224 MHz (typ.) output which is used to synchronize the subcoding data.
36	1	EFAB	**Error Flag:** output from interpolation and mute circuit indicating unreliable data.
37	2	DAAB	**Data:** this output together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Fig. 7).
38	3	CLAB	**Clock:** I^2S output.
39	4	WSAB	**Word Select:** I^2S output.
40	5	DINT2	**Data interpolated input:** this pin should normally be set HIGH. When using the CD3A in a non-digital audio application this pin should be set LOW (with DEEM/$\overline{\text{DINT1}}$ set HIGH) to prevent data being interpolated.

The following pins apply to the 44-pin QFP package only:

–	6	TEST1	**Test output 1**
–	17	TEST2	**Test output 2**
–	33	TEST3	**Test output 3**
–	39	TEST4	**Test output 4**

Note to the pin functions

The pin sequence of the address outputs (A0 - A7) and the data outputs (D1 - D4) has been selected to be compatible with various dynamic 16 K x 4-bit RAMs including the 4416.

FUNCTIONAL DESCRIPTION

All references to pin numbers show the 40-lead DIL pin first followed by the 40-lead QFP pin in parenthesis.

Demodulation

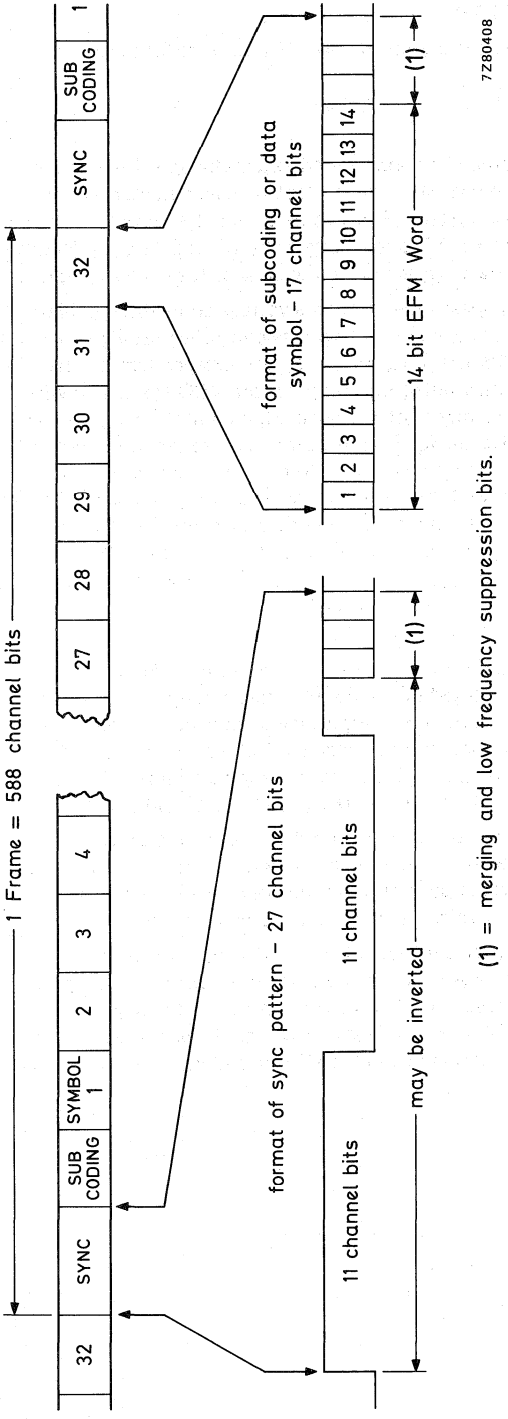
Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at the input data rate (typically at 4,3218 MHz), its frequency being dependent on the voltage at pin 22 (29) (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output provides the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (29), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source I_{ref} connected to pin 23 (30).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input at pin 28 (36) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.



(1) = merging and low frequency suppression bits.

Fig. 5 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output pin 32 (41) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34 (43). The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally in the rising edge of SWAB at pin 33 (42); see Fig. 6.

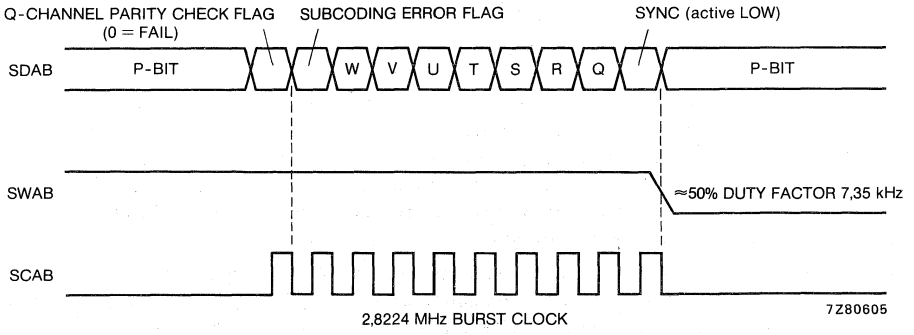


Fig. 6 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4-symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency.

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 8) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address $\overline{\text{RAS}}$ pin 9 (15) is set up first and then three 4-bit nibbles are accessed using sequential column addresses $\overline{\text{CAS}}$ pin 15 (22). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good' data (flags = 00) and three levels of error can be indicated.
The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

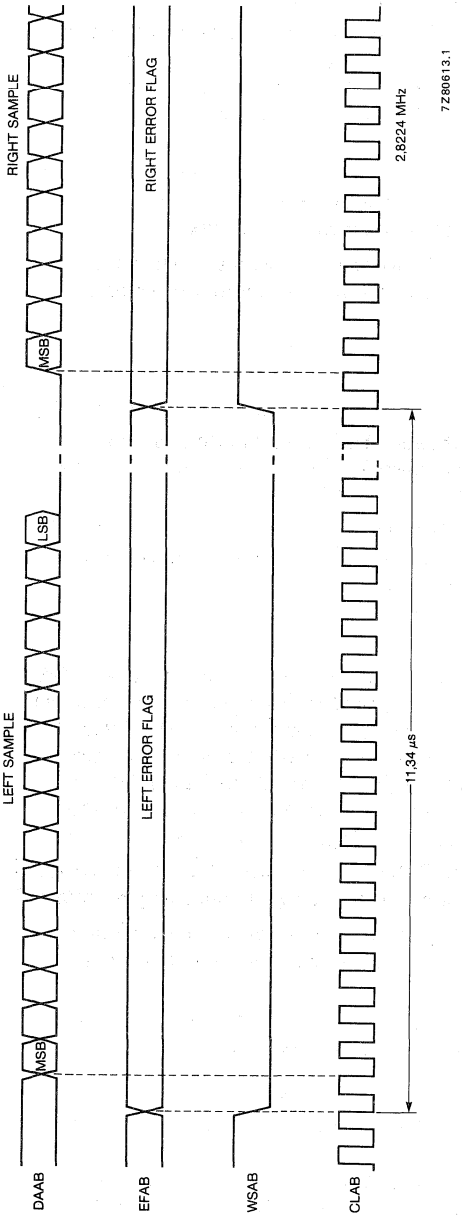


Fig. 7 Typical I²S waveform outputs to SAA7220 or SAA7320.

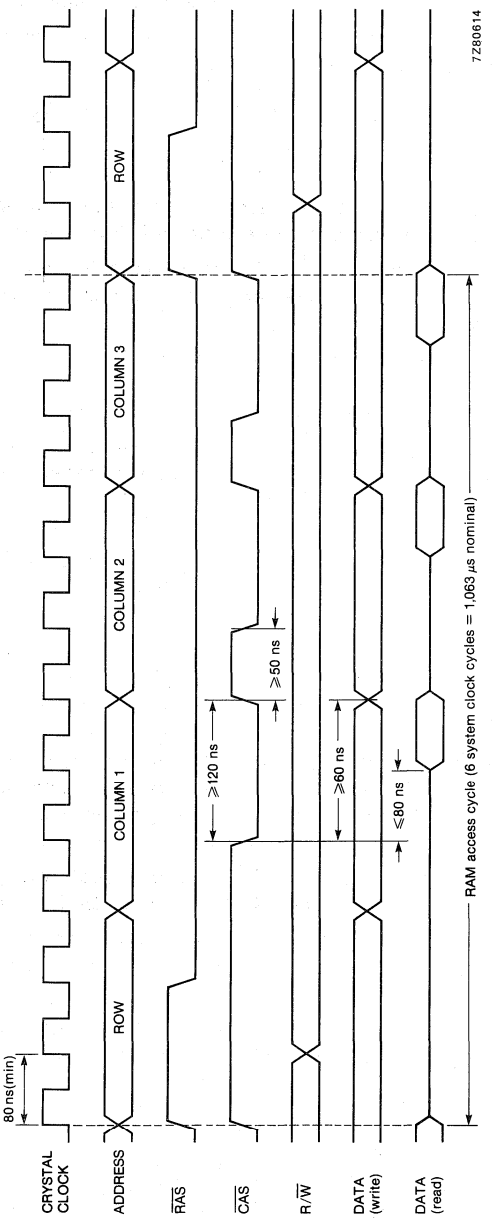


Fig. 8 RAM timing waveforms: timings based on RAM TMS4416; $\overline{G}$ input to RAM held LOW.

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

When using the CD3A in a non-digital audio application, pins DINT2 and DEEM/$\overline{\text{DINT1}}$ should be set to logic 0 and logic 1 respectively. The URD flag will then be disabled to prevent data being interpolated.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the SAA7220 where it receives additional and more efficient concealment (see Fig. 9).

FUNCTIONAL DESCRIPTION (continued)

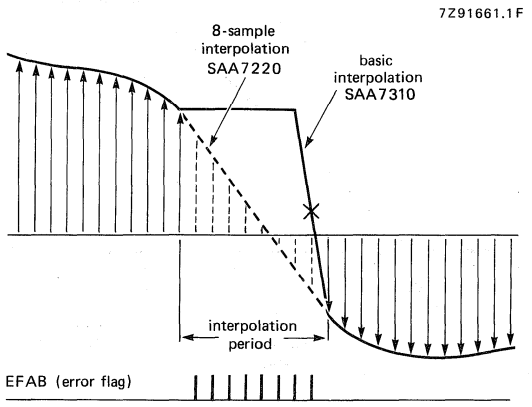


Fig. 9 The SAA7220 can make an 8-sample linear interpolation, the SAA7310 a hold and single-sample interpolation. When interpolating more than 8 samples, a hold function operates in the SAA7220 before the interpolation.

Non-digital audio applications

The CD3A contains a special mode for non-digital applications such as CD-ROM and CD-I. In this mode the concealment section is not allowed to operate. The flagged output words of the error correction circuit are passed to the output DAAB without being affected by the interpolation circuit. The EFAB output signal indicates unreliable output words on a sample basis when one or both bytes in a sample are unreliable. This is necessary as the CD-ROM/CD-I player performs its own error correction strategy on the data. The level of data integrity has to be much higher to ensure no errors occur in text or numerical information.

Specifications of CD-ROM and CD-I modes are available on request.

Motor speed control (see Fig. 10)

The motor speed control (MSC) output from pin 17 (24) is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

Track loss correction

The CD3A also incorporates a function to provide extra correction during track loss. Should track loss occur, the additional mute pin ($\overline{AM}$) should be taken LOW, which forces the data LOW at the pre-FIFO stage. This muted data is then corrected after de-interleaving. This function is particularly useful for applications where mechanical shock is likely to occur.

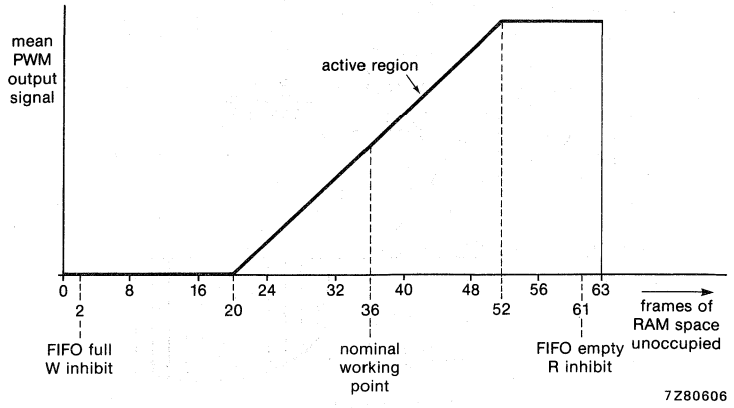


Fig. 10 Motor speed control.

CD2A replacement

The CD3A can become a direct replacement for the CD2A by externally connecting pin 21 to V_{DD} and modifying the PLL peripheral components (see Fig. 12).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage, pin 21 (28)	V_{DD}	−0,5	+ 6,5	V
Maximum input voltage	V_I	−0,5	V_{DD} + 0,5	V
Input current, pin 23 (30)	I_I	−	5	mA
Maximum output voltage MSC, QRA, SWAB/SSM	V_O	−0,5	+ 6,5	V
Output current (each output)	I_O	−	± 10	mA
DC V_{SS} or V_{DD} current	I_{DD} or I_{SS}	−	± 100	mA
DC input diode current	I_{IK}	−	± 20	mA
DC output diode current	I_{OK}	−	± 20	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*	V_{es}	−1000	+ 1000	V

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

Detailed information on the I²S bus specification is available on request.

Supply of this Compact Disc IC does not convey an implied licence under any patent right to use this IC in any Compact Disc application.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage, pin 21 (28)		V_{DD}	4,5	5,0	5,5	V
Supply current, pin 21 (28)		I_{DD}	–	35	50	mA
Inputs						
D1 – D4, QCL, $\overline{AM}$, DEEM/$\overline{DINT1}$, DINT2						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
$\overline{MUTE}$, $\overline{CRI}$						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	18	50	110	kΩ
Input capacitance		C_I	–	–	10	pF
QRA, SWAB/SSM						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance		C_I	–	–	10	pF
Internal pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	3,9	10	18	kΩ
HFD						
Input voltage LOW		V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH		V_{IH}	2,0	–	clamped	V
Input clamping voltage	I_I = 100 μA	V_{CL}	2,0	3,0	4,5	V
Input source current		I_S	−100	–	100	μA
Input capacitance		C_I	–	–	10	pF
Internall pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	18	50	110	kΩ

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs						
A0–A7, R/$\overline{W}$, D1–D4, $\overline{CAS}$, $\overline{RAS}$, QDATA, DEEM/$\overline{DINT1}$, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB, TEST1, TEST2, TEST3, TEST4						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD}	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
MSC (open drain)						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	0	–	0,35	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
SWAB/SSM, QRA (open drain)						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance		C_L	–	–	50	pF
Internal load resistance		R_L	3,9	10	18	kΩ
ANALOGUE CIRCUITS						
Data slicer (see Fig. 11)						
Input HFI						
AC input voltage range (peak-to-peak value)		$V_{I(p-p)}$	0,5	–	2,5	V
Input impedance						
normal (HFD HIGH)		$\|Z_I\|$	500	–	–	kΩ
disabled (HFD LOW)		$\|Z_I\|$	50	100	200	kΩ
Input capacitance		C_I	–	–	10	pF
Output FB						
Output current	V_{FB} = 2 V	I_O	$I_{ref}/5$ −20%	$I_{ref}/5$	$I_{ref}/5$ +20%	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase detector						
Output PD/OC	see Fig. 12					
Output current	PD/OC = 1 to 3 V	I_O	$\pm I_{ref}-20\%$	$\pm I_{ref}$	$\pm I_{ref}+20\%$	μA
Control range	note 3	α	±2,1	–	–	rad
Input I_{ref}	see Fig. 13					
Input reference current		I_{ref}	–	500	*	μA
Fine frequency detector						
Output PD/OC						
Output impedance		$\|Z_O\|$	2	4,1	5,6	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Coarse frequency detector						
Output PD/OC	note 4					
Output impedance		$\|Z_O\|$	1	2,3	3,2	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Voltage controlled oscillator						
Input PD/OC						
Oscillator constant		K_{osc}	–	3,5	–	MHz/V
Crystal oscillator	see Fig. 14					
Input XTAL1						
Output XTAL2						
Mutual conductance	100 kHz	G_m	1,5	–	–	ms
Small signal voltage gain	$G_v = G_m \times R_o$	G_v	3,5	–	–	V/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
Output capacitance		C_O	–	–	10	pF
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Slave clock mode	see Fig. 15					
Input voltage (peak-to-peak value)		$V_{I(p-p)}$	3,0	–	$V_{DD}+0,5$	V
Input voltage LOW	note 1	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	note 1	V_{IH}	2,4	–	$V_{DD}+0,5$	V
Input rise time	note 5	t_r	–	–	20	ns
Input fall time	note 5	t_f	–	–	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	–	55	%
TIMING						
Operating frequency (XTAL)		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)	PLL locked on to data	f_{VCO1}	2,54	4,3218	6,21	MHz
Operating frequency (VCO)	VCO absolute limits; PLL not locked on to data	f_{VCO2}	2	–	7,5	MHz
Outputs	Figs. 16 and 17					
CEFM	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
Output HIGH time		t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (I^2S format)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB						
Data set-up time		$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB						
Data hold time		$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (subcoding outputs)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
SDAB to SCAB						
Subcoding data set-up time		$t_{SU;SDAT}$	100	–	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
SCAB to SDAB						
Subcoding data hold time		$t_{HD;SDAT}$	100	–	–	ns
SWAB/SSM	note 6					
Output rise time		t_r	–	–	1	ns
Output fall time		t_f	–	–	100	ns
Output duty factor			–	50	–	%
Q-channel I/O	Figs 18 and 19					
QRA, QCL, QDATA						
Access time	note 7					
normal mode		$t_{ACC;N}$	0	–	13,3 + n x 13,3	ms
refresh mode		$t_{ACC;F}$	13,3	–	n x 13,3	ms
QCL to QRA						
acknowledge delay		t_{DACK}	–	–	500	ns
request hold time		$t_{HD;R}$	750	–	–	ns
QCL clock input LOW time		$t_{CK;LOW}$	750	–	–	ns
QCL clock input HIGH time		$t_{CK;HIGH}$	750	–	–	ns
QCL to QDATA delay time		t_{DD}	–	–	750	ns
Data hold time before						
new frame is accessed		$t_{HD;ACC}$	2,3	–	–	ms
Acknowledge time		t_{ACK}	–	–	10,8	ms

Notes to the characteristics

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{LI(min)}$ and $I_{LO(min)}$ measured at $V_I = 0$ V; $I_{LI(max)}$ and $I_{LO(max)}$ measured at $V_I = V_{DD}$.
3. 1 rad = $\frac{180^o}{(3,14)}$.
4. Coarse frequency detector output PD/OC active for VCO frequencies

   $> \frac{f_{XTAL}}{2}$ and $< \frac{f_{XTAL}}{4}$.
5. Reference levels = 0,5 V and 2,5 V.
6. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
7. Q-channel access times dependent on cyclic redundancy check (CRC);
   n = number of cycles until CRC is 'good'.

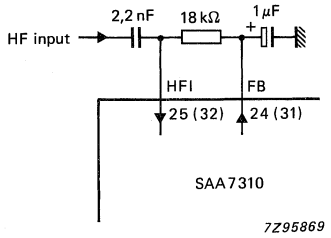


Fig. 11 Data slicer HFI input.

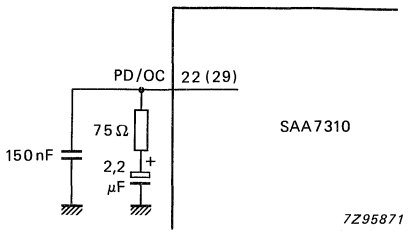


Fig. 12 PLL circuit.

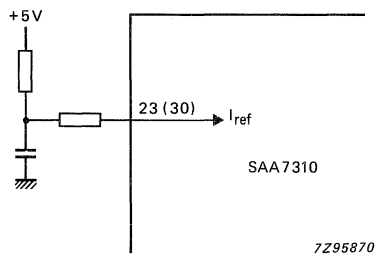


Fig. 13 I_{ref} circuit.

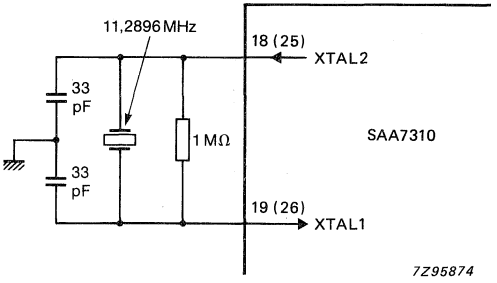


Fig. 14 Crystal oscillator circuit; using crystal type: 4322 143 05031.

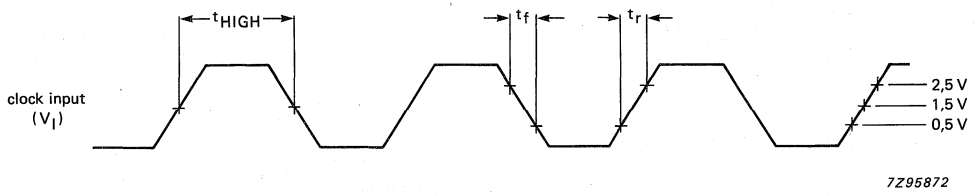


Fig. 15 Input clock timing diagram; reference levels 0,5 V, 1,5 V and 2,5 V.

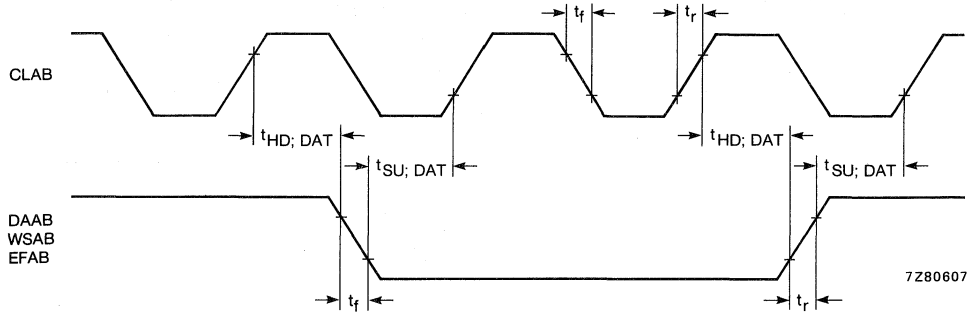


Fig. 16 Typical I²S data output waveforms; reference levels = 0,8 V and 2,0 V.

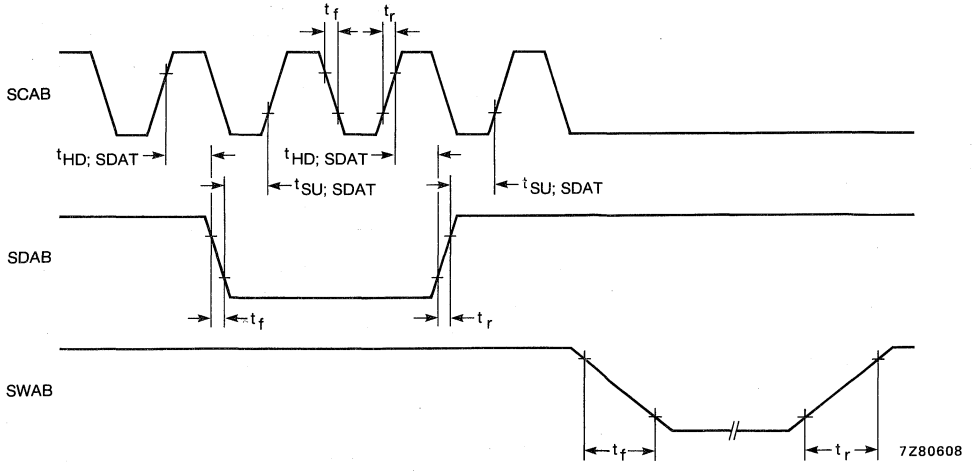


Fig. 17 Typical subcoding data output waveforms; reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

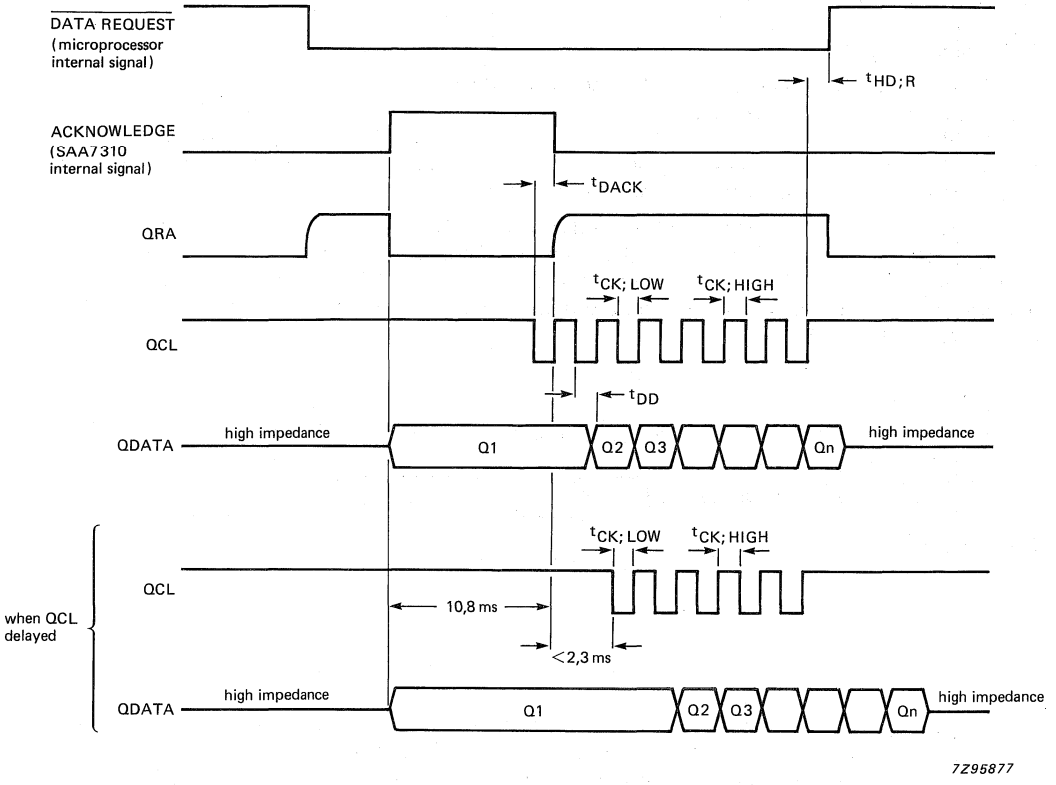


Fig. 18 Q-channel timing waveforms (normal mode).

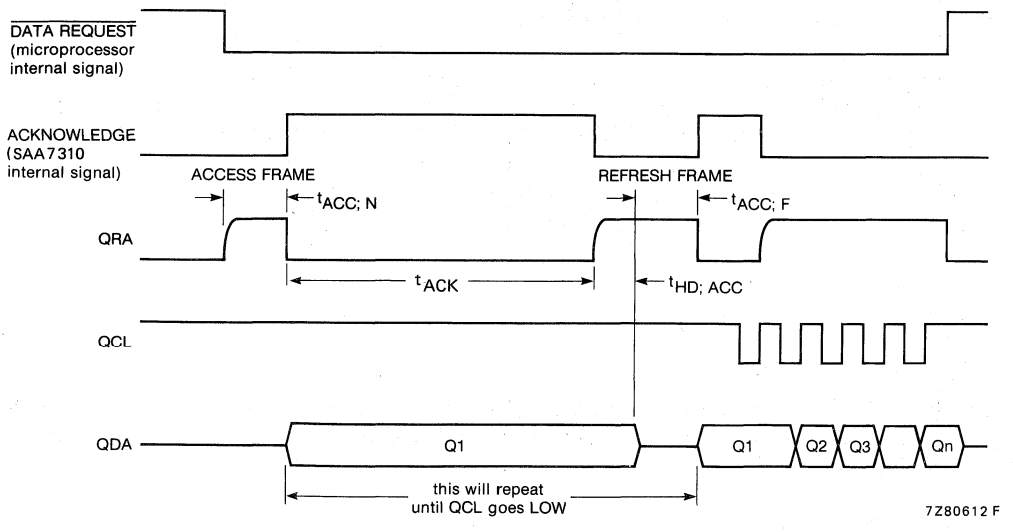


Fig. 19 Q-channel timing waveforms (refresh mode).

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a DC free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the DC content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 20).

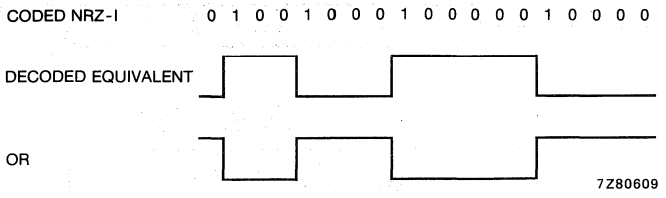


Fig. 20 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

APPLICATION INFORMATION (continued)

Table 2 EFM code conversion

No.	DNZ data symbol D1 D8	equivalent code word C1 C14	No.	DNZ data symbol D1 D8	equivalent code word C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 0 1 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 0 1 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11 to 119			139 to 247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

Subcoding microprocessor handshaking protocol (see Figs. 18, 19 and 21)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7310.

The SAA7310 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7310 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7310 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowlegde signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7310 now disabled the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7310 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7310 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

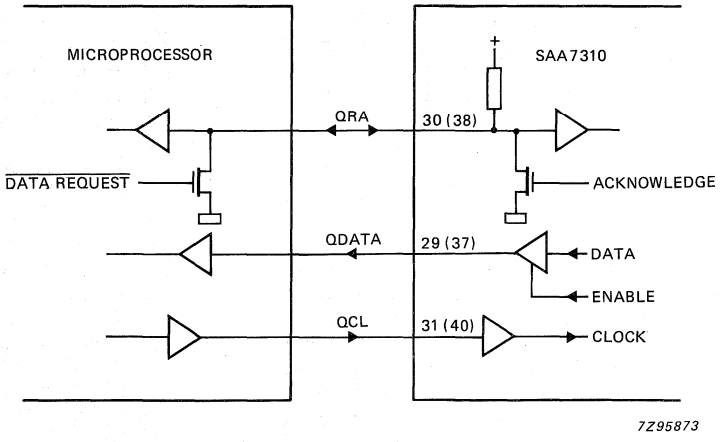


Fig. 21 Microprocessor handshaking protocol.

Stereo CMOS bitstream DAC for digital audio systems

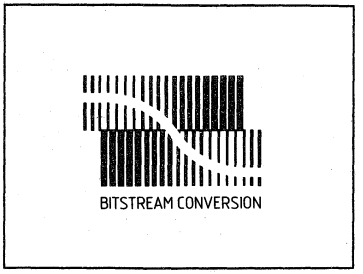
SAA7322/SAA7323

FEATURES

- I²S data input
- 3-stage digital filter incorporating F.I.R. filter, linear interpolator and sample-and-hold
- 2nd order noise shaper to improve analog performance
- 16-bit resolution from a bitstream conversion DAC, using switched capacitor integrator
- 3rd order low-pass filter to reduce out-of-band noise
- −12 dB attenuation, de-emphasis and mute control
- TTL compatible input/outputs

GENERAL DESCRIPTION

The SAA7322/7323 (DAC3) is a complete monolithic stereo CMOS 16-bit input bitstream conversion digital-to-analog converter designed for use in digital audio systems. The device is a replacement for the SAA7320, offering improved "idle pattern" performance at low-levels. The SAA7322 is a lower performance version of the SAA7323.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
DR	dynamic range	note 1				
	SAA7322		–	93	–	dB
	SAA7323		93	–	–	dB
THD+N	total harmonic distortion plus noise	note 1				
	SAA7322		–	−88	–	dB
	SAA7323		–	–	−90	dB
f_{XTAL}	operating crystal frequency		8	11.2896	12.3	MHz
T_{amb}	operating ambient temperature range					
	SAA7322		−10	–	+70	°C
	SAA7323		−40	–	+85	°C

Note to the quick reference data

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7322GP	44	QFP	plastic	SOT205AG
SAA7323GP	44	QFP	plastic	SOT205AG

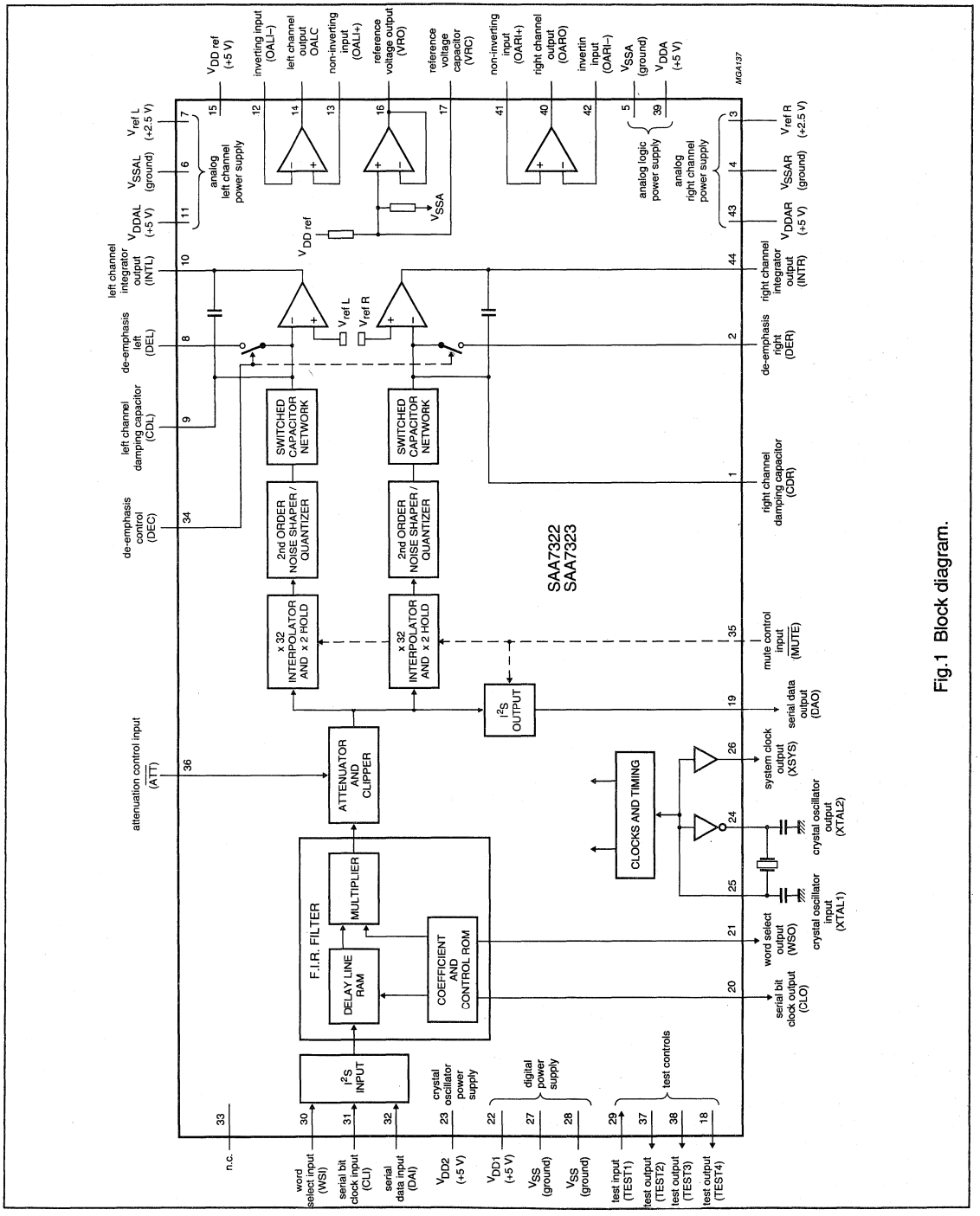


Fig.1 Block diagram.

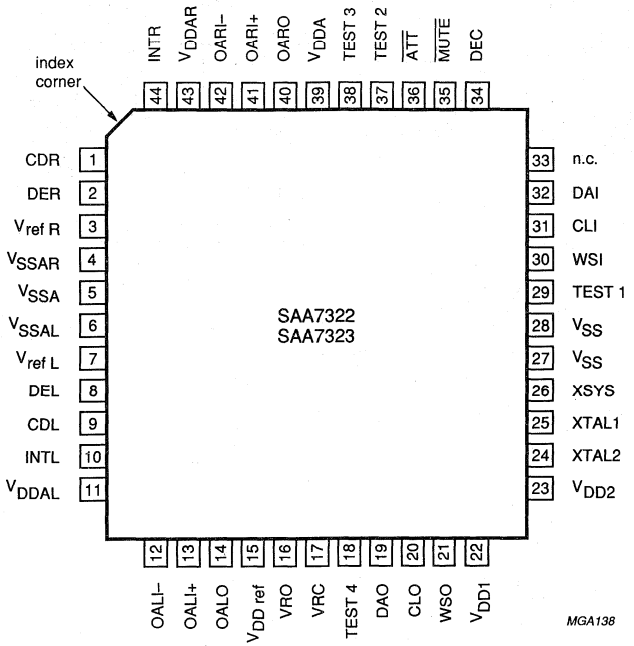


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
CDR	1	damping capacitor for the right channel switched-capacitor integrator
DER	2	connection to the de-emphasis switch in the right channel integrator
V_{refR}	3	reference voltage input for the analog channel ground (normally connected to VRO)
V_{SSAR}	4	ground connection for the analog right channel
V_{SSA}	5	ground connection for logic in the analog section
V_{SSAL}	6	ground connection for the analog left channel
V_{refL}	7	reference voltage input for the analog left channel ground (normally connected to VRO)
DEL	8	connection to the de-emphasis switch in the feedback of the left channel integrator
CDL	9	damping capacitor for the left channel switched-capacitor integrator
INTL	10	output from the left channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDL
V_{DDL}	11	+5 V supply voltage for the analog left channel
OALI−	12	inverting input to the left channel low-pass filter operational amplifier
OALI+	13	non-inverting input to the left channel low-pass filter operational amplifier

SYMBOL	PIN	DESCRIPTION
OALO	14	output from the left channel operational amplifier
V_{DDref}	15	+5 V supply voltage for the reference voltage generator
VRO	16	internal reference voltage output (+2.5 V typ.)
VRC	17	internal reference voltage high impedance node requiring an external smoothing capacitor
TEST4	18	test output 4: pin should be left open-circuit
DAO	19	I²S serial data output is a 16-bit linear two's-complement PCM signal at a data rate of 176.4 kHz (typ.) formatted in accordance with I²S . After 4 x upsampling by the digital filter this signal is output so that an external DAC could be used; combined with CLO and WSO it can be considered as a master transmitter
CLO	20	I²S serial bit clock output, f_{CLKO} = 5.6448 MHz (typ).
WSO	21	I²S word select output 176.4 kHz (typ).
V_{DD1}	22	+5 V supply voltage for the digital section
V_{DD2}	23	+5 V supply voltage for the crystal oscillator
XTAL2	24	drive output to clock crystal
XTAL1	25	input from crystal oscillator or external clock input 11.2896 MHz (typ.)
XSYS	26	buffered output from crystal oscillator
V_{SS}	27, 28	ground connection for the digital section
TEST1	29	test input 1, pin should be connected to ground
WSI	30	I²S word select input, 44.1 kHz (typ) WSI together with CLI, is used to clock the I²S serial data input (DAI) and synchronize the main timing chain
CLI	31	I²S serial bit clock input, f_{CLKI} = 2.8224 MHz (typ).
DAI	32	I²S serial data input is a 16-bit linear two's-complement PCM signal formatted in accordance with I²S. If more than 16 bits are supplied then the least significant bits (LSBs) will be truncated
n.c.	33	not connected
DEC	34	de-emphasis control input switches an extra external capacitor network into both the analog left and right channel integrator feedback
MUTE	35	when active LOW this Schmitt trigger control input will force the interpolator data input to zero. It will also force the I²S data output (DAO) to zero
ATT	36	when active LOW this control input provides –12 dB attenuation to the analog output amplitude
TEST2	37	test output 2, pin should be left open-circuit
TEST3	38	test output 3, pin should be left open-circuit
V_{DDA}	39	+5 V supply voltage for logic in the analog section
OARO	40	output from the right channel operational amplifier
OARI+	41	non-inverting input to the right channel low-pass filter operational amplifier
OARI–	42	inverting input to the right channel low-pass filter operational amplifier
V_{DDAR}	43	+5 V supply voltage for the analog right channel
INTR	44	output from the right channel switched-capacitor integrator. Internal capacitor (85 pF typ.) connected to CDR

FUNCTIONAL DESCRIPTION

General

The SAA7322/7323 CMOS DAC heavily oversamples to several MHz (256 x the sampling frequency f_s), so that the band-limiting filters required for waveform smoothing and out-of-band noise reduction are mainly digital. In addition to the digital filters, the circuit contains active components for analog post filtering. In most applications very few external components are required. An output after the 4 x upsampling filter allows the circuit to be used as an interface between the decoder and external DAC in high-performance compact disc systems. The device requires only one +5 V supply; the required reference voltage is generated internally.

Separate supply pins for each of the bitstream conversion DACs achieves high performance signal-to-noise ratio and channel separation.

There is no phase delay between the two analog outputs despite the fact that the upsampling filter structure is multiplexed between the two data channels.

Oversampling digital filter

This is a 3-stage digital filter

- The first stage provides 4 x oversampling to 176.4 kHz using a 128-tap F.I.R. low-pass filter. Data is stored in a cyclic RAM, the filter coefficients in a ROM and the convolutions are performed using an array multiplier.
- The second stage is a 32 x oversampling linear interpolator.
- The third stage provides 2 x upsampling using a sample-and-hold, giving a total of 256 x upsampling (11.2896 MHz).

The first stage oversamples to 176.4 kHz with a band-pass ripple of ±0.035 dB and a stop-band attenuation of −60 dB above 24.2 kHz. It also contains frequency response compensation for the interpolator/analog post-filtering roll-off and coefficient scaling to prevent overflow in the noise shaper.

The characteristics of the F.I.R. filter are shown in Fig.9.

Switched-capacitor DAC

The digital-to-analog conversion is achieved with a bitstream conversion DAC oversampled to 256 f_s with second-order noise shaping performed digitally to give a 1-bit Pulse Density Modulated (PDM) code. Integral with the actual bitstream conversion converter is a first-order low-pass filtering action which reduces the total HF noise power.

A switched capacitor technique is used for the bitstream conversion DAC which converts the PDM stream to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of a first-order filter. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure. The output slew rate of this filter is chosen so that the operational amplifiers always remains within its high gain linear region.

An internally generated out-of-band dither signal is used to suppress audible idling patterns in the noise shaper at low signal levels. This signal is injected digitally into the x 32 upsampling interpolator at a frequency of 352.8 kHz and a level of −20 dB.

Attenuation

Attenuation is controlled by the ATT input at pin 36. This input will allow an attenuation of the analog output amplitude by 12 dB during track search.

De-emphasis and low-pass filter

Extra on-chip analog circuitry provides post filtering:

- Input DEC (pin 34) switches an extra external capacitor network into both the left and right channel analog integrator feedback to control roll-off. Output from the right channel switched-capacitor integrator (INTR) is available at pin 44. Output from the left channel switched-capacitor integrator (INTL) is available at pin 10.
- A low-pass filter, for further attenuation of out-of-band noise, can be constructed using the internal CMOS operational amplifiers. The digital filter contains compensation for a third-order Butterworth filter with a −3 dB cut-off at 60 kHz.

I²S serial interface

The SAA7322/7323 has two I²S ports incorporated; DAI (pin 32) and DAO (pin 19).

- DAI receives data from the compact disc decoder IC (or any 16-bit 44.1 kHz I²S source).
- DAO transmits the 4 x oversampled data to an external DAC.

The 'slave' receiver requires a serial bit clock input (CLI; pin 31) and a word select input (WSI; pin 30). To ensure that the filter is 'in-phase' with the input, the main timing chain

is automatically synchronized to the incoming word select signal. The frequency of the data must also be synchronized to the filter by:

- the source supplying the 11.2896 MHz system clock via crystal oscillator input (XTAL1; pin 25).

or

- SAA7322/7323 supplying the system clock to the source via XSYS (pin 26).

The SAA7322/7323 will use only the 16 most significant bits of input data even though the I²S format allows a variable word length (see Fig.4).

The 'master' transmitter supplies bit clock, word select and data signals for the 4 x upsampled output (see Fig.5).

Conversion path

The data conversion path is shown in Fig.3. As both paths are identical only one path is shown. The data flow is in a serial format up to the linear interpolator stage and then separated into two channels.

A recommended system application diagram of the SAA7322/7323 is shown in Fig.10.

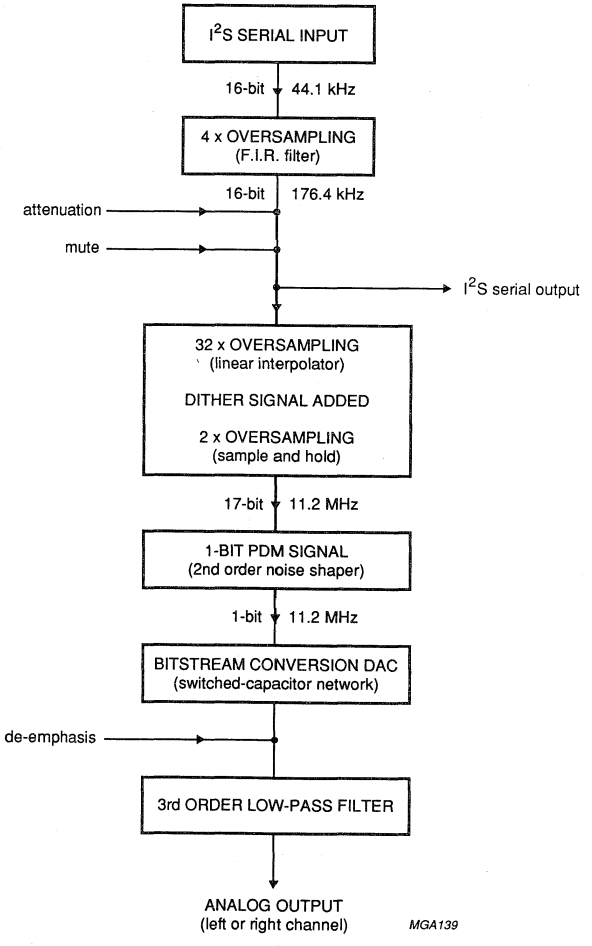


Fig.3 Flow diagram of SAA7322/7323 data conversion path (one channel).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	V_{DD}+0.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD}+0.5	V
I_O	DC output sink/source current		–	±25	mA
$I_{DD, SS}$	total DC current V_{DD} or V_{SS}		–	±0.5	A
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range				
	SAA7322		−10	+70	°C
	SAA7323		−40	+85	°C
V_{es}	electrostatic handling	note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Suppy						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	20	35	mA
I_{DDD}	digital supply current		–	40	85	mA
Analog part						
REFERENCE VOLTAGE SOURCE VRC						
V_{refC}	high impedance reference voltage level		–	2.5	–	V
Z_{refO}	reference voltage output impedance		–	2	–	Ω
OUTPUTS OALO AND OARO (NOTES 1 AND 2)						
$V_{O\ RMS}$	output level (RMS value)	note 3; 0 dB	0.8	0.9	1.0	V
CHM	channel matching	note 4	–	–	±0.25	dB
OUTPUT PERFORMANCE (NOTE 1)						
DR	dynamic range					
	SAA7322		–	93	–	dB
	SAA7323		93	–	–	dB
THD+N	total harmonic distortion plus noise	at 0 dB/1 kHz				
	SAA7322		–	–88	–	dB
	SAA7323		–	–	–90	dB
	digital silence		–	–96	–	dB
α	channel separation	at 1 kHz	–	90	–	dB
SVRR	supply voltage rejection ratio to V_{DD}		–	60	–	dB
L	linearity	–60 to –100 dB	–	±2	–	dB
Digital part						
INPUTS WSI, CLI, DAI, DEC AND ATT						
V_{IL}	LOW level input voltage	note 5	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 5	2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA
C_I	input capacitance		–	–	10	pF
MUTE (Schmitt trigger)						
V_{IL}	LOW level input voltage	note 5	–0.5	–	1.8	V
V_{IH}	HIGH level input voltage	note 5	3.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	note 6	–10	0	+10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance		–	–	10	pF
XTAL1 (external clock only)						
V_{IL}	LOW level input voltage	note 5	−0.5	–	1.5	V
V_{IH}	HIGH level input voltage	note 5	3.5	–	V_{DD} to 5 V	V
I_{LI}	input leakage current	note 6	−10	0	+10	μA
C_I	input capacitance		–	–	10	pF
OUTPUTS DAO, CLO, WSO AND XSYS						
V_{OL}	LOW level output voltage	note 5; I_{OL} = 400 μA	−0.5	–	+0.4	V
V_{OH}	HIGH level output voltage	note 5; I_{OH} = 20 μA	2.4	–	V_{DD}+0.5	V
C_L	load capacitance		–	–	35	pF
Crystal oscillator (input XTAL1, output XTAL2) (see Fig.8)						
f_{XTAL}	crystal operating frequency		8	11.2896	12.3	MHz
gm	mutual conductance	at 100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	G_v = gm x R_O	3.5	–	–	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 6	−10	–	+10	μA
Timing						
EXTERNAL CLOCK INPUT						
XTAL1						
f_{CLK}	input frequency	f_s x 256	8	11.2896	12.3	MHz
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	relative at 1.5 V to clock period	45	–	55	%
SYSTEM CLOCK OUTPUT XSYS (NOTE 8)						
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
t_{HIGH}	input HIGH time	note 9; relative at 1.5 V to clock period	45	–	55	%
I^2S TIMING; RECEIVER CLOCK INPUT CLK_I (SEE FIG.6)						
t_{CLK}	input clock period		320	354	1000	ns
t_{CLKH}	input clock time HIGH		112	–	–	ns
t_{CLKL}	input clock time LOW		112	–	–	ns
Data input WSI and DAI						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMITTER (SEE FIG.7)						
clock output CLO						
t_{CLK}	output clock period		–	$2/f_{CLK}$	–	ns
t_{CLKH}	output clock time HIGH		60	–	–	ns
t_{CLKL}	output clock time LOW		60	–	–	ns
Word select WSO						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns
Data output DAO						
$t_{SU;DAT}$	data set-up time		40	–	–	ns
$t_{HD;DAT}$	data hold time		40	–	–	ns
t_r, t_f	input rise and fall time	note 7	–	–	20	ns

Notes to the characteristics

1. Output characteristics measured with external components shown in Fig.10. Sample rate = 44.1 kHz.
2. Maximum load on INTL, INTR (excluding feedback) is 10 kΩ, 20 pF to V_{ref}. Dynamic output impedance is typ. 150 Ω (open loop).

   Maximum load on OALO, OARO (excluding feedback) is 3 kΩ, 200 pF. Dynamic output impedance is typ. 100 Ω (open loop).
3. Output level changes linearly with clock frequency.
4. With matched external components.
5. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
6. $I_{LI\ min}$ and $I_{LO\ min}$ measured at $V_I = 0$ V; $I_{LI\ max}$ and $I_{LO\ max}$ measured at $V_I = V_{DD}$.
7. Reference levels = 0.8 V and 2 V.
8. Output times are measured with a capacitive load of 35 pF.
9. t_{HIGH} valid only when used with XTAL.

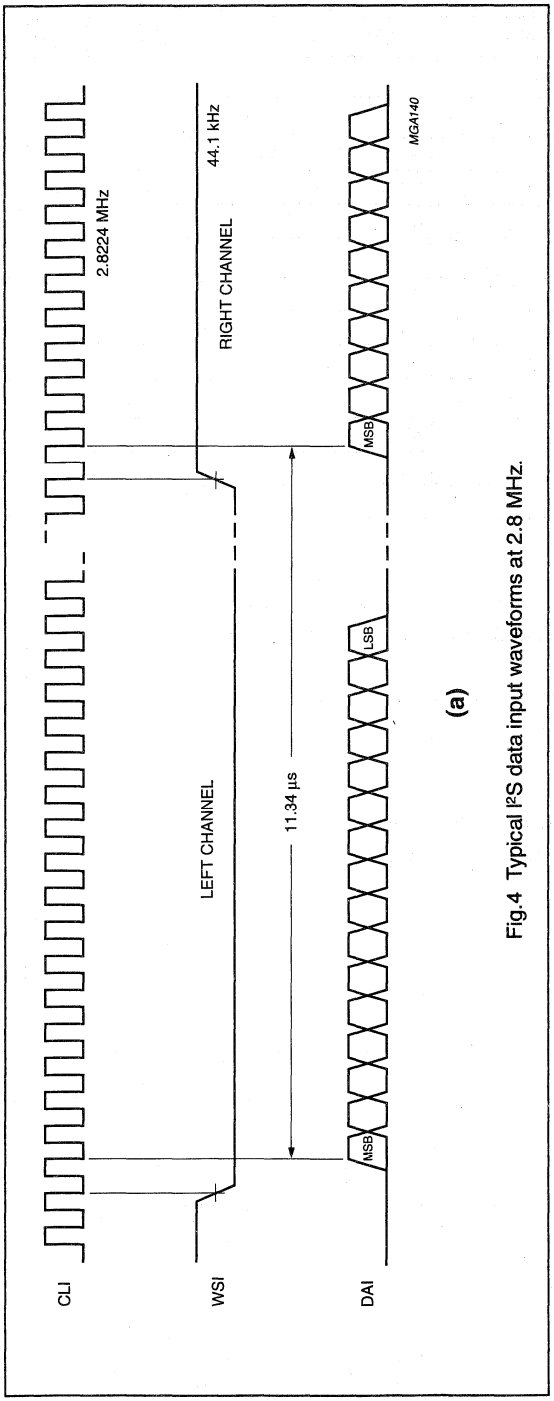


Fig.4 Typical I²S data input waveforms at 2.8 MHz.

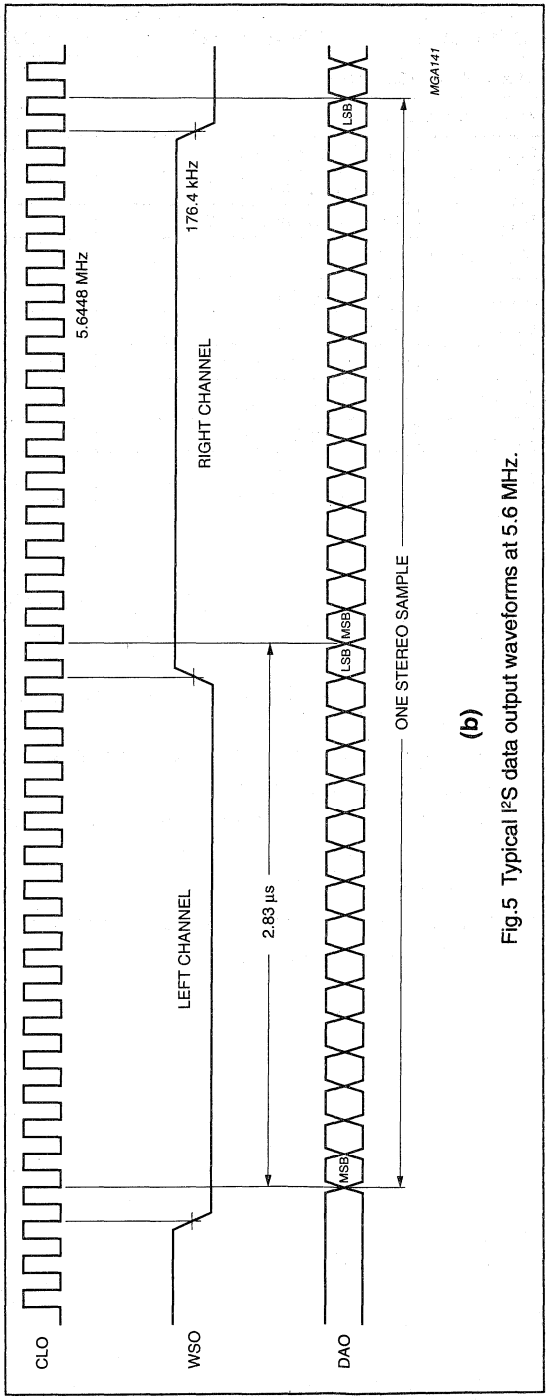
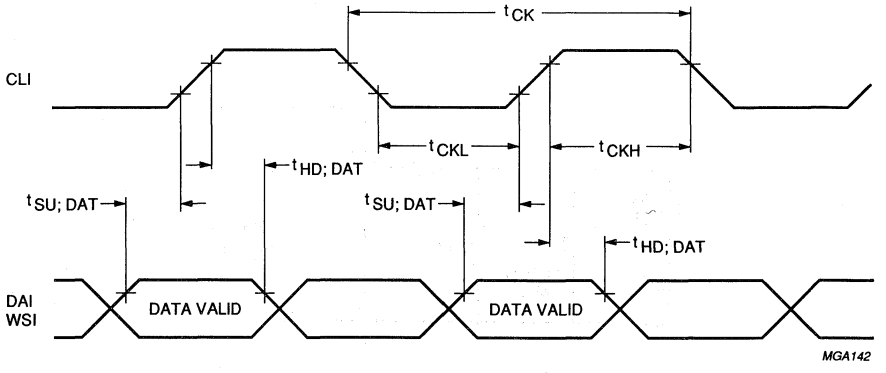
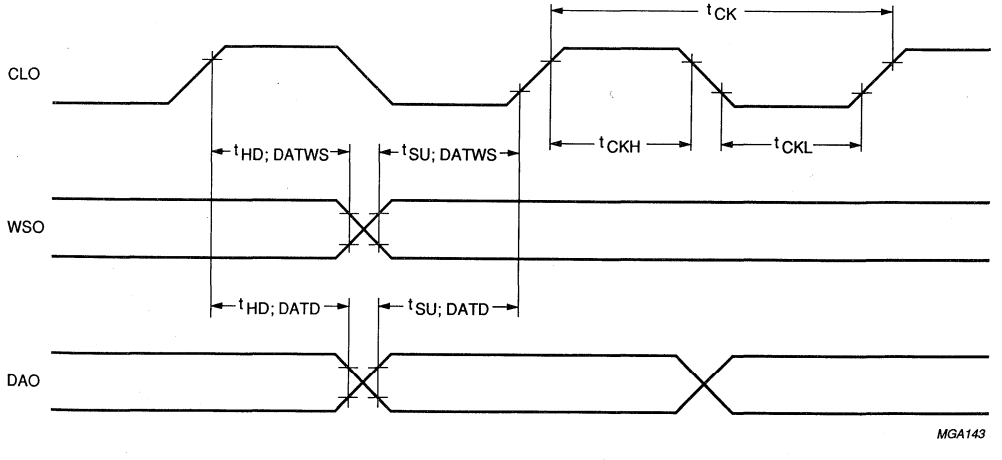


Fig.5 Typical I²S data output waveforms at 5.6 MHz.



Reference levels = 0.8 V and 2 V.

Fig.6 Data input timing with respect to I²S serial bit clock input (CLI).



Reference levels = 0.8 V and 2 V.

Fig.7 Data output timing with respect to clock output (CLO).

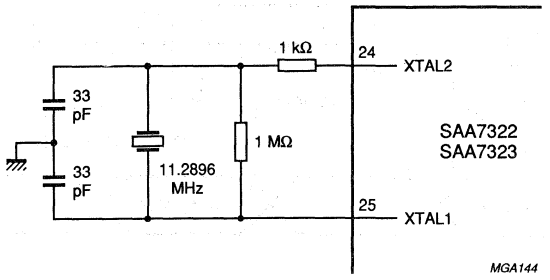


Fig.8 Crystal oscillator circuit using crystal type: 4322 143 05031.

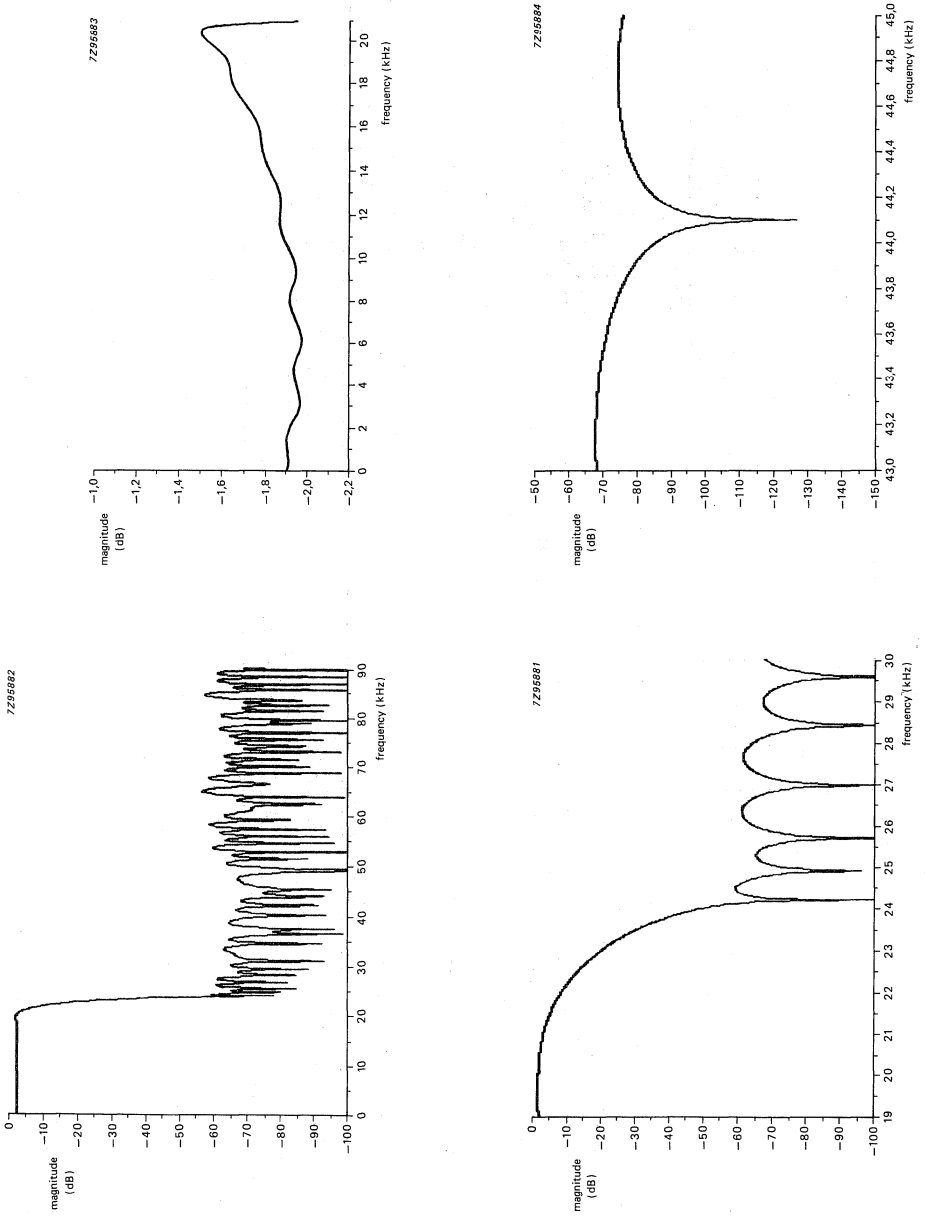


Fig.9 Digital filter characteristics; magnitude as a function of frequency.

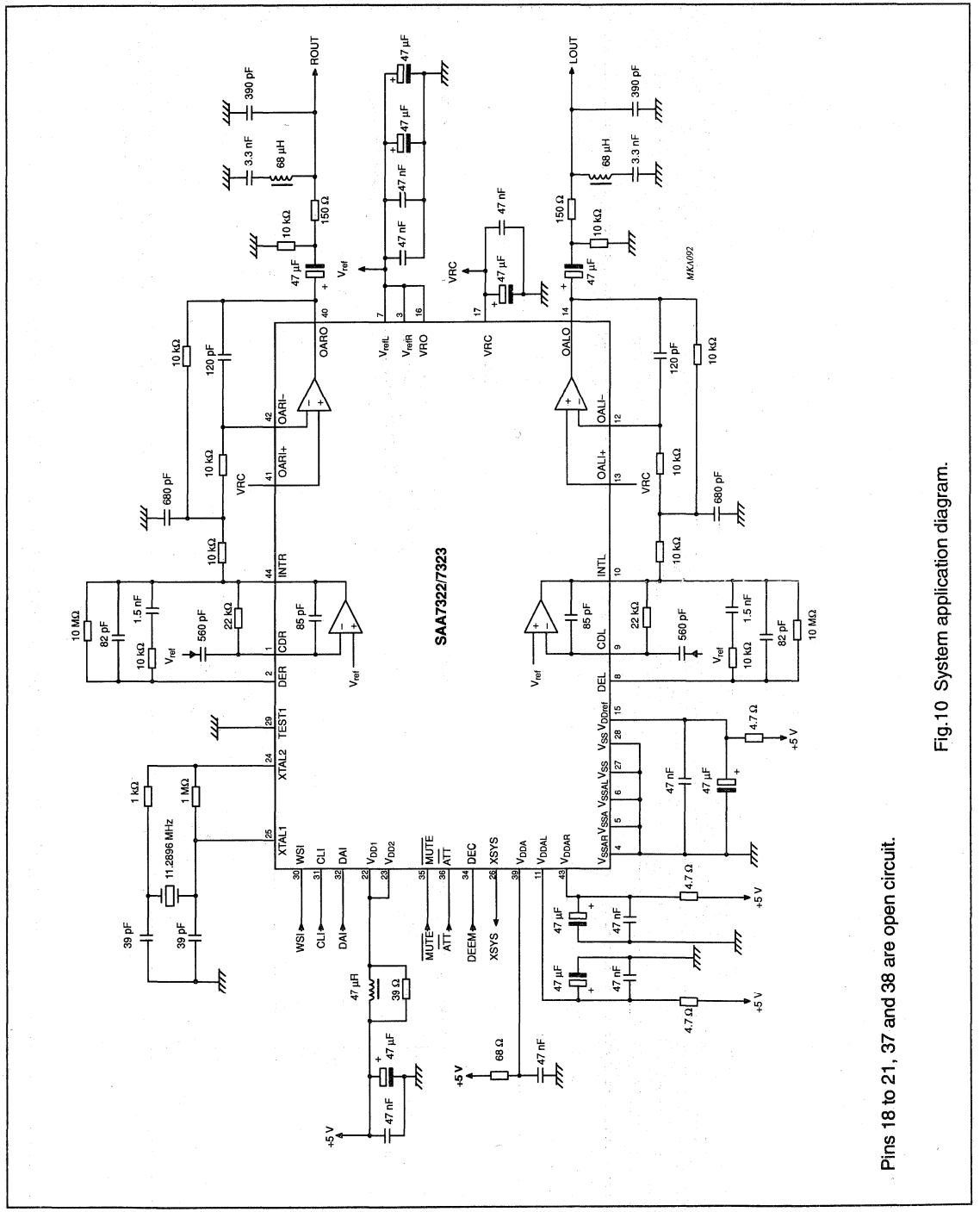


Fig.10 System application diagram.

Pins 18 to 21, 37 and 38 are open circuit.

CMOS Digital decoding IC for Compact Disc

SAA7341

FEATURES

- Analog front end (data slicer, phase detector, VCO)
- Demodulator and EFM decoding
- Subcoding microprocessor handshaking protocol
- Integrated programmable motor speed control
- Single/four wire motor operation option
- Bidirectional data bus to external SRAM (8k x 8 bits)
- Error correction and concealment functions
- IEC/EBU digital output
- 192 x oversampling via 2-stage digital filter
- 2nd order noise shaping
- One-bit DAC with 1.4 V (RMS)
- Attenuation, mute and de-emphasis functions
- Power-on reset and standby functions

GENERAL DESCRIPTION

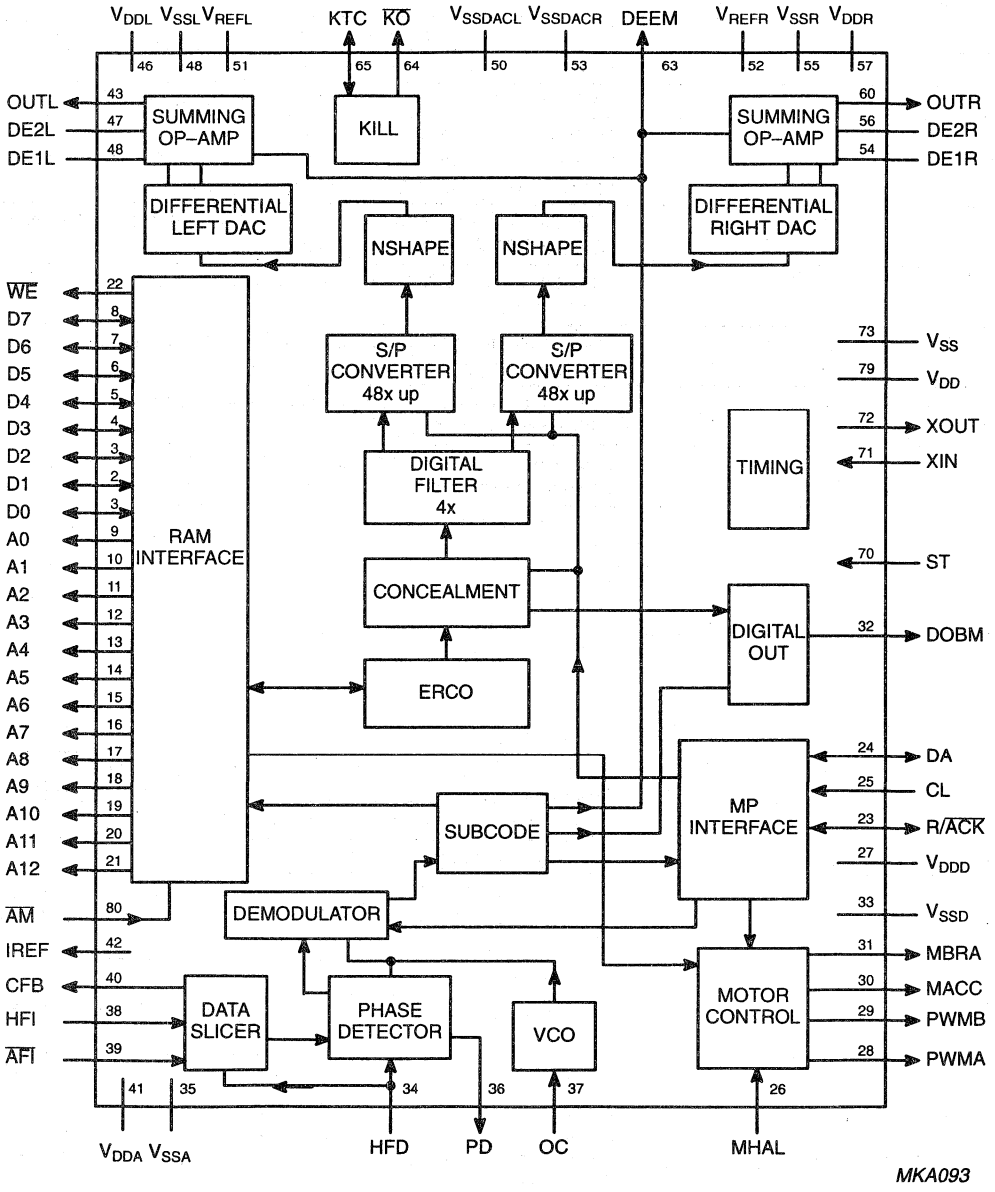
The SAA7341 incorporates the functions of decoding, digital filtering, and differential Digital-to-Analog conversion all on one CMOS IC. The device is specifically aimed at the mid-low end CD market, suitable for portable and car type applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
I_{DD}	supply current	-	60	-	mA
f_{XTAL}	crystal frequency range	15.24	16.9344	18.63	MHz
T_{amb}	operating ambient temperature range	–40	-	+85	°C
T_{stg}	storage temperature range	–55	-	+150	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7341GP	80	QPF	plastic	SOT219



Test pins (numbers 66 to 69, 74 to 78) not shown

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D0 to D7	1 to 8	data inputs/outputs to external RAM
A0 to A12	9 to 21	address outputs to external RAM
$\overline{WE}$	22	write enable: output signal to external RAM (active LOW)
R/$\overline{ACK}$	23	request/acknowledge: input/output microprocessor interface; this pin has an open drain output with internal pull-up of 50 kΩ; input is debounced by two 4.2336 MHz clock cycles
DA	24	microprocessor interface data input/output line; input is debounced by two 4.2336 MHz clock cycles
CL	25	microprocessor interface clock input debounced by two 4.2336 MHz clock cycles
MHAL	26	Hall effect detector for motor: input for motor reversal, with internal pull-up of 50 kΩ
V_{DDD}	27	+5 V supply for digital audio output (DOBM) and motor speed control (MSC) output buffers
PWMA	28	pulse width modulated motor control acceleration signal: output active during acceleration; single ended mode output
PWMB	29	pulse width modulated motor control brake signal: output active during braking
MACC	30	motor accelerate signal output
MBRA	31	motor brake signal output
DOBM	32	biphase-mark digital audio output: this output conforms to the format defined by IEC 958
V_{SSD}	33	ground for digital audio output (DOBM) and motor speed control (MSC) outputs
HFD	34	high-frequency detector: when HIGH this input enables the fine frequency and phase detector outputs and also the feedback from the data slicer; this input has an internal pull-up of 50 kΩ
V_{SSA}	35	analog ground for front end
PD	36	phase detector: the phase detector output and fine/coarse frequency outputs are combined internally and the resultant signal controls the VCO frequency
OC	37	VCO control input
HFI	38	non-inverting data slicer input; normally AC-coupled to EFM data source
$\overline{HFI}$	39	inverting data slicer input; normally connected via external capacitor to ground of EFM data source
CFB	40	data slicer feedback output to capacitor: disabled when a data run length violation is detected or HFD is LOW to stop the slicing level from drifting
V_{DDA}	41	+5 V analog supply for front end
IREF	42	current reference output: reference current for internal curr ent sources, nominally 114 μA, requires external resistor connected to ground

SYMBOL	PIN	DESCRIPTION
OUTL	43	left channel output
n.c.	44	not connected
n.c.	45	not connected
V_{DDL}	46	+5 V analog supply for left channel integrator and operational amplifier
DE2L	47	pin 2 for external de-emphasis capacitor and resistor (left channel)
V_{SSL}	48	analog ground for left channel integrator and operational amplifier
DE1L	49	pin 1 for external de-emphasis capacitor and resistor (left channel)
V_{SSDACL}	50	analog ground for DAC (left channel)
V_{REFL}	51	internal reference voltage node for DAC left channel requiring an external decoupling capacitor
V_{REFR}	52	internal reference voltage node for DAC right channel requiring an external decoupling capacitor
V_{SSDACR}	53	analog ground for DAC (right channel)
DE1R	54	pin 1 for external de-emphasis capacitor and resistor (right channel)
V_{SSR}	55	analog ground for right channel integrator and operational amplifier
DE2R	56	pin 2 for external de-emphasis capacitor and resistor (right channel)
V_{DDR}	57	+5 V analog supply for the right channel integrator and operational amplifier
n.c.	58	not connected
n.c.	59	not connected
OUTR	60	right channel output
n.c.	61	not connected
n.c.	62	not connected
DEEM	63	output for external de-emphasis switches
$\overline{KO}$	64	output pulse (LOW) used to activate external kill circuit during power on/off
KTC	65	input/output connection to external capacitor used for the timing of the kill pulse at power on
TEST1 to 4	66 to 69	these output pins should be left open-circuit
$\overline{ST}$	70	standby mode, input active LOW. Internal 50 kΩ pull-up resistor
XIN	71	input from crystal oscillator or external clock input (16.9344 MHz typ.)
XOUT	72	output to clock crystal
V_{SS}	73	ground for digital section
TEST5	74	this output pin should be left open-circuit
TEST6 to 9	75 to 78	these input pins should be tied HIGH
V_{DD}	79	+5 V supply for digital section
$\overline{AM}$	80	this input pin is normally held HIGH; should track loss occur this pin should be taken LOW and then the data is corrupted before the FIFO stage; this pin has an internal 50 kΩ pull-up resistor

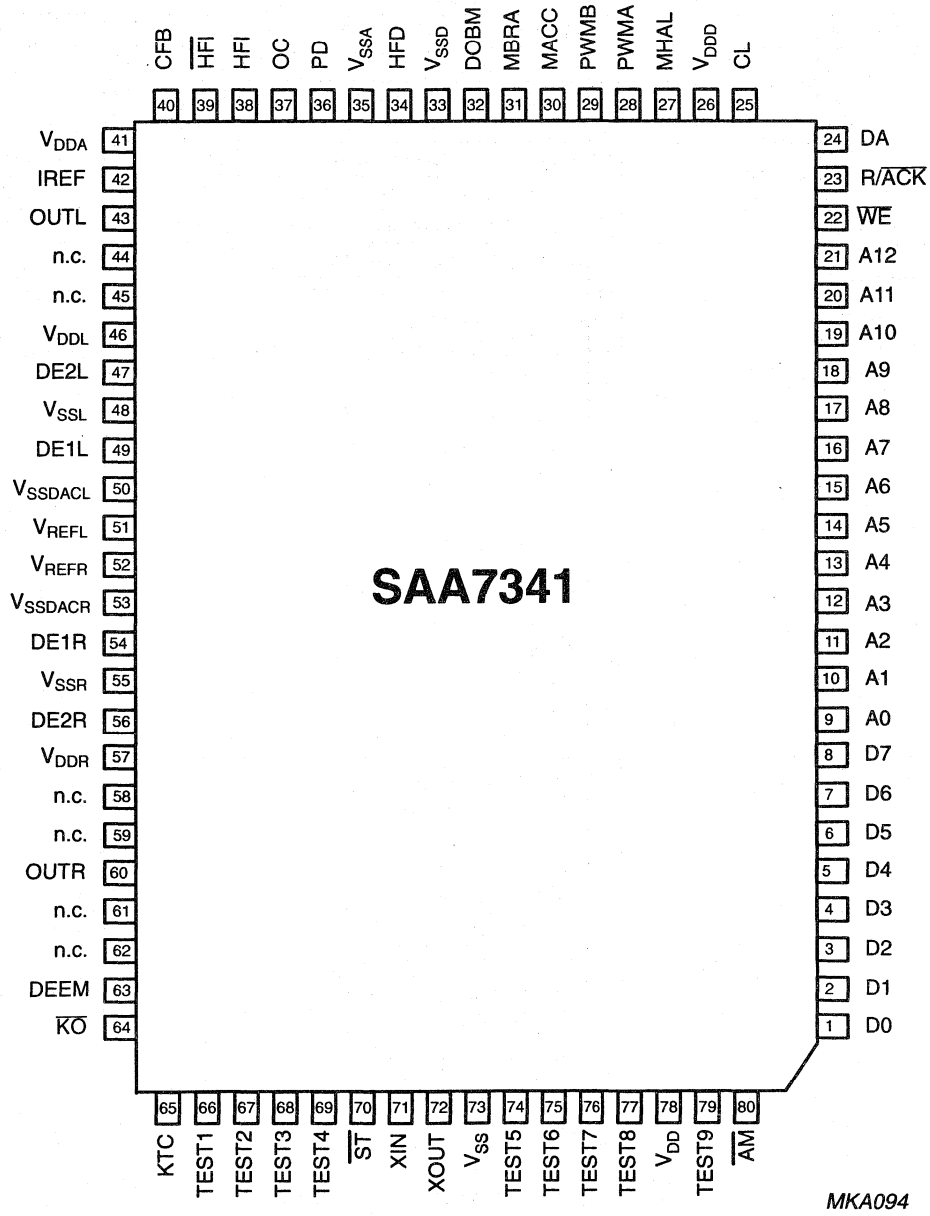


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Analog Front-End

The analog front-end contains the following functions: a data slicer, a VCO clock generator, fine and coarse frequency current switches and a current reference circuit.

The HFI input signal is converted to a digital signal by the data slicer. This is an adaptive level detector which relies on the DC-free nature of the modulation system to determine the optimum slicing level. When a signal drop-out is detected either externally via the HFD input or internally via the data run length violation detector, the feedback around the data slicer is disabled to stop the slicing level drifting.

Two (digital) frequency detectors and the phase detector provide coarse and fine control signals for the internal phase-locked-loop (PLL). The voltage controlled oscillator (VCO) is totally integrated, the frequency being dependent on the voltage at the OC pin. A coarse frequency detector compares the VCO frequency with the crystal clock and if necessary pulls the VCO to within the capture range of the fine frequency detector. This second detector uses data run length violations to pull the VCO further to within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled.

A separate current reference circuit is built in. An external resistor is needed at pin IREF (connected to V_{SS}).

Demodulator

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected master counter is only reset if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the master counter. During track jumping it is necessary to allow the master counter to free run to minimise interference to the motor speed controller. An out-of-lock signal indicates that no sync coincidences are found within a certain period. This signal enables the fine frequency detector when the HFD input is HIGH. When HFD is LOW the working of the fine frequency detector is disabled.

The EFM (eight-to-fourteen modulation) decoder converts each symbol into one of 256 8-bit binary words which are passed across the clock interface to the subcode section. An additional output from the EFM decoder senses both extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe is also passed across the clock interface.

Subcoding

The subcode section runs on a clock divided from the crystal clock while the demodulator uses the VCO clock.

The demodulator output word and timing signals are latched on an enable signal derived from the demodulator data sync. The output of this latch either goes to the subcode processor (first byte of frame) or goes to the external RAM during a WRITE1 cycle. Due to the extended accessibility of the external RAM for the WRITE1 cycles compared to previous decoders a pre-FIFO is not needed. There are 72 time slots to write an EFM data frame of 32 bytes. The nominal period between two bytes delivered by the EFM decoder is 3.93 µs. the longest period between two WRITE1 slots is 2.13 µs.

The Q-channel processor of the subcoding section accumulates a subcoding word of 96 bits from the Q-bit of the subcoding symbol. It performs a cyclic redundancy check (CRC) using up 16 bits. If the CRC is good and the data is requested by the external processor the remaining 80 bits are put on the DA output on an external clock (CL).

The de-emphasis control signal is derived from 1 bit of the CRC checked Q-channel. This goes to DEEM output. A de-bounce is added for extra protection.

Subcode words (without the P-bit) are clocked to the digital output section together with a sync flag and a CRC result flag. They are fed into the user channel of the DOBM output signal. The control bits of a Q-frame are also copied to the first four bits of a channel status block. Conforms to Annex A of IEC 958.

Microprocessor Interface

The SAA7341 interfaces with a microprocessor by means of a 3-line bus consisting of a request/acknowledge line (R/$\overline{\text{ACK}}$), a clock line (CL) and a data line (DA). The microprocessor can request Q-data from the SAA7341 or send control data for the motor speed control section.

Q-FRAME OUTPUT PROTOCOL

As long as the R/$\overline{\text{ACK}}$ line is held LOW by the microprocessor it can write control information to the SAA7341.

A Q-frame request is carried out when CL is HIGH by releasing the R/$\overline{\text{ACK}}$ line which should then go HIGH due to the pull-up resistor internal to the SAA7341. Figs 5 and 6 show the timing waveforms.

The SAA7341 is continually collecting Q-channel data and if it detects that R/$\overline{ACK}$ is HIGH it will hold the first frame of Q-data for which the CRC is good. It will then pull down R/$\overline{ACK}$ (acknowledge) and switch on the DA output. The microprocessor provides the clock to the CL input. After the first HIGH-to-LOW transition of CL, the SAA7341 will allow the R/$\overline{ACK}$ line to go HIGH. At the following HIGH-to-LOW transitions of CL the next Q-channel data bits will become available at the DA pin. As soon as the microprocessor has enough data (not necessarily 80 bits) it will pull R/$\overline{ACK}$ down again and the SAA7341 will disable DA and start collecting new Q-channel data.

If the microprocessor does not give a clock signal within 10.88 ms from the start of the acknowledge (R/$\overline{ACK}$ LOW) then the SAA7341 will reset the acknowledge signal and allow the R/$\overline{ACK}$ line to go HIGH again. After that the microprocessor still has 2.3 ms to accept the data. After a further 13.3 ms (typ.) the SAA7341 will have received a new Q-channel frame and if the CRC check is good a new acknowledge will be given.

Microprocessor data write protocol

The microprocessor can write data words into the 4-bit control registers of the SAA7341 when R/$\overline{ACK}$ is LOW. An 8-bit data burst on DA clocked with the positive edge of CL contains a 4-bit address (MSB first) and 4 bits of control data. It can be followed immediately by another burst of data without taking R/$\overline{ACK}$ HIGH.

Internally the receiver is reset when R/$\overline{ACK}$ is HIGH. The receiver will also be reset at stand-by and power-on. During the initialisation procedure the R/$\overline{ACK}$ line is held LOW by the SAA7341. When R/$\overline{ACK}$ becomes HIGH the SAA7341 is ready to receive data from the microprocessor.

A 2 bit debounce mechanism on CL and on the DA input protects the receiver against spikes.

Internal Control Registers

A set of 8 control registers hold the different system parameters for all types of applications. One register is used to control the audio processing (e.g. mute, −12 dB attenuation). Other registers hold the parameters for the spindle motor control loop.

Table 1 Internal control registers; the initial values are loaded during power-on

ADDRESS				DATA				INITIAL STATE			
msb			lsb								
A3	A2	A1	A0	D3	D2	D1	D0				
0	0	0	0	DIM	ANM	ATT	CRIB	1	1	1	1
0	0	0	1	TIM3	TIM2	TIM1	TIM0	0	1	1	1
0	0	1	0	OFS3	OFS2	OFS1	OFS0	0	0	0	0
0	0	1	1	OFS7	OFS6	OFS5	OFS4	1	1	1	0
0	1	0	0	STOP	STRT	STPM	PWMM	1	1	1	1
0	1	0	1	LEV3	LEV2	LEV1	LEV0	0	0	1	1
0	1	1	0	VEL	POS	INT	INH	1	1	1	1
0	1	1	1	GAIN3	GAIN2	GAIN1	GAIN0	0	0	0	0

Where:

DIM Digital mute. When HIGH the DAC outputs and the sample data in the digital output (DOBM) will be muted.

ANM Analog mute. When HIGH only the DAC output is suppressed. The digital output (DOBM) is not affected.

ATT Attenuate (-12dB). When HIGH the DAC outputs and sample data in the digital output (DOBM) are attenuated.

CRIB Counter reset inhibit. When CRIB is LOW the Demodulator master counter will free run.

The following signals are used in the motor control section:

TIM [3:0] Start time selector. The selected start time is loaded in a timer which determines the duration of the start pulse.

OFS [3:0] Low order nibble of accumulator offset.

OFS [7:4] High order nibble of accumulator offset.

STOP STOP signal.

STRT START signal.

STPM STOP Mode selection.

PWMM PWM mode selection.

LEV [3:0] Start/stop level selection. The selected level is the modulus of a constant value injected into the motor control output processor during start or stop. The sign is controlled by STRT/STOP (negative for STRT).

VEL Velocity branch selection. When HIGH the output of the velocity branch is added with the output of other selected branches.

POS Position branch selection. When HIGH the output of the position branch is added with the output of other selected branches.

INT Position integrator branch selection. When HIGH the output of the integrator is added with the output of other selected branches.

IHB Integrator hold. Signal to switch off the input of the integrator. When IHB is LOW the position information is added to the contents of the accumulator once per frame.

GAIN [3:0] Loop gain selection. The loop gain can be selected according to the application.

Error Correction (ERCO)

The error corrector (ERCO) carries out t = 1, e = 0 error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy t = 1, e = 0 means that the ERCO can correct one erroneous symbol per frame and detect all erroneous frames. As e = 0, no erasure corrections (to flagged symbols) are carried out.

The error corrector also contains the Flag Processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags. There are no input flags for C1.

Concealment

The concealment section performs the following functions:

- Up to 6 sample interpolation in each channel to conceal erroneous data flagged by the error corrector. When more than 6 samples are corrupted the last good value will be held.
- Attenuation of −12 dB.
- Digital mute.
- Signal conditioning for filter section.

RAM Interface

The RAM interface section generates addresses for the external RAM in order to carry out the processing necessary to supply data in the correct manner to ERCO (for both C1 and C2 correction processes) and subsequently to the concealment section.

The data path involves entering and leaving the external RAM 3 times. These operations are:

- FIFO and "small d" de-interleaving between SUBCODE and C1.
- "Large D" de-interleaving between C1 and C2.
- De-scrambling between C2 and CONCEALMENT.

In addition to the data operations, flags generated by the C1 and C2 correction processes are also processed by the RAM interface section. C1 output symbol flags receive the same de-interleaving processing as C1 output data, before being supplied to C2. C2 flags are also passed through the de-scrambling process but receive one frame less delay than the corresponding C2 output data before being supplied to the concealment section. This enables the concealment section to initiate a jump action by the RAM interface to fetch the next good sample from the RAM when the flagged data needs to be interpolated.

External RAM Timing

The external RAM is an 8k x 8 static CMOS RAM. An SAA7341 RAM address cycle takes nominally 236.2 ns. The write cycles are $\overline{WE}$ controlled. The RAM interface timing waveforms are shown in Fig.4.

Digital Audio Output (DOBM)

The biphase-mark digital output signal is according to the format defined by IEC 958. The clock frequency for this section is 5.6448 MHz (one third the crystal frequency).

Format

The digital audio output consists of 32 bit words ("subframes") transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384.

Each word contains information as shown in Table 2.

Table 2 Word information

PARAMETER	BIT	DESCRIPTION
sync	1 to 4	-
auxiliary	1 to 4	not used; always zero
audio sample	9 to 28	first 4 bits not used (always zero); two's compliment; LSB = bit 13, MSB = bit 28
validity flag	29	valid = logic 0
user data	30	used for subcode data (Q-W)
channel status	31	control bits and category code
parity bit	32	even parity for bits 5 to 31

SYNC

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:

Sync B	Start of a block (384 words), word contains left sample.
M	Word contains left sample (no block start).
W	Word contains right sample.

AUDIO SAMPLE

Left and right samples are transmitted alternately. Audio samples are available for DOBM in the concealment section after interpolation, attenuation and muting.

VALIDITY FLAG

Audio samples are flagged when they are not the original samples after error correction. The validity flag is logic 1 when the audio sample is the result of interpolation, muting or attenuation.

USER DATA

Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

CHANNEL STATUS

The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is as shown in Table 3.

Table 3 Bit assignment

PARAMETER	BIT	DESCRIPTION
control	1 to 4	copy of CRC checked Q-channel
reserved mode	5 to 8	always zero
category code	9 to 16	CD: bit 9 = logic 1, all other bits = logic 0
remaining	17 to 192	always zero

DIGITAL FILTER

The digital filter is a 4 times oversampling recursive interpolation filter. It is constructed of 2 cascaded bireciprocal wave low-pass filters operating on a clock frequency of 4.2336 MHz. The sampling rates are 44.1 kHz and 88.2 kHz respectively.

The filter receives 16 bit samples from the concealment section. The output of the filter is scaled in such a way that a sinewave with maximum amplitude at the input can never cause overflow in the noise shaper.

The serial outputs of the digital filter contain 20 bit data samples at a rate of 176.4 kHz. Left and right samples are converted to parallel and held for 48 cycles of 8.4672 MHz.

The analog mute signal set via a microprocessor control register is synchronized to a sample. When it is HIGH the input of the converter is zero.

The second order digital noise shaper operates at a rate of 8.4672 MHz which is 192 times the sampling frequency. Overflow is prevented by a clipping mechanism. The 1-bit output of the noise shaper is connected to the DAC. There are two noise shapers, one for each channel.

Table 4 Filter characteristics

PARAMETER	VALUE (dB)	FREQUENCY (kHz)
passband ripple	–0.1 to 0	0 to 20
transition band	monotonic –3 –14	20 to 26 22.05 24
stopband attenuation	<–30 <–35	26 to 88.2 40 to 65
roll off due to sinx/x	0.18	-

D/A Conversion

The 1-bit output of the noise shaper is converted to an analog signal by a 1-bit differential switched-capacitor integrator.

The differential outputs are summed by an internal operational amplifier.

Kill, Power-on Reset and Standby Functions

A kill signal is available from the $\overline{KO}$ output to activate an external kill circuit when required.

A power-on reset signal is derived from the external capacitor on KTC to initialize some of the internal control signals.

The SAA7341 can be put in standby mode to achieve silence at the outputs (except for XOUT) when the CD function in a combination player (music centre) is switched off. Also interference and power consumption will be minimized in the standby mode.

Spindle Motor Control Section

The motor control section uses the FIFO phase information from the RAM addressing section and disc speed information to calculate the motor control output signals. This calculation is performed at a rate of 7.35 kHz. The master clock of this section is 4.2336 MHz.

The motor control loop contains three branches : velocity, position and integrated position. These branches can be switched off independently by the microprocessor.

The outputs that drive the motor are MACC, MBRA, PWMA and PWMB. MACC and MBRA are active (HIGH) when the motor has to be accelerated or braked respectively. PWMA and PWMB are pulse width modulated signals with a frequency of 22.05 kHz of which the duty cycle controls the strength of the acceleration (PWMA) or braking effect (PWMB). In a second selectable PWM-mode only one output (PWMA) is used.

By means of a 4-bit control register the following 5 modes of operation are possible :

- PASSIVE (motor control loop switched off)
- START (accelerate for a set time before PLAY takes over)
- PLAY (PLL motor on)
- BRAKE (braking unit told otherwise by microprocessor)
- STOP1 (braking until disc stopped then PASSIVE)

A block diagram of the motor control loop, including the microprocessor registers, is shown in Fig.8.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage; note 1	−0.5	+6.5	V
V_I	maximum input voltage	−0.5	V_{DD} + 0.5	V
I_{REFabs}	input current, IREF only	-	+2	mA
I_{IK}	DE input diode current	-	±20	mA
V_O	output voltage	−0.5	+6.5	V
I_O	output current		±10	mA
T_{stg}	storage temperature range	−55	+150	°C
T_{amb}	operating ambient temperature range	−40	+85	°C
V_{es}	electrostatic handling; note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0; T_{amb} = 25° C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		4.5	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	-	60	-	mA
V_{SS}, V_{SSD}, V_{SSA}, V_{SSL}, V_{SSR}	ground	note 1	0	-	0	V
V_{DD}, V_{DDD}, V_{DDA}, V_{DDL}, V_{DDR}, V_{DDR}	positive supply voltage	note 1	4.5	5	5.5	V
Digital inputs						
$\overline{AM}$, $\overline{ST}$, MHAL, HFD						
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
V_{PU}	pull-up voltage	I_I = 0 µA	2.0	-	V_{DD} + 0.3	V
C_I	input capacitance		-	-	10	pF
R_I	internal pull-up resistor		15	50	100	kΩ
CL						
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	-	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_I	input capacitance		-	-	10	pF
XIN (EXTERNAL CLOCK)						
V_{IL}	input voltage LOW		−0.3	-	1.5	V
V_{IH}	input voltage HIGH		3.5	-	V_{DD} + 0.3	V
I_{LI}	input leakage current		−10	-	+10	μA
C_I	input capacitance		-	-	10	pF
Digital Input/Output						
D0 TO D7						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3V	
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	-	+10	μA
C_I	input capacitance		-	-	10	pF
DA						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	100	pF
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3V	
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	-	+10	μA
C_I	input capacitance		-	-	10	pF
R/$\overline{\text{ACK}}$						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
C_L	load capacitance		-	-	100	pF
R_I	internal pull-up resistor		15	50	100	kΩ
V_{IL}	input voltage LOW		−0.3	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{DD} + 0.3	V
V_{PU}	pull-up voltage	I_I = 0 μA	2.0	-	V_{DD} + 0.3	V
C_I	input capacitance		-	-	10	pF
Digital Outputs						
A0 TO A12						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
I_{LO}	3-state leakage current	V_O = 0 to V_{DD}	−10	0	10	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\overline{WE}$, DEEM						
V_{OL}	output voltage LOW	I_{OL} = +0.4 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = −0.2 mA	3.0	-	V_{DD}	V
C_L	load capacitance		-	-	50	pF
DOBM (SEE FIG. 3 FOR LOAD)						
$V_{O(p-p)}$	voltage across a 75 Ω load (peak-to-peak value)		0.4	-	0.6	V
MACC, MBRA						
V_{OL}	output voltage LOW	I_{OL} = +50 µA	0	-	0.3	V
I_{OH}	output current HIGH (constant source current)	V_O = 0 to 2 V	-	−1.5	-	mA
PWMA, PWMB						
V_{OH}	output voltage HIGH	I_{OH} = −50 µA	V_{DD} - 0.3	-	V_{DD}	V
I_{OL}	output current LOW (constant sink current)	V_O = 3 to V_{DD}	-	1.5	-	mA
Crystal Oscillator						
XIN, XOUT						
f_{XTAL}	crystal frequency		15.24	16.9344	18.63	MHz
g_m	mutual conductance at 100 kHz		1.5	-	-	mS
A_V	small signal voltage gain	$A_V = g_m.R_O$	3.5	-	-	V/V
C_I	input capacitance		-	-	10	pF
C_{FB}	feedback capacitance		-	-	5	pF
C_O	output capacitance		-	-	10	pF
Reference Voltage outputs						
VREFL, VREFR						
V_R	voltage reference		-	2.5	-	V
OUTPUT PERFORMANCE						
$V_{AO(RMS)}$	output level (RMS value)	note 2	-	1.4	-	V
S/N	signal-to-noise ratio	0 dB input	90	-	-	dB
THD	total harmonic distortion	0 dB/1 kHz	-	-	−70	dB
	(plus noise)	−10 dB/1 kHz	-	−80	-	dB
	channel matching	0 dB/1 kHz	−0.25	0	+0.25	dB
	crosstalk		-	−90	-	dB
PSRR	power supply rejection ratio		-	40	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Kill Circuit						
INPUT/OUTPUT: KTC						
	KTC switching level	KTC rising	-	3.0	-	V
		KTC falling	-	2.0	-	V
V_{OL}	output voltage LOW	$I_{OL} = 0$	0	-	0.4	V
R_I	internal discharge resistor	KTC = LOW	-	2	-	kΩ
I_{OH}	output current HIGH		-	10	-	µA
OUTPUT: $\overline{KO}$						
R_I	internal pull-down resistor		-	50	-	kΩ
V_{OH}	output voltage HIGH	$I_{OH} = 0$	V_{DD} - 0.2	-	-	V
V_{TK}	supply threshold for power on		-	1	-	V
V_{TPD}	supply threshold for power down		-	4.6	-	V
V_{HPD}	hysteresis of V_{TPD}		0	-	200	mV
Timing (note 3)						
RAM INTERFACE (SEE FIG. 4)						
t_{acc}	read access time (for external RAM)		-	-	150	ns
t_{wp}	write enable pulse		100	-	-	ns
t_{as}	address set-up time		0	-	-	ns
t_{wlz}	delay from falling edge of $\overline{WE}$ to data bus going low impedance	XIN = 16.9 MHz XIN = 18.6 MHz	35 30	- -	- -	ns ns
t_{wr}	write recovery time from rising edge of $\overline{WE}$		20	-	-	ns
t_{dw}	data valid before end of write		50	-	-	ns
t_{dh}	data hold time from rising edge of $\overline{WE}$		5	-	-	ns
MICROPROCESSOR INTERFACE (SEE FIGS 5, 6 AND 7)						
t_{an}	access time normal mode	note 4	0	-	n x 13.3	ms
t_{ar}	access time refresh mode	note 4	13.3	-	n x 13.3	ms
t_{da}	CL to RA acknowlege delay		-	0.9	2.0	µs
t_{rh}	CL to RA request hold time		2.0	-	-	µs
t_{cl}	CL input LOW time		2.0	-	-	µs
t_{ch}	CL input HIGH time		2.0	-	-	µs
t_{dd}	CL to DA delay time		-	0.9	2.0	µs
t_{ak}	acknowledge time	note 5	-	-	10.88	ms
t_{ah}	data hold time after acknowledge	note 6	2.31	-	-	ms
t_{ds}	microprocessor data set-up time to positive edge of CL		1.0	-	-	µs

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0; T_{amb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{dh}	microprocessor data hold time after positive edge of CL		2.0	-	-	µs
t_{drw}	delay to write after read		2.0	-	-	µs
t_{dwr}	delay to read after write		2.0	-	-	µs

Notes to the characteristics

1. All $V_{SS's}$ and all $V_{DD's}$ must be connected back to the ground and positive terminals of a single supply, respectively.
2. Maximum load recommended on OUTL, OUTR, is 5 kΩ, 100 pF. Device measured with external components shown in recommended application diagram (Fig.9). Maximum digital code.
3. Timing reference voltage levels are 0.8 V and 2.0 V.
4. Q-channel access times are dependent on the parity check on the Q channel data frame; n = the number of cycles until data is valid.
5. The acknowledge time is the time for which the SAA7341 will hold R/$\overline{ACK}$ LOW without the microprocessor driving CL LOW. The time is related to the frequency of the incoming data, and is therefore dependent on the frequency of the demodulation section. The value given is for demodulator operating at a nominal frequency of 4.32 MHz.
6. This is the amount of time for which the microprocessor can still successfully access the Q channel data after the SAA7341 has released R/$\overline{ACK}$ without CL going LOW. Again the time given is for demodulator operating at a nominal frequency of 4.32 MHz.

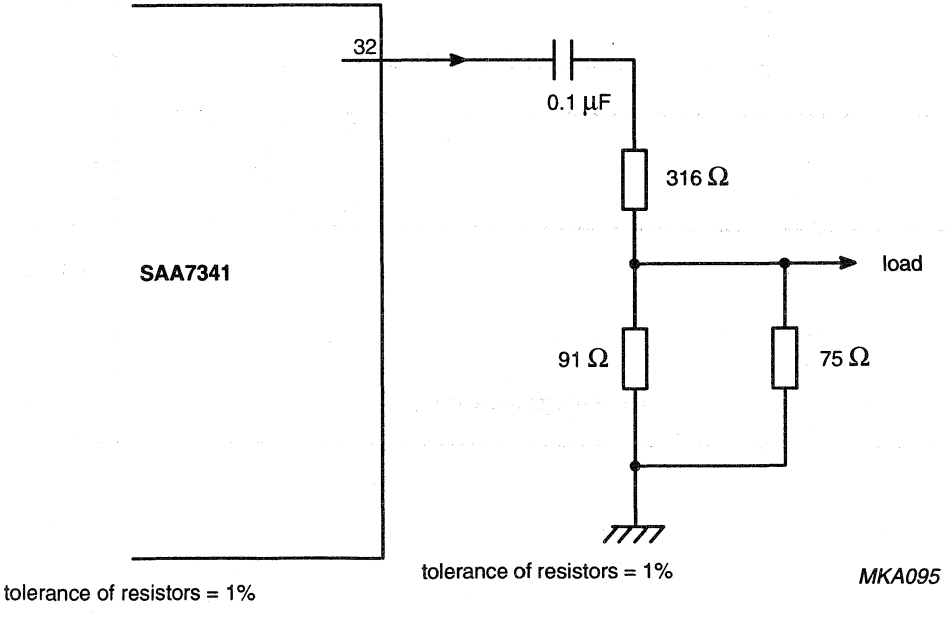


Fig.3 Digital audio output load.

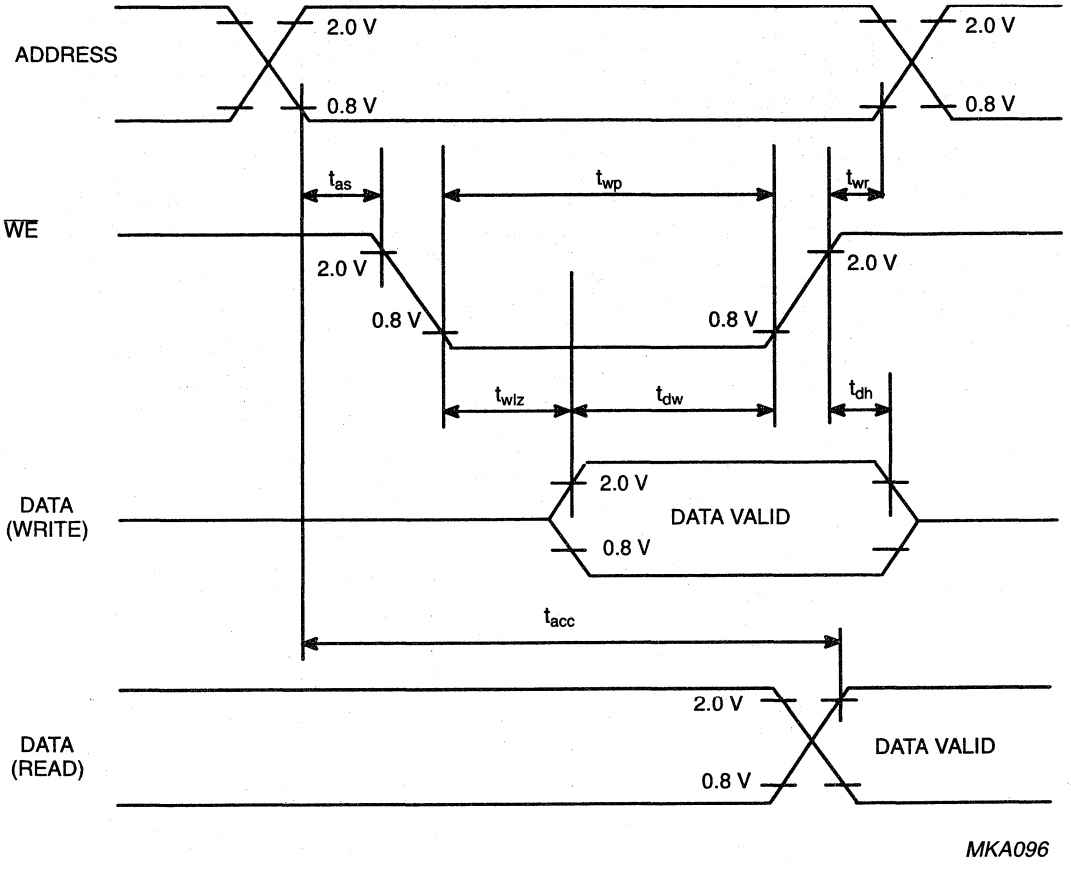


Fig.4 RAM interface timings.

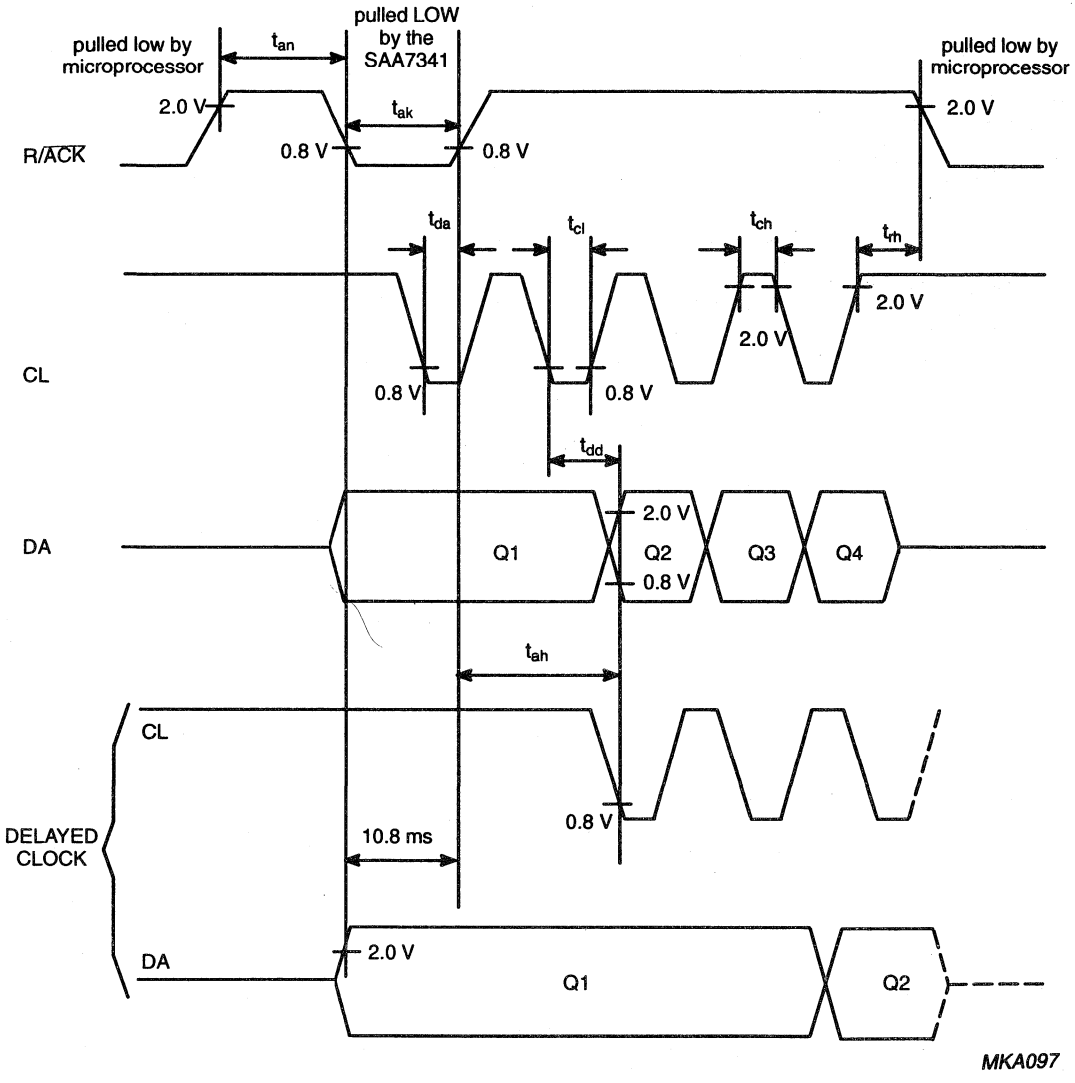


Fig.5 Q-channel timing wave forms (read mode).

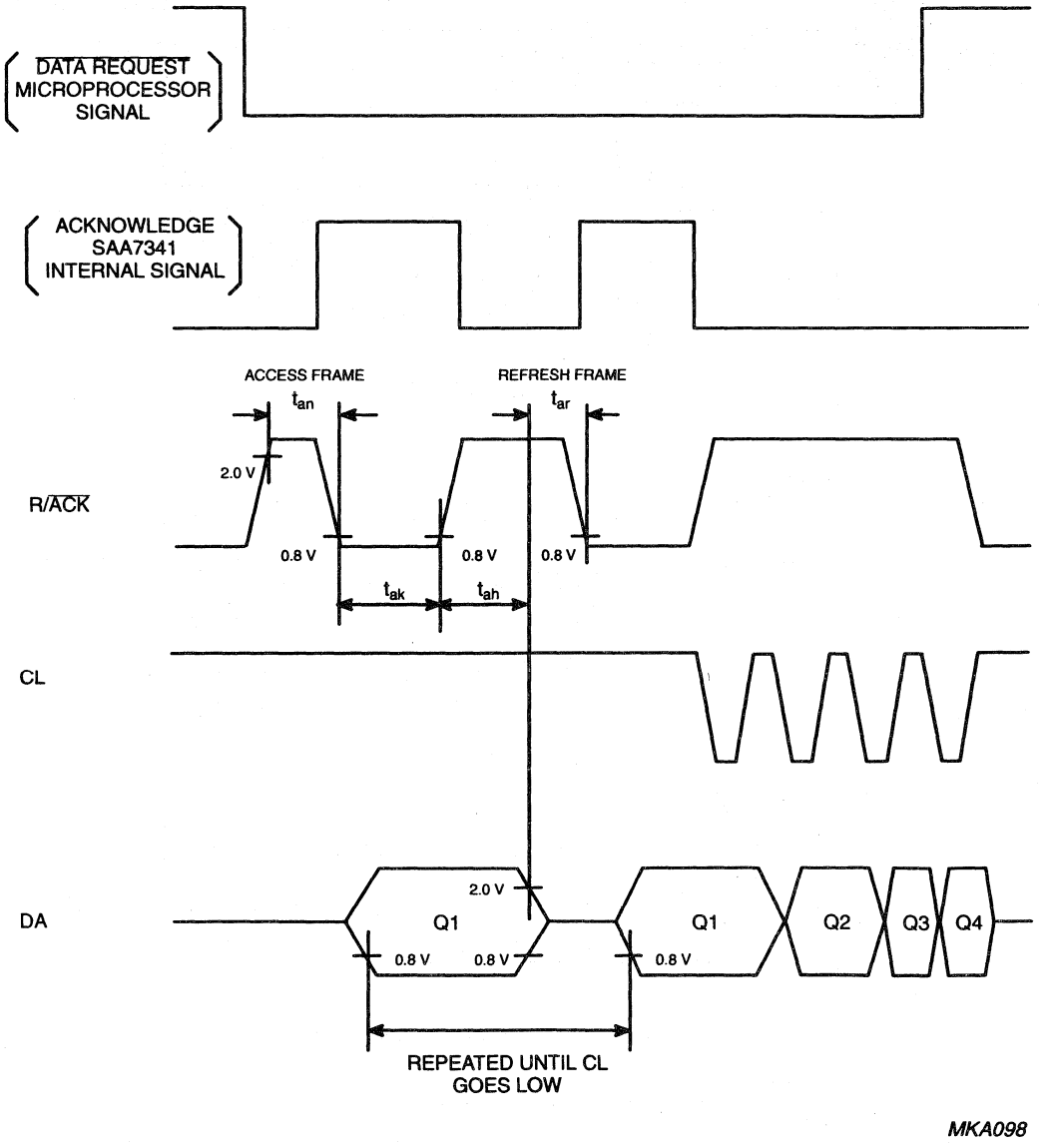


Fig.6 Q-channel timing waveforms (refresh mode).

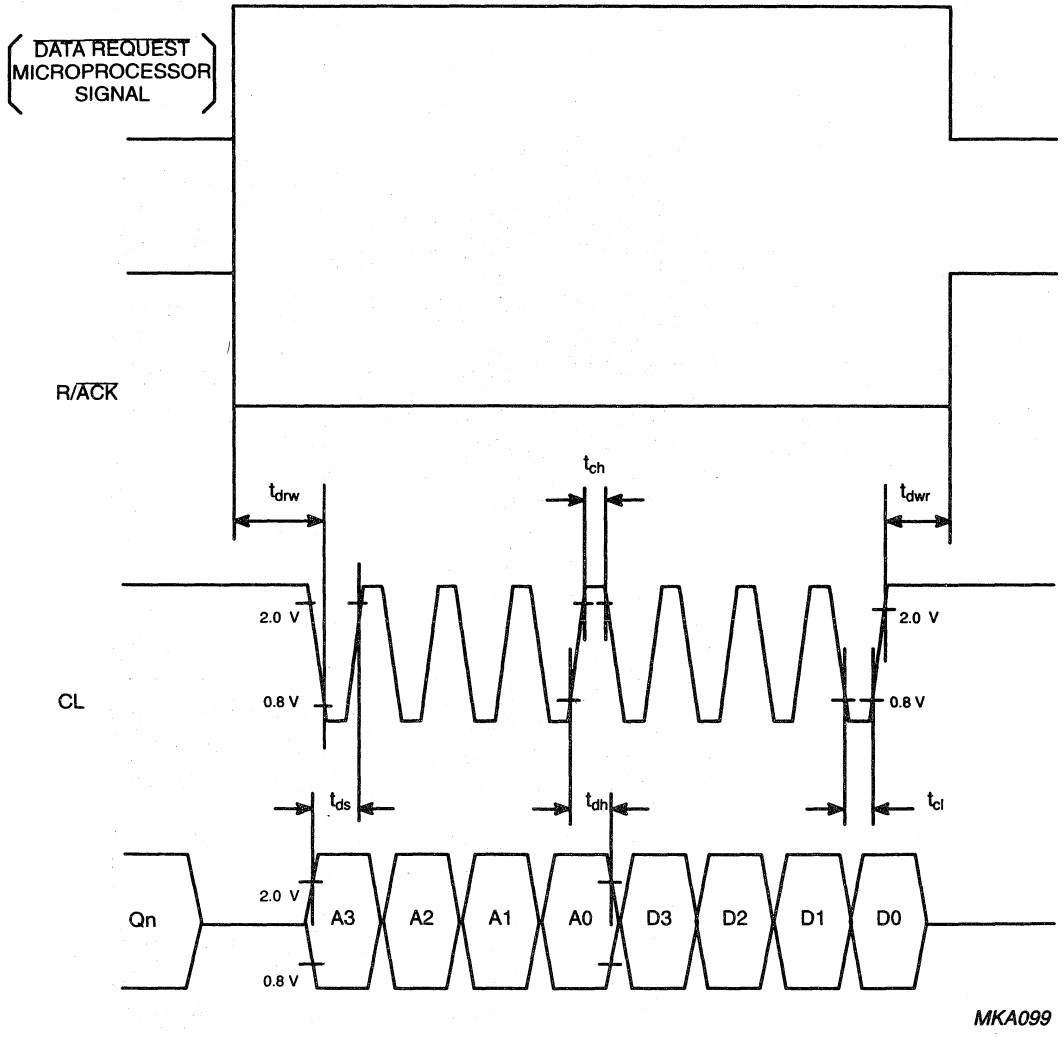


Fig.7 Microprocessor interface write mode.

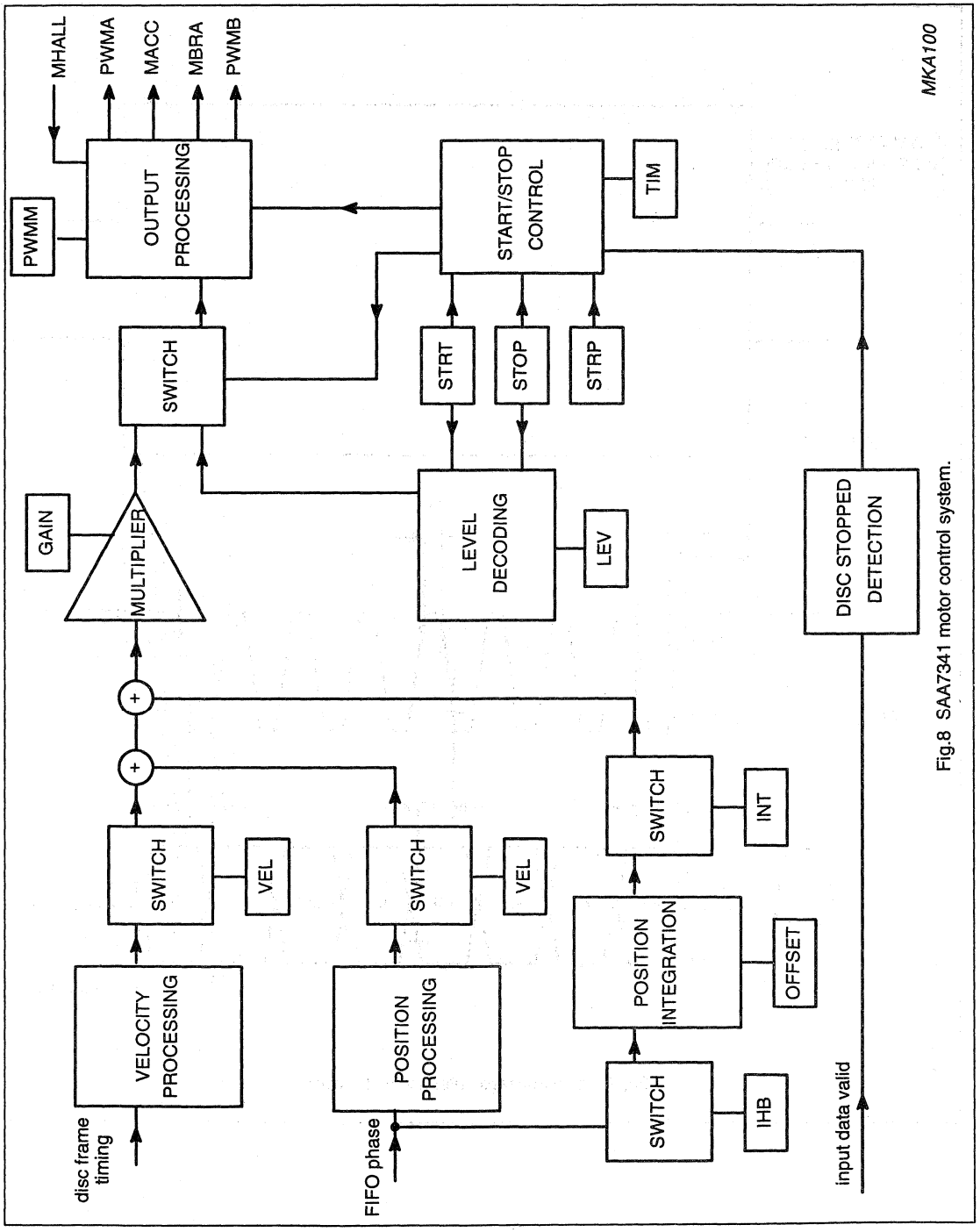


Fig.8 SAA7341 motor control system.

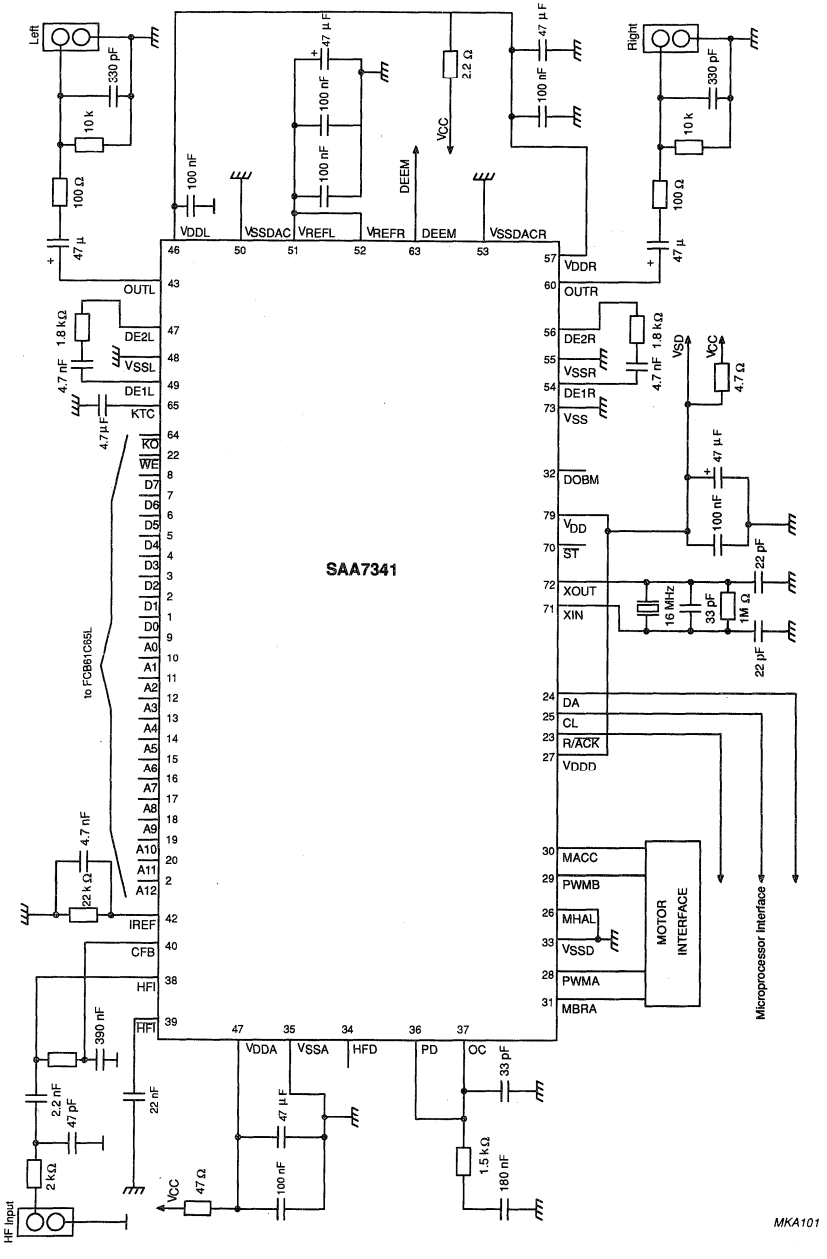


Fig.9 SAA7341 application circuit.

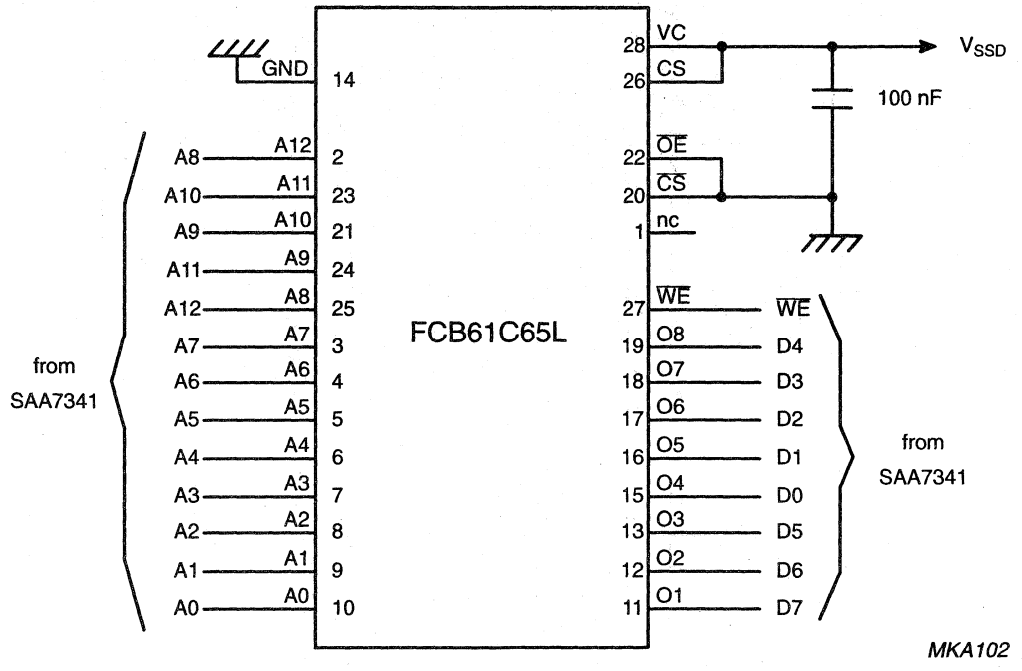


Fig.10 SRAM FCB61C65L configuration.

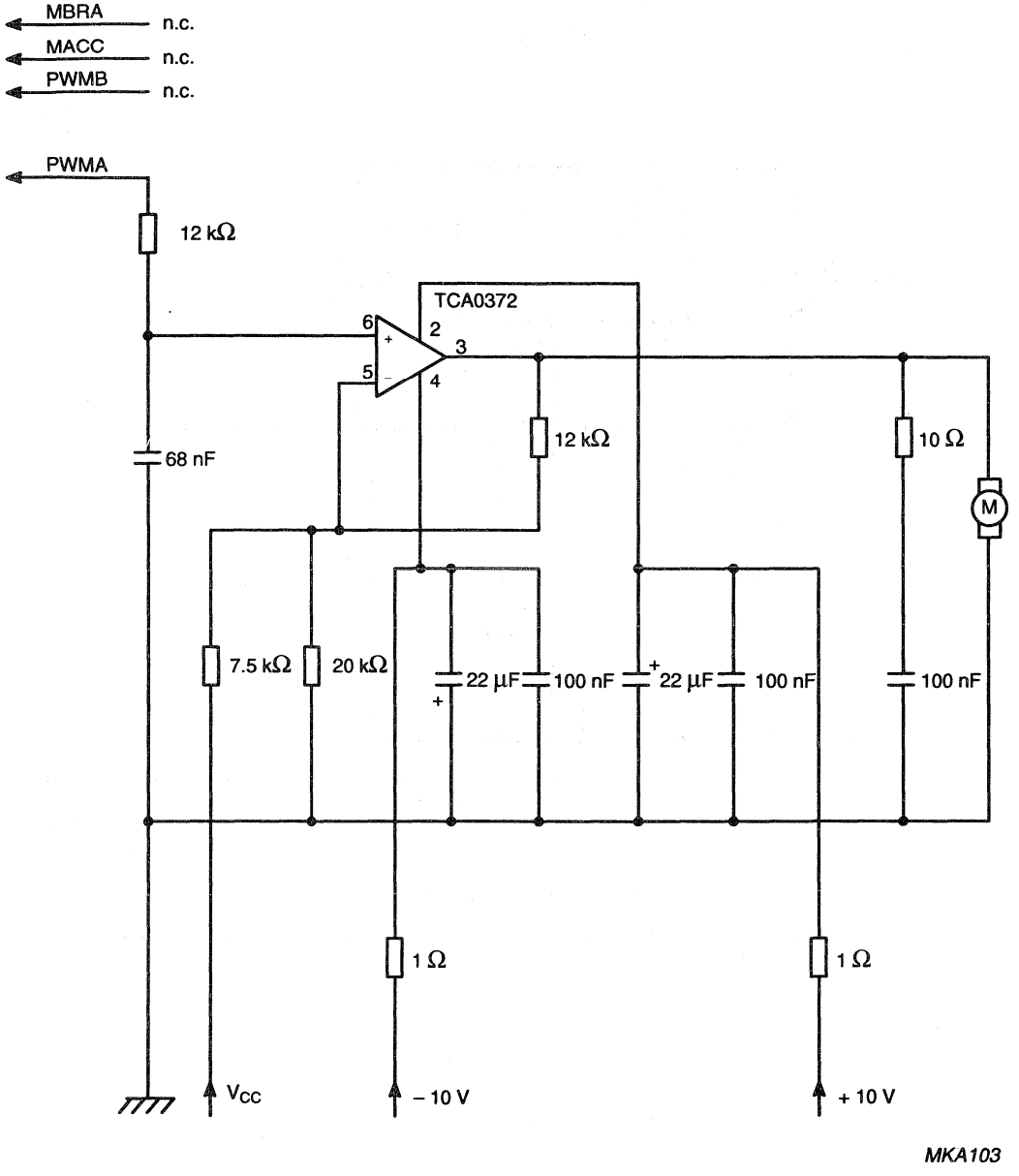


Fig.11 Motor interface; singled ended.

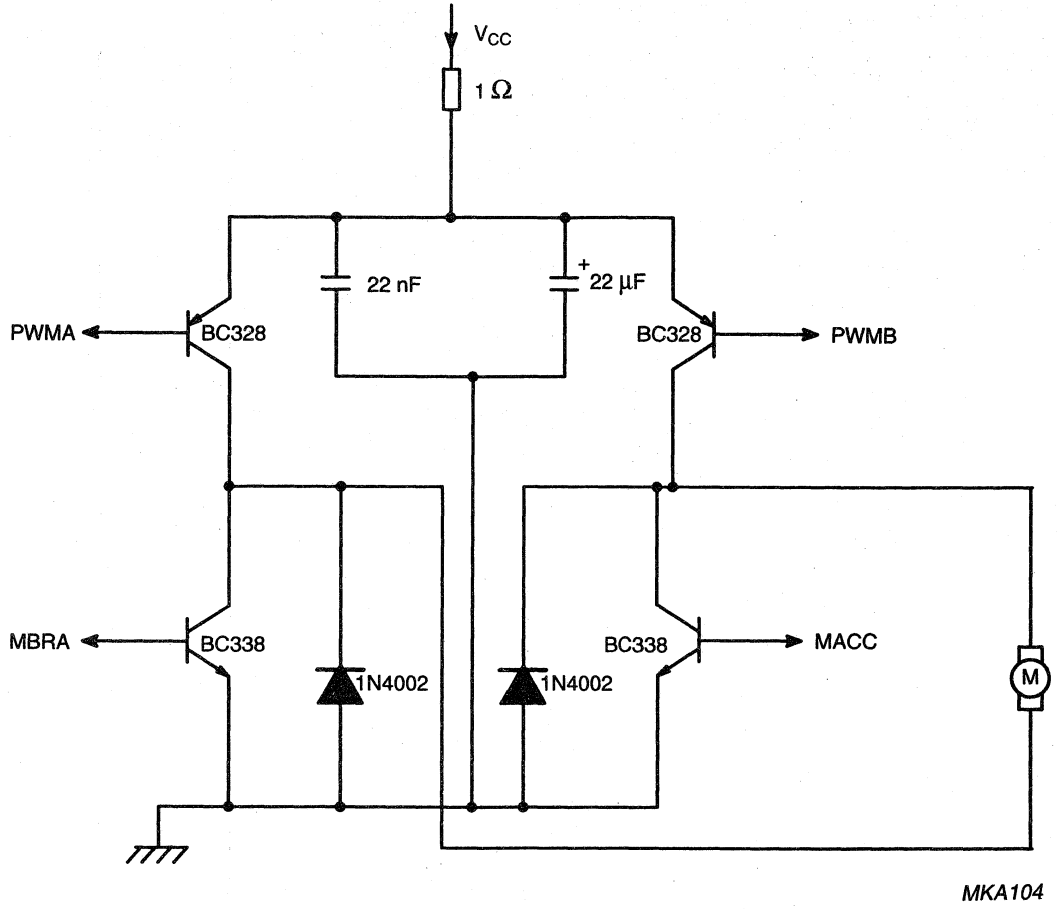


Fig.12 Motor interface; four wire.

CMOS Digital decoding IC with RAM for Compact Disc

SAA7345

FEATURES

- Integrated data slicer and clock regenerator
- Digital Phase-Locked Loop (PLL)
- Demodulator and EFM decoding
- Subcoding microprocessor serial interface
- Integrated programmable motor speed control
- Error correction and concealment functions
- Embedded SRAM for de-interleave and FIFO
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU)
- 2 to 4 times oversampling integrated digital filter
- Audio data peak level detection
- Versatile audio data serial interface
- Digital de-emphasis filter
- Kill interface for DAC deactivation during digital silence
- Double speed mode
- CD-ROM mode

GENERAL DESCRIPTION

The SAA7345 incorporates the CD signal processing functions of decoding and digital filtering. The device is equipped with on-board SRAM and includes additional features to reduce the processing required in the analog domain.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	3.4	5.0	5.5	V
I_{DD}	supply current	–	30	–	mA
f_{XTAL}	crystal frequency	8	16.9344 or 33.8688	35	MHz
T_{amb}	operating ambient temperature range	–40	–	+85	°C
T_{stg}	storage temperature range	–55	–	+125	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7345GP	44	QFP	plastic	SOT205A

CMOS Digital decoding IC with RAM for Compact Disc

SAA7345

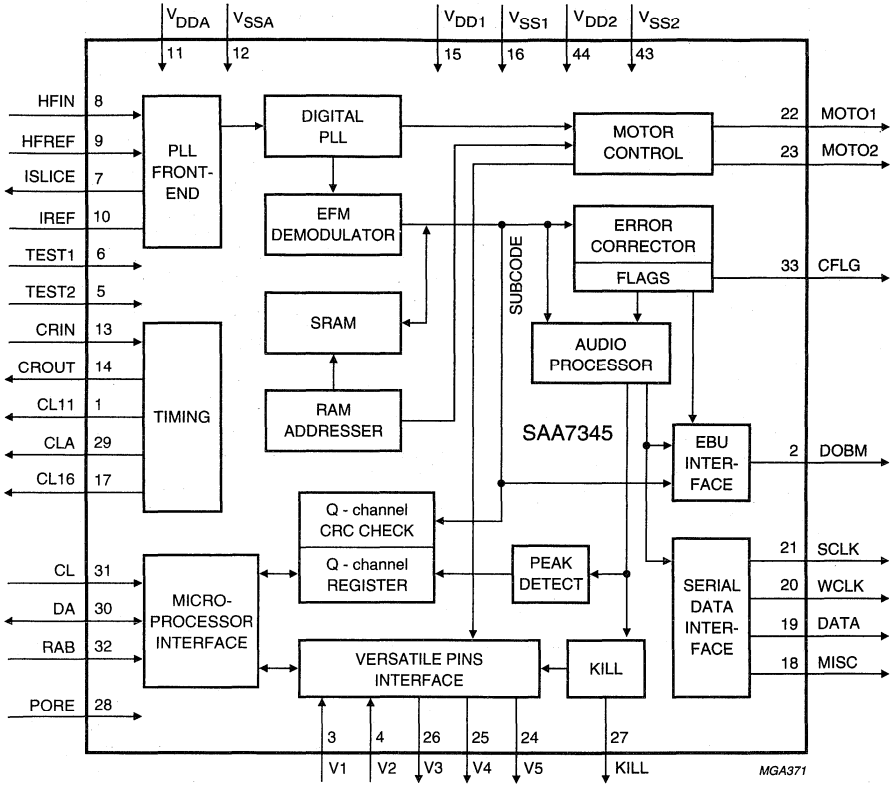


Fig.1 Block diagram.

CMOS Digital decoding IC with RAM for Compact Disc

SAA7345

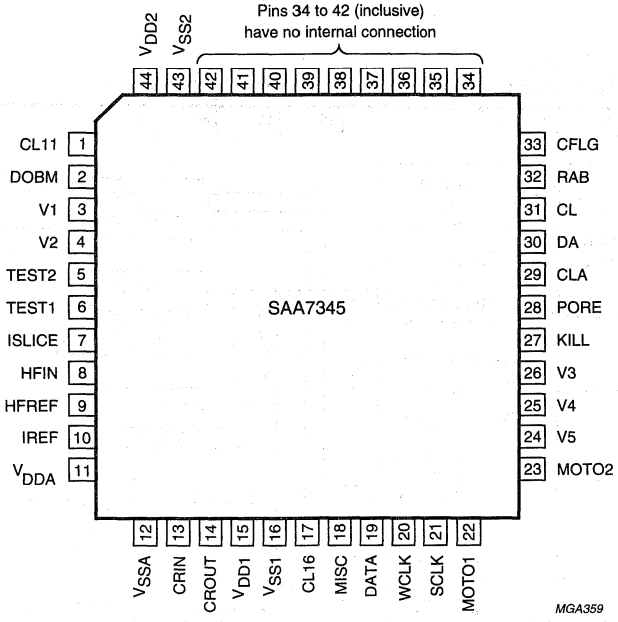


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
CL11	1	11.2896 MHz clock output (3-state)
DOBM	2	bi-phase mark output (externally buffered; 3-state)
V1	3	versatile input pin
V2	4	versatile input pin
TEST2	5	test input; this pin should be tied LOW
TEST1	6	test input; this pin should be tied LOW
ISLICE	7	current feedback from data slicer
HFIN	8	comparator signal input
HFREF	9	comparator common-mode input
IREF	10	reference current pin (nominally $V_{DD}/2$)
V_{DDA}	11	analog supply
V_{SSA}	12	analog supply
CRIN	13	crystal/resonator input
CROUT	14	crystal/resonator output
V_{DD1}	15	digital supply
V_{SS1}	16	digital supply
CL16	17	16.9344 MHz system clock output
MISC	18	general purpose DAC output (3-state)
DATA	19	serial data output (3-state)
WCLK	20	word clock output (3-state)
SCLK	21	serial bit clock output (3-state)
MOTO1	22	motor output 1; versatile (3-state)
MOTO2	23	motor output 2; versatile (3-state)
V5	24	versatile output pin
V4	25	versatile output pin
V3	26	versatile output pin (open-drain)
KILL	27	kill output; programmable (open-drain)
PORE	28	power-on reset enable input (active LOW)
CLA	29	4.2336 MHz microprocessor clock output
DA	30	interface data I/O line
CL	31	interface clock input line
RAB	32	interface R/$\overline{W}$ and acknowledge input
CFLG	33	correction flag output (open-drain)
	34-42	no internal connection
V_{SS2}	43	digital supply
V_{DD2}	44	digital supply

FUNCTIONAL DESCRIPTION

Data Slicer and Clock Regenerator

The SAA7345 has an integrated slice level comparator which is clocked by the crystal frequency clock. The slice level is controlled by an internal current source applied to an external capacitor under the control of the digital phase-locked loop (DPLL).

Regeneration of the bit clock is achieved with an internal fully digital PLL. No external components are required and the bit clock is not output. The PLL has two microprocessor control registers (addresses 1000 and 1001) for bandwidth and equalization.

For certain applications an offtrack input is necessary. If this flag is HIGH, the SAA7345 will assume that the servo is following on the wrong track, and will flag all incoming HF data as incorrect. The offtrack is input via the V1 pin when the versatile pins interface register (address 1100) bit 0 is set to 1.

2. The main counter is used to partition the EFM signal into 17-bit words. This counter is reset when
   (a) A Sync coincidence is generated
   (b) A sync is found within ±6 EFM clocks of its expected position

The Sync coincidence signal is also used to generate the Lock signal which will go active HIGH when 1 Sync coincidence is found. It will reset to LOW when, during 61 consecutive frames, no Sync coincidence is found. This Lock signal is accessed via the status signal when the status control register (address 0010) is set to x100. See section on microprocessor interface.

EFM demodulation

The 14-bit EFM data and subcode words are decoded into 8-bit symbols by a PLA.

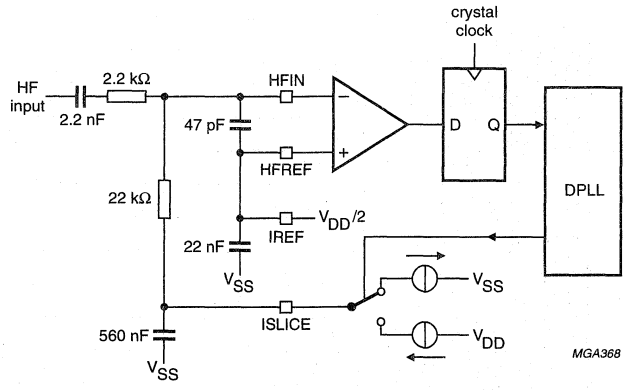


Fig.3 Data slicer showing typical application components.

Demodulator

FRAME SYNC PROTECTION

This circuit will detect the frame synchronization signals. Two synchronization counters are used in the SAA7345:

1. The coincidence counter which is used to detect the coincidence of successive syncs. It generates a Sync coincidence signal if 2 syncs are 588 ±1 EFM clocks apart.

Subcode data processing

Q-CHANNEL PROCESSING

The 96-bit Q-channel word is accumulated in an internal buffer. 16 bits are used to perform a Cyclic Redundancy Check (CRC). If the data is good, the SUBQREADY-I signal will go LOW. SUBQREADY-I can be read via the status signal when the status control register (address 0010) is set to x000 (normal reset condition). Good Q-channel data may be read via the microprocessor interface.

OTHER SUBCODE CHANNELS

Data of the other subcode channels (Q-W) may be read via the V4 pin if the versatile pins interface register (address 1101) is set to xx01.

The format is similar to RS232. The subcode sync word is formed by a pause of 200 µs minimum. Each subcode byte starts with a logic 1 followed by 7 bits (Q to W). The gap between bytes is variable between 11.3 µs and 90 µs.

The subcode data is also available in the EBU output (DOBM) in a similar format.

Microprocessor interface

The SAA7345 has a 3-line microprocessor interface which is compatible with the digital servo IC TDA1301.

WRITING DATA TO SAA7345

The SAA7345 has fifteen 4-bit programmable configuration registers as shown in Table 1. These can be written to via the microprocessor interface using the protocol shown in figure 5.

Write operation sequence:

- RAB is held LOW by the microprocessor to hold the SAA7345 DA pin at HIGH-impedance
- Microprocessor data is clocked into the internal shift register on the LOW-to-HIGH clock transition CL
- Data D(3:0) is latched into the appropriate control register (address bits A(3:0)) on the LOW-to-HIGH transition of RAB with CL HIGH
- If more data is clocked into SAA7345 before the LOW-to-HIGH transition of RAB then only the last 8 bits are used
- If less data is clocked into SAA7345, unpredictable operation will result
- If the LOW-to-HIGH transition of RAB occurs with CL LOW, the command will be disregarded

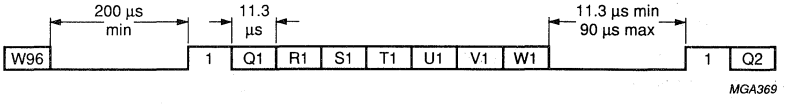


Fig.4 Subcode format and timing on V4 pin.

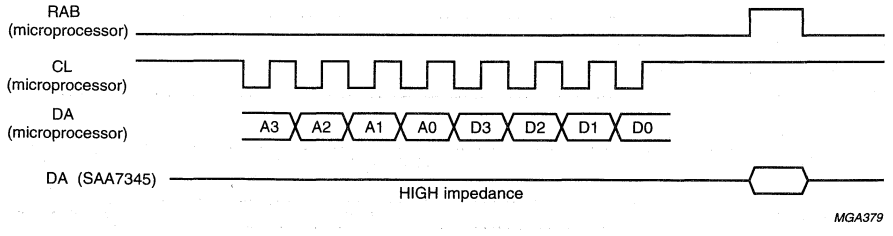


Fig.5 Microprocessor WRITE timing.

WRITING DATA TO SAA7345; REPEAT MODE

The same command can be repeated several times (e.g. for fade function.) by applying extra RAB pulses as shown in figure 6.

Note that CL must stay HIGH between RAB pulses.

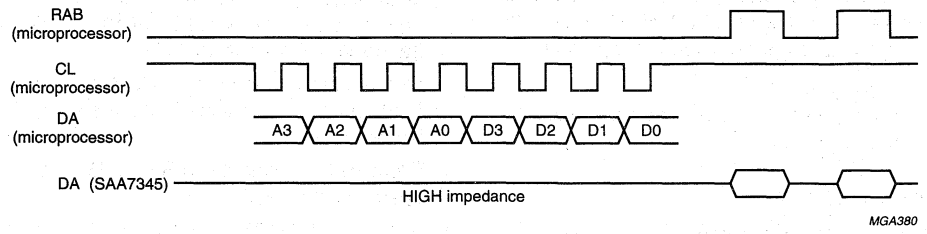


Fig.6 Microprocessor WRITE timing; repeat mode.

READING STATUS INFORMATION FROM SAA7345

There are several internal status signals which can be made available on the DA line. These are:

SUBQREADY-I	LOW if new subcode word is ready in Q-channel register
MOTSTART1	HIGH if motor is turning at 75% or more of nominal speed
MOTSTART2	HIGH if motor is turning at 50% or more of nominal speed
MOTSTOP	HIGH if motor is turning at 12% or less of nominal speed
PLL Lock	HIGH if Sync coincidence signals are found
V1	Follows input on V1 pin
V2	Follows input on V2 pin
MOTOR-OV	HIGH if the motor servo output stage saturates

The status signal to be output is selected by status control register (address 0010). The timing for reading the status signal is shown in figure 7.

Status read operation sequence:

- Write appropriate data to register 0010 to select required status signal
- With RAB LOW, set CL LOW
- Set RAB HIGH - this will tell SAA7345 to output status signal on DA

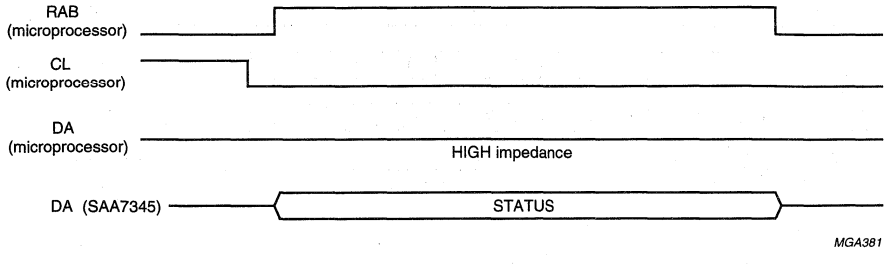


Fig.7 SAA7345 status READ timing.

READING Q-CHANNEL SUBCODE FROM SAA7345

To read Q-channel subcode from SAA7345, the SUBQREADY-I signal should be selected as status signal. The subcode read timing is shown in figure 8.

Read subcode operation sequence:

- Monitor SUBQREADY-I status signal
- When this signal is LOW, and up to 2.3 ms after its LOW-to-HIGH transition, it is permitted to read subcode
- Set CL LOW, SAA7345 will output first subcode bit (Q1)
- After subcode read starts, the microprocessor may take as long as it wants to terminate read operation
- SAA7345 will output consecutive subcode bits after each HIGH-to-LOW transition of CL
- When enough subcode has been read (1 to 96 bits), stop reading by pulling RAB LOW

PEAK DETECTOR OUTPUT

In place of the CRC-bits (bits 81 to 96), the peak detector information is added to the Q-channel data. The peak information corresponds to the highest audio level (absolute value) and is measured on positive peaks. Only the most significant 8 bits of the peak level are given, in unsigned notation.
Bits 81 to 88 contain the LEFT peak value (bit 88 = MSB) and bits 89 to 96 contain the RIGHT channel (bit 96 = MSB).

BEHAVIOUR OF THE SUBQREADY-I SIGNAL

When the CRC of the Q-channel word is good, and no subcode is being read, the SUBQREADY-I signal will react as shown in figure 9.

When the CRC is good and subcode is being read, the timing in figure 10 applies.

If t_1 (SUBQREADY-I LOW to end of subcode read) is below 2.6 ms, then t_2 = 13.1 ms (i.e. the microprocessor can read all subcode frames if it completes the read operation within 2.6 ms after subcode ready).

If this criterion is not met, it is only possible to guarantee that t_3 will be below 26.2 ms (approximately).

If subcode frames with failed CRC's are present, the t_2 and t_3 times will be increased by 13.1 ms for each defective subcode frame.

SHARING THE MICROPROCESSOR INTERFACE

When the RAB pin is held LOW by the microprocessor, it is permitted to put any signal on the DA and CL lines (SAA7345 will set output DA to HIGH impedance). Under this circumstance these lines may be used for another purpose (e.g. TDA1301 microprocessor interface Data and Clock line, see figure 11).

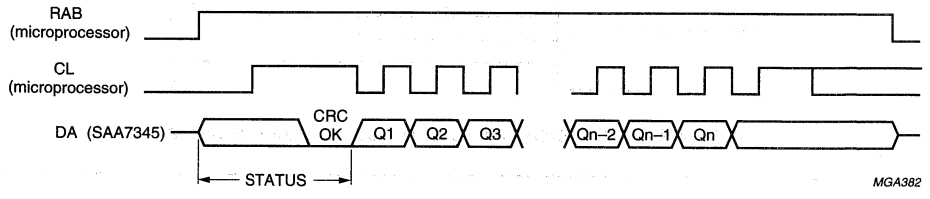


Fig.8 SAA7345 Q-channel subcode READ timing.

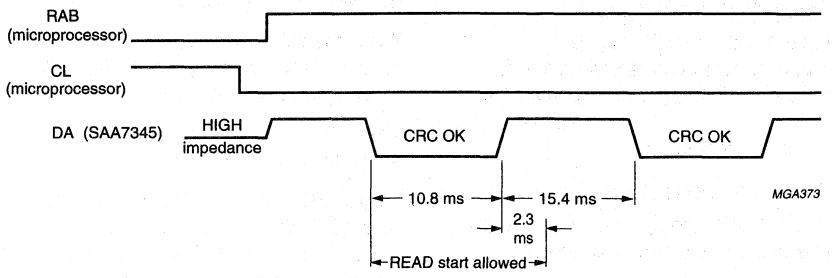


Fig.9 SUBQREADY-I timing when no subcode is read.

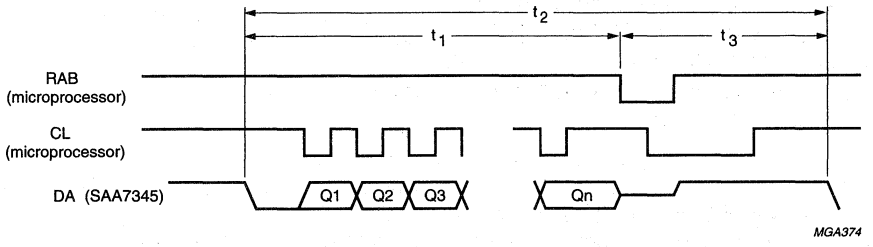


Fig.10 SUBQREADY-I timing when subcode is being read.

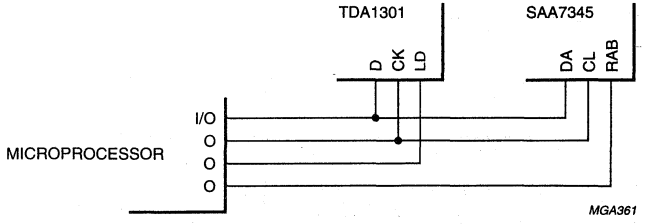


Fig.11 SAA7345 microprocessor interface application diagram.

Table 1 Command registers
The INITIAL column shows the power-on reset state

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
Fade and Attenuation	0 0 0 0	x 0 0 0	Mute	Reset
		x 0 1 x	Attenuate	
		x 0 0 1	Full Scale	
		x 1 0 0	Step Down	
		x 1 0 1	Step Up	
Motor mode	0 0 0 1	x 0 0 0	Motor off mode	Reset
		x 0 0 1	Motor brake mode 1	
		x 0 1 0	Motor brake mode 2	
		x 0 1 1	Motor start mode 1	
		x 1 0 0	Motor start mode 2	
		x 1 0 1	Motor jump mode	
		x 1 1 1	Motor play mode	
		x 1 1 0	Motor jump mode 1	
		1 x x x	anti-windup active	
		0 x x x	anti-windup off	Reset
Status control	0 0 1 0	x 0 0 0	status = SUBQREADY-I	Reset
		x 0 0 1	status = MOTSTART1	
		x 0 1 0	status = MOTSTART2	
		x 0 1 1	status = MOTSTOP	
		x 1 0 0	status = PLL Lock	
		x 1 0 1	status = V1	
		x 1 1 0	status = V2	
		x 1 1 1	status = MOTOR-OV	
		0 x x x	L channel first at DAC (WCLK normal)	Reset
		1 x x x	R channel first at DAC (WCLK inverted)	
DAC output	0 0 1 1	1 0 1 0	CD ROM mode	
		1 1 0 x	I^2S – 4 fs mode	Reset
		1 1 1 1	I^2S – 2 fs mode	
		1 1 1 0	I^2S – fs mode	
		0 0 0 x	Sony – 16-bit – 4 fs	
		0 0 1 1	Sony – 16-bit – 2 fs	
		0 0 1 0	Sony – 16-bit – fs	
		0 1 0 x	Sony – 18-bit – 4 fs	
		0 1 1 1	Sony – 18-bit – 2 fs	
		0 1 1 0	Sony – 18-bit – fs	

REGISTER	ADDRESS	DATA	FUNCTION			INITIAL
Motor gain	0 1 0 0	x 0 0 0	Motor gain G = 3.2			Reset
		x 0 0 1	Motor gain G = 4.0			
		x 0 1 0	Motor gain G = 6.4			
		x 0 1 1	Motor gain G = 8.0			
		x 1 0 0	Motor gain G = 12.8			
		x 1 0 1	Motor gain G = 16.0			
		x 1 1 0	Motor gain G = 25.6			
		x 1 1 1	Motor gain G = 32.0			
Motor bandwidth	0 1 0 1	x x 0 0	Motor f4 = 0.5 Hz			Reset
		x x 0 1	Motor f4 = 0.7 Hz			
		x x 1 0	Motor f4 = 1.4 Hz			
		x x 1 1	Motor f4 = 2.8 Hz			
		0 0 x x	Motor f3 = 0.85 Hz			Reset
		0 1 x x	Motor f3 = 1.71 Hz			
		1 0 x x	Motor f3 = 3.42 Hz			
Motor output configuration	0 1 1 0	x x 0 0	Motor power maximum 37%			Reset
		x x 0 1	Motor power maximum 50%			
		x x 1 0	Motor power maximum 75%			
		x x 1 1	Motor power maximum 100%			
		0 0 x x	MOTO1, MOTO2 pins 3-state			Reset
		0 1 x x	Motor PWM mode			
		1 0 x x	Motor PDM mode			
		1 1 x x	Motor CDV mode			
			Loop BW Hz	Int. BW Hz	Low-pass BW Hz	
PLL loop filter bandwidth	1 0 0 0	0 0 0 0	1640	525	8400	
		0 0 0 1	3279	263	16800	
		0 0 1 0	6560	131	33600	
		0 1 0 0	1640	1050	8400	
		0 1 0 1	3279	525	16800	
		0 1 1 0	6560	263	33600	
		1 0 0 0	1640	2101	8400	
		1 0 0 1	3279	1050	16800	Reset
		1 0 1 0	6560	525	33600	
		1 1 0 0	1640	4200	8400	
		1 1 0 1	3279	2101	16800	
		1 1 1 0	6560	1050	33600	

REGISTER	ADDRESS	DATA	FUNCTION	INITIAL
PLL loop filter equalization	1 0 0 1	0 0 0 1	PLL 30 ns over-equalization	
		0 0 1 0	PLL 15 ns over-equalization	
		0 0 1 1	PLL nominal equalization	Reset
		0 1 0 0	PLL 15 ns under-equalization	
		0 1 0 1	PLL 30 ns under-equalization	
EBU output	1 0 1 0	x x 0 0	EBU data before concealment	
		x x 1 0	EBU data after concealment and fade	Reset
		x x 1 1	EBU off – output LOW	
		x 0 x x	Level II clock accuracy (<1000 ppm)	Reset
		x 1 x x	Level III clock accuracy (>1000 ppm)	
		0 x x x	Flags in EBU off	Reset
		1 x x x	Flags in EBU on	
Speed control	1 0 1 1	1 x x x	double-speed mode	
		0 x x x	single-speed mode	Reset
		x 0 x x	33.869 MHz crystal present	Reset
		x 1 x x	16.934 MHz crystal present	
		x x 0 0	standby 1 : 'CD-STOP' mode (note 1)	Reset
		x x 1 0	standby 2 : 'CD-PAUSE' mode (note 1)	
		x x 1 1	operating mode	
Versatile pins interface	1 1 0 0	x x x 1	offtrack input at V1	
		x x x 0	no offtrack input (V1 may be read via status)	Reset
		x x 0 x	Kill-L at KILL output, Kill-R at V3 output	
		x 0 1 x	V3 = 0; single Kill output	Reset
		x 1 1 x	V3 = 1; single Kill output	
Versatile pins interface	1 1 0 1	0 0 0 0	4-line motor (using V4, V5)	
		x x 0 1	Q to W subcode at V4	
		x x 1 0	V4 = 0	
		x x 1 1	V4 = 1	Reset
		0 1 x x	de-emphasis signal at V5	
		1 0 x x	V5 = 0	
		1 1 x x	V5 = 1	Reset

Notes to Table 1

1. Standby modes = CL, DA, RAB – normal operation
   MISC, SCLK, WCLK, DATA, CL11, DOBM – 3-state
   CRIN, CROUT, CL16, CLA – normal operation
   V1, V2, V3, V4, V5 – normal operation
   MOTO1, MOTO2 – in standby 2 'CD-PAUSE' – normal operation
   MOTO1, MOTO2 – in standby 1 'CD-STOP' – held LOW in PWM mode, – 3-state in PDM mode

FUNCTIONAL DESCRIPTION (continued)

Error corrector

The error corrector carries out t = 2, e = 0 error corrections on both C1 (32 symbol) and C2 (28 symbol) frames. Four symbols are used from each frame as parity symbols. The strategy t = 2, e = 0 means that the error corrector can correct two erroneous symbols per frame and detect all erroneous frames.

The error corrector also contains a flag processor. Flags are assigned to symbols when the error corrector cannot ascertain if the symbols are definitely good. C1 generates output flags which are read (after de-interleaving) by C2, to help in the generation of C2 output flags.

The C2 output flags are used by the interpolator for concealment of uncorrectable errors. They are also output via the EBU signal (DOBM) and the MISC output with I²S for CD-ROM applications.

The flags output pin CFLG provides information on the state of all error correction and concealment flags.

Audio functions

DE-EMPHASIS AND PHASE LINEARITY

When de-emphasis is detected in the Q-channel subcode, the digital filter automatically includes a de-emphasis filter section. When de-emphasis is not required, a phase compensation filter section controls the phase linearity of the digital oversampling filter to ≤ ± 1° within the band 0 to 16 kHz.

DIGITAL OVERSAMPLING FILTER

The SAA7345 contains a 2 to 4 times oversampling filter. The filter specification of the 4x oversampling filter is given in Table 2 and shown in figure 12.

These attenuations do not include the sample and hold at the DAC output or the DAC post filter.

When using the oversampling filter, the output level is scaled –0.5 dB down, to avoid overflow on full-scale sinewave inputs (0 to 20 kHz).

Table 2 Digital filter characteristics

PASSBAND	ATTENUATION
0 to 19 kHz	≤ 0.001 dB
19 to 20 kHz	≤ 0.03 dB
STOPBAND	**ATTENUATION**
24.0 kHz	≥ 25 dB
25 to 35 kHz	≥ 40 dB
35 to 64 kHz	≥ 50 dB
64 to 68 kHz	≥ 31 dB
68 kHz	≥ 35 dB
69 to 88 kHz	≥ 40 dB

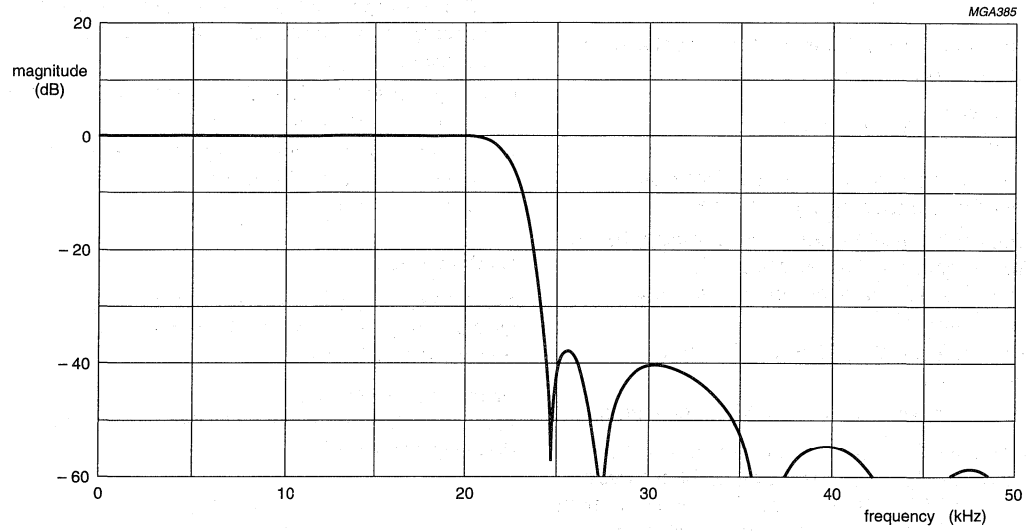


Fig.12 Digital filter characteristics.

Concealment

A 1-sample linear interpolator becomes active if a single sample is flagged as erroneous but cannot be corrected. The erroneous sample is replaced by a level midway between the preceding and following samples. Left and right channels have independent interpolators.

If more than one consecutive uncorrectable sample is found, the last good sample is held. A 1-sample linear interpolation is then performed before the next good sample (see figure 13).

Mute, Attenuation and Fade

A digital level controller is present on the SAA7345 which performs the functions of soft mute, attenuation and fade.

Mute and Attenuation

Soft mute is activated by sending the Mute command to the fade control register (address 0000, data x000). The signal will reduced to zero in up to 128 steps (depending on the current position of the fade control), taking a maximum of 3 ms.

Attenuation (–12 dB) is activated by sending the Attenuate command to the fade control register (data x01x).

Attenuation and mute are cancelled by sending the Full Scale command to the fade control register (data x001). It will take 3 ms to ramp the output from mute to the full-scale level.

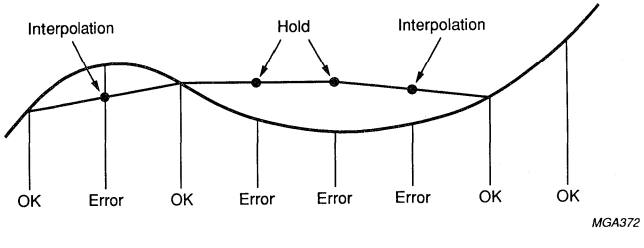


Fig.13 Concealment mechanism.

Fade

The audio output level is determined by the value of the internal fade counter.

$$Level = \frac{counter}{128} \times maximum\ level$$

- The counter is preset to 128 by the Full Scale command if no oversampling is required.
- The counter is preset to 120 (–0.5 dB scaling) by the Full Scale command if either 2 fs or 4 fs oversampling is programmed in the DAC output register (address 0011).
- The counter is preset to 32 by the Attenuate command.
- The counter is preset to 0 by the Mute command.

To control the fade counter in a continuous way, the step-up and step-down commands are available (fade control register data x101 and x100). They will increment or decrement the counter by 1 for each register write operation.

- When issuing more than 1 step-up or step-down command in sequence, the write repeat mode may be used (see figure 6).
- A pause of at least 22 µs is necessary between any two step-up or step-down commands.
- When a step-up command is given when the fade counter is already at its full-scale value, the counter will not increment.

DAC Interface

The SAA7345 is compatible with a wide range of Digital-to-Analog Converters. 10 formats are supported and are shown in Table 3.

All formats are MSB first
fs is 44.1 kHz in single-speed mode and 88.2 kHz in double-speed mode

Table 3 DAC interface formats

MODE	DAC CONTROL REGISTER DATA	SAMPLE FREQUENCY	BITS	SCLK (MHz)	FORMAT	INTERPOLATION
1	1 0 1 0	fs	16	2.1168	CD-ROM (I^2S)	no
2	1 1 1 0	fs	16	2.1168	Philips I^2S – 16 bits	yes
3	0 0 1 0	fs	16	2.1168	Sony – 16 bits	yes
4	0 1 1 0	fs	18	2.1168	Sony – 18 bits	yes
5	0 0 0 x	4fs	16	8.4672	Sony – 16 bits	yes
6	0 1 0 x	4fs	18	8.4672	Sony – 18 bits	yes
7	1 1 0 x	4 fs	18	8.4672	Philips I^2S – 18 bits	yes
8	0 0 1 1	2 fs	16	4.2336	Sony – 16 bits	yes
9	0 1 1 1	2 fs	18	4.2336	Sony – 18 bits	yes
10	1 1 1 1	2 fs	18	4.2336	Philips I^2S – 18 bits	yes

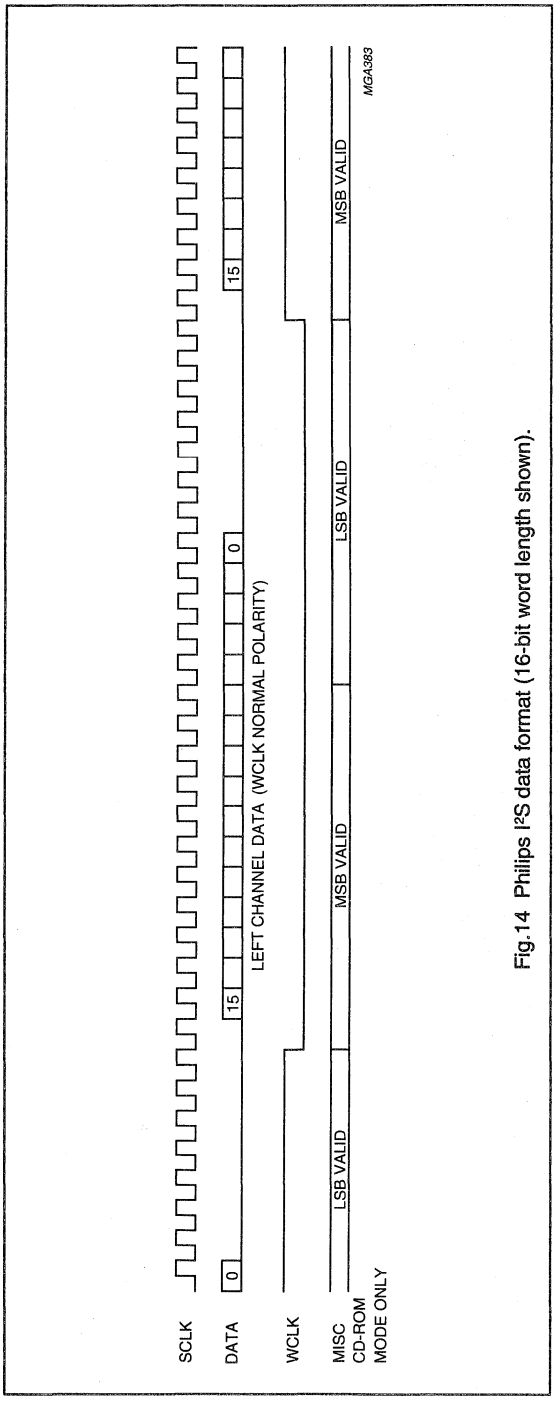


Fig.14 Philips I²S data format (16-bit word length shown).

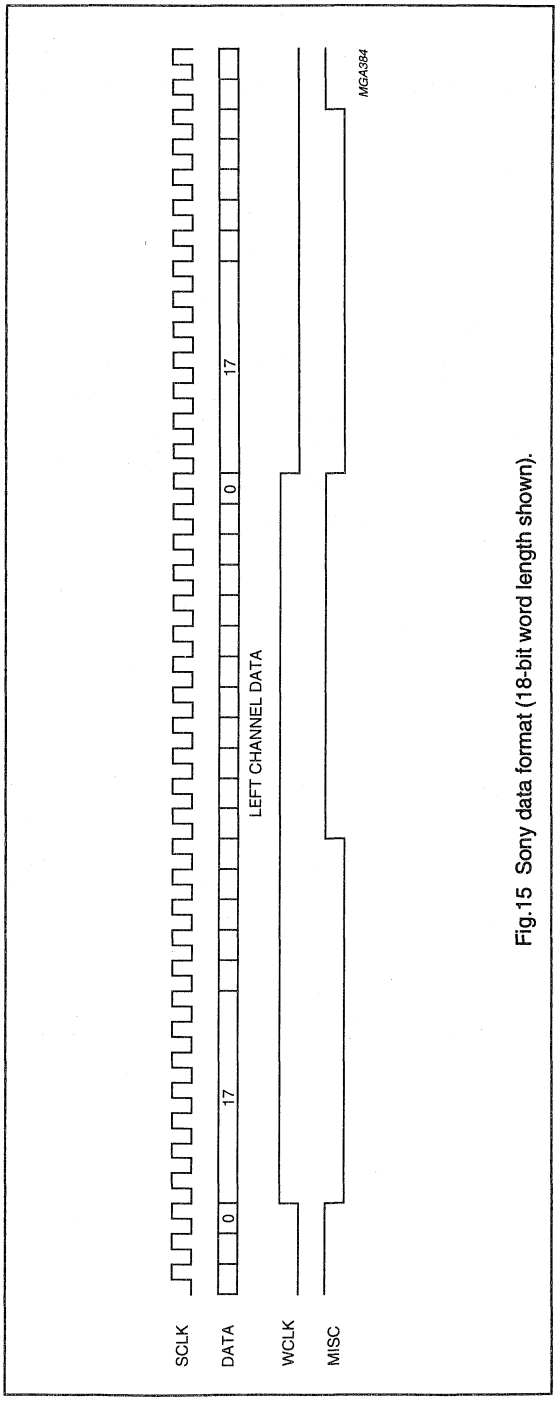


Fig.15 Sony data format (18-bit word length shown).

EBU interface

The biphase-mark digital output signal at pin DOBM is according to the format defined by the IEC958 specification.

Three different modes can be selected via the EBU output control register (address 1010).

Table 4 EBU output modes

EBU CONTROL REGISTER DATA	EBU OUTPUT AT DOBM PIN	EBU VALIDITY FLAG (bit 28)
x x 1 1	DOBM pin held LOW	
x x 0 0	data taken before concealment, mute and fade	HIGH if data is uncorrectable (concealment flag)
x x 1 0	data taken after concealment, mute, fade and digital de-emphasis	HIGH if data is uncorrectable (concealment flag)

FORMAT

The digital audio output consists of 32-bit words ("subframes") transmitted in biphase-mark code (two transitions for a logic 1 and one transition for a logic 0). Words are transmitted in blocks of 384.

Table 5 EBU word format

WORD	BITS	FUNCTION
sync	0 to 3	
auxiliary	4 to 7	not used; normally zero
error flags	4	CFLG error and interpolation flags when bit 3 of EBU control register is set to logic 1
audio sample	8 to 27	first 4 bits not used (always zero). 2's complement LSB = bit 12, MSB = bit 27
validity flag	28	valid = logic 0
user data	29	used for subcode data (Q to W)
channel status	30	control bits and category code
parity bit	31	even parity for bits 4 to 30

SYNC

The sync word is formed by violation of the biphase rule and therefore does not contain any data. Its length is equivalent to 4 data bits. The three different sync patterns indicate the following situations:

- Sync B Start of a block (384 words), word contains left sample.
- Sync M Word contains left sample (no block start).
- Sync W Word contains right sample.

AUDIO SAMPLE

Left and right samples are transmitted alternately.

VALIDITY FLAG

Audio samples are flagged (bit 28 = logic 1) if an error has been detected but was uncorrectable. This flag remains the same even if data is taken after concealment.

USER DATA

Subcode bits Q until W from the subcode section are transmitted via the user data bit. This data is asynchronous with the block rate.

CHANNEL STATUS

The channel status bit is the same for left and right words. Therefore a block of 384 words contains 192 channel status bits. The category code is always CD. The bit assignment is shown in Table 6.

KILL circuit

The KILL circuit detects digital silence by testing for an all-zero or all-ones data word in the left or right channel before the digital filter. The output is switched active-LOW when silence has been detected for at least 200 ms. Two modes are available, selected by the versatile pins register (address 1100):

1-PIN KILL MODE

Active LOW signal on KILL pin when digital silence has been detected on both LEFT and RIGHT channels for 200 ms.

2-PIN KILL MODE

Independent digital silence detection for left and right channels. The KILL pin is active-LOW when digital silence has been detected in the LEFT channel for 200 ms, and V3 is active-LOW when digital silence has been detected in the RIGHT channel for 200 ms.

When MUTE is active then the KILL outputs are forced LOW.

Spindle Motor control

The spindle motor speed is controlled by a fully integrated digital servo. Address information from the internal + 8 frame FIFO and disc speed information are used to calculate the motor control output signals.

Several output modes are supported:

1. Pulse Density, 2-line (true complement output), 1 MHz sample frequency
2. PWM output, 2-line, 22.05 kHz modulation frequency
3. PWM-output, 4-line, 22.05 kHz modulation frequency
4. CDV motor mode

The modes are selected via the motor output configuration register (address 0110).

Table 6 EBU channel status

WORD	BITS	FUNCTION
control	0 to 3	copy of CRC checked Q-channel control bits 0 to 3 bit 2 is logic 1 when copy permitted bit 3 is logic 1 when recording has pre-emphasis
reserved mode	4 to 7	always zero
category code	8 to 15	CD: bit 8 = logic 1; all other bits = logic 0
clock accuracy	28 to 29	set by EBU control register 00 = Level II 01 = Level III
remaining	16 to 27 30 to 191	always zero

Pulse Density Mode

In the Pulse Density mode the motor output pin MOTO1 is the pulse density modulated motor output signal. 50% duty cycle corresponds with the motor not actuated, higher duty cycles mean acceleration, lower mean braking.

In this mode, the MOTO2 signal is the inverse of the MOTO1 signal. Both signals change state only on the edges of a 1 MHz internal clock signal.

Possible application diagrams are shown in figure 16.

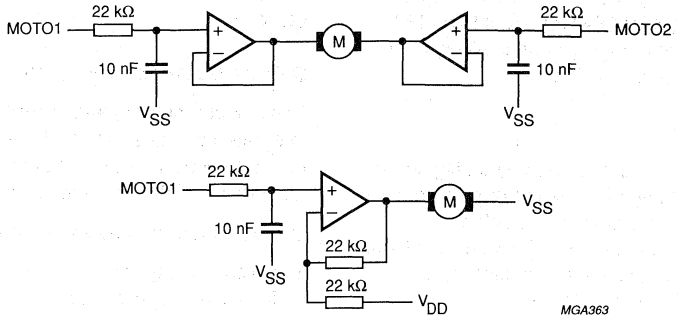


Fig.16 Motor pulse density application diagram.

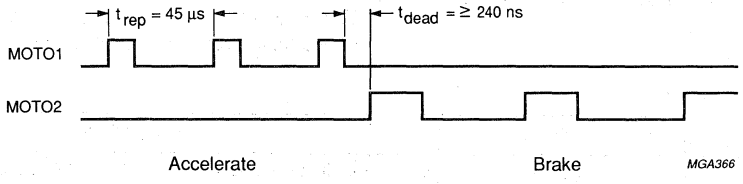


Fig.17 2-line PWM mode timing.

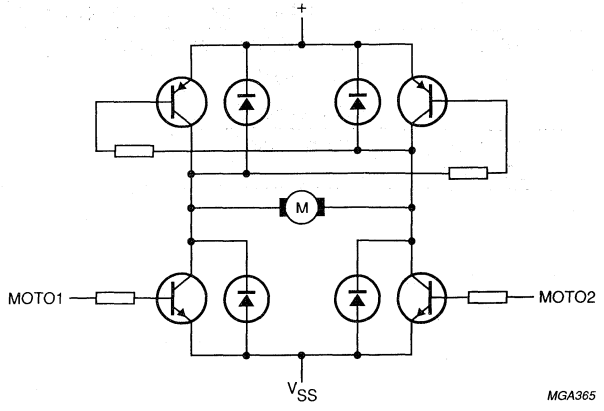


Fig.18 Motor 2-line PWM mode application diagram.

PWM MODE, 2-LINE

In the PWM mode the motor acceleration signal is put in pulse-width modulation form on the MOTO1 output and the motor braking signal is pulse-width modulated on the MOTO2 output.

Figure 17 shows the timing and figure 18 a typical application diagram.

PWM MODE, 4-LINE

Using two extra outputs from the Versatile Pins Interface, it is possible to use the SAA7345 with a 4-input motor bridge.

Figure 19 shows the timing and figure 20 a typical application diagram.

CDV MODE

In the CDV motor mode, the FIFO position will be put in pulse-width modulated form on the MOTO1 pin (carrier frequency 300 Hz) and the PLL frequency signal will be put in pulse-density modulated form on the MOTO2 pin (carrier frequency 4.23 MHz). The integrated motor servo is disabled in this mode.

Note The PWM signal on MOTO1 corresponds to a total memory space of 20 frames, therefore the nominal FIFO position (half-full) will result in a PWM output of 60%.

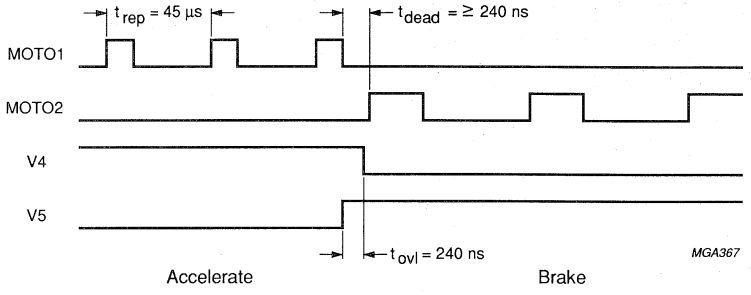


Fig.19 4-line PWM mode timing.

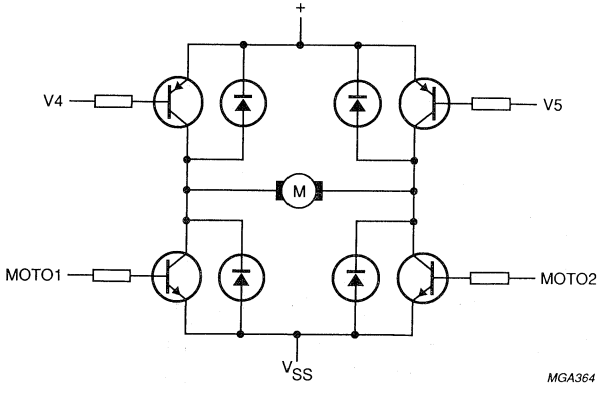


Fig.20 Motor 4-line PWM mode application diagram.

OPERATION MODES

The motor servo has the following operation modes controlled by the motor mode register (address 0001):

Start mode 1	Disc is accelerated by applying a positive voltage to the spindle motor. No decisions are involved and the PLL is reset. No disc speed information is available for the microprocessor.
Start mode 2	The disc is accelerated as in Start mode 1, however the PLL will monitor the disc speed. When the disc reaches 75% of its nominal speed, the controller will switch to Jump mode. The motor status signals are valid (register 0010).
Jump mode	Motor servo enabled but FIFO kept rest at 50%. The audio is muted but it is possible to read the subcode.
Jump mode 1	Similar to Jump mode but motor integrator is kept at zero. Used for long jumps.
Play mode	FIFO released after resetting to 50%. Audio mute released.
Stop mode 1	Disc is braked by applying a negative voltage to the motor. No decisions are involved.
Stop mode 2	The disc is braked as in Stop mode 1, but the PLL will monitor the disc speed. As soon as the disc reaches 12% of its nominal speed, the MOTSTOP status signal will go HIGH and switch the motor servo to Off mode.
Off mode	Motor not steered.

POWER LIMIT

In Start mode 1, Start mode 2, Stop mode 1 and Stop mode 2, a fixed positive or negative voltage is applied to the motor. This voltage can be programmed as a percentage of the maximum possible voltage via the motor output configuration register (address 0110) to limit current drain during start and stop. The following power limits are possible:

- 100% of maximum (no power limit)
- 75% of maximum
- 50% of maximum
- 37% of maximum

LOOP CHARACTERISTICS

The gain and cross-over frequencies of the motor control loop can be programmed via the motor gain and bandwidth registers (addresses 0100 and 0101). The possible parameter values are as follows:

Gain : 3.2, 4.0, 6.4, 8.0 12.8, 16, 26.6 or 32

Cross-over frequency, f3 : –0.5, –0.7, –1.4 or –2.8 Hz

Cross-over frequency, f4 : –0.85, –1.71 or –3.42 Hz

FIFO OVERFLOW

If FIFO overflow occurs during Play mode (e.g. as a result of motor shock), the FIFO will be automatically reset to 50% and the audio interpolator is activated to minimize the effect of data loss.

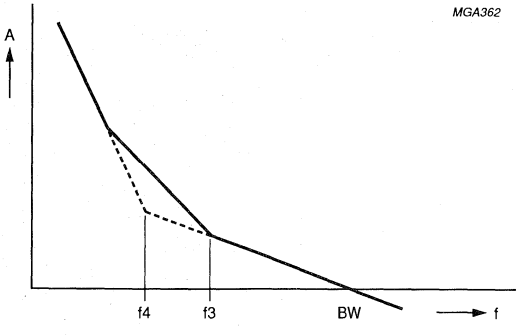


Fig.21 Motor servo mode diagram.

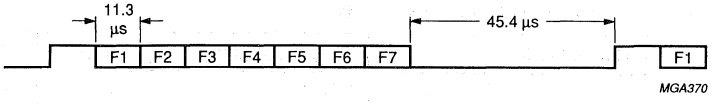


Fig.22 Flags output timing.

Flags Output (CFLG) (open drain output)

A 1-bit flag signal is available at the CFLG pin. This signal shows the status of the error corrector and interpolator and is updated every frame (7.35 kHz).

ABSOLUTE TIME SYNC

The first flag bit (F1) is the absolute time sync signal. It is the FIFO-passed subcode-sync and relates the position of the subcode-sync to the audio data (DAC output).

The flag may be used for special purposes such as synchronization of different players.

FLAGS AT EBU OUTPUT

The CFLG flags are available on bit 4 of the EBU data format when bit 3 of the EBU output control register (address 1010) is set to 1.

Double speed mode

Double speed mode is programmed via the Speed control register (address 1011). It is possible to program double speed independently of clock frequency, but performance will be reduced if a 16.934 MHz crystal is used. Double speed is guaranteed only over the supply voltage range of V_{DD} = 4.5 V to 5.5 V.

Table 7 Meaning of flag bits

F1	F2	F3	F4	F5	F6	F7	MEANING
0	x	x	x	x	x	x	no absolute time sync
1	x	x	x	x	x	x	absolute time sync
x	0	0	x	x	x	x	C1 frame contained no errors
x	0	1	x	x	x	x	C1 frame contained 1 error
x	1	0	x	x	x	x	C1 frame contained 2 errors
x	1	1	x	x	x	x	C1 frame uncorrectable
x	x	x	0	0	x	x	C2 frame contained no errors
x	x	x	0	1	x	x	C2 frame contained 1 error
x	x	x	1	0	x	x	C2 frame contained 2 errors
x	x	x	1	1	x	x	C2 frame uncorrectable
x	x	x	x	x	0	0	no interpolations
x	x	x	x	x	0	1	at least one 1-sample interpolation
x	x	x	x	x	1	0	at least one hold and no interpolations
x	x	x	x	x	1	1	at least one hold and one 1-sample interpolation

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	−0.5	+6.5	V
V_I	maximum input voltage		−0.5	V_{DD} +0.5	V
V_O	output voltage		−0.5	+6.5	V
I_O	output current (continuous)		–	±20	mA
T_{amb}	operating ambient temperature range		−40	+85	°C
T_{stg}	storage temperature range		−55	+125	°C
$V_{stat(HBM)}$	electrostatic handling	note 2	−2000	+2000	V
$V_{stat(MM)}$	electrostatic handling	note 3	−200	+200	V

Notes to the limiting values

1. All V_{DD} and V_{SS} connections must be made externally to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 µH series inductor.

CHARACTERISTICS

V_{DD} = 3.4 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	positive supply voltage		3.4	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5 V	–	30	–	mA
Analog Front End (V_{DD} = 4.5 V to 5.5 V)						
Comparator Inputs HFIN, HFREF						
f_{CLK}	clock frequency		8	–	35	MHz
V_{ptp}	HFIN input voltage level		–	1.0		V
Analog Front End (V_{DD} = 3.4 V to 5.5 V)						
Comparator Inputs HFIN, HFREF						
f_{CLK}	clock frequency		8	–	20	MHz
V_{tpt}	HFIN input voltage level		–	1.0		V
Digital Inputs CL, RAB,						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} +0.3	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
Digital inputs PORE, V1, V2						
V_{thr}	switching threshold voltage rising		–	–	$0.8V_{DD}$	V
V_{thf}	switching threshold voltage falling		$0.2V_{DD}$	–	–	V
V_{hys}	hystersis voltage		–	$0.33V_{DD}$	–	V
R_{PU}	input pull-up resistance	V_I = 0	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
Digital outputs CL16, CLA						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time (C_L = 20 pF)	note 1	–	–	15	ns
t_f	output fall time (C_L = 20 pF)	note 1	–	–	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs V4, V5						
V_{OL}	LOW level output voltage					
	V_{DD} = 4.5 V to 5.5 V	I_{OL} = +10 mA	0	–	1.0	V
	V_{DD} = 3.4 V to 5.5 V	I_{OL} = +5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage					
	V_{DD} = 4.5 V to 5.5 V	I_{OH} = −10 mA	V_{DD}−1	–	V_{DD}	V
	V_{DD} = 3.4 V to 5.5 V	I_{OH} = −5 mA	V_{DD}−1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time (C_L = 20 pF)	note 1	–	–	15	ns
t_f	output fall time (C_L = 20 pF)	note 1	–	–	15	ns
Open-drain output CFLG						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time (C_L = 20 pF)	note 1	–	–	30	ns
Open-drain outputs KILL, V3						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
I_{OL}	output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time (C_L = 20 pF)	note 1	–	–	15	ns
3-state outputs MISC, SCLK, WCLK, DATA, CL11						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = −1 mA	V_{DD}−0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time (C_L = 20 pF)	note 1	–	–	15	ns
t_f	output fall time (C_L = 20 pF)	note 1	–	–	15	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA
3-state outputs MOTO1, MOTO2, DOBM						
V_{OL}	LOW level output voltage					
	V_{DD} = 4.5 V to 5.5 V	I_{OL} = +10 mA	0	–	1.0	V
	V_{DD} = 3.4 V to 5.5 V	I_{OL} = +5 mA	0	–	1.0	V
V_{OH}	HIGH level output voltage					
	V_{DD} = 4.5 V to 5.5 V	I_{OH} = −10 mA	V_{DD}−1	–	V_{DD}	V
	V_{DD} = 3.4 V to 5.5 V	I_{OH} = −5 mA	V_{DD}−1	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time (C_L = 20 pF)	note 1	–	–	10	ns
t_f	output fall time (C_L = 20 pF)	note 1	–	–	10	ns
I_{LI}	3-state leakage current	V_I = 0 to V_{DD}	−10	–	+10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input/output DA						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD}+0.3$	V
I_{LI}	3-state leakage current	$V_I = 0$ to V_{DD}	−10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	$I_{OL} = +1$ mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	$I_{OH} = -1$ mA	$V_{DD}-0.4$	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time (C_L = 20 pF)	note 1	–	–	15	ns
t_f	output fall time (C_L = 20 pF)	note 1	–	–	15	ns
Crystal oscillator input CRIN (external clock)						
V_{IL}	LOW level input voltage		−0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	$V_{DD}+0.3$	V
C_I	input capacitance		–	–	10	pF
I_{LI}	input leakage current		−10	–	+10	µA
Crystal oscillator output CROUT (see Fig.26)						
f_{XTAL}	crystal frequency		8	16.9344	35	MHz
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I²S Timing						
Clock output SCLK (see Fig.23)						
t_{po}	output clock period					
	sample rate = fs		–	472.4	–	ns
	sample rate = 2 fs		–	236.2	–	ns
	sample rate = 4 fs		–	118.1	–	ns
t_{HC}	clock HIGH time					
	sample rate = fs		166	–	–	ns
	sample rate = 2 fs		83	–	–	ns
	sample rate = 4 fs		42	–	–	ns
t_{LC}	clock LOW time					
	sample rate = fs		166	–	–	ns
	sample rate = 2 fs		83	–	–	ns
	sample rate = 4 fs		42	–	–	ns
Outputs WCLK, DATA, MISC						
t_{ST}	set-up time					
	sample rate = fs		95	–	–	ns
	sample rate = 2 fs		48	–	–	ns
	sample rate = 4 fs		24	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs WCLK, DATA, MISC						
t_{HT}	hold time					
	sample rate = fs		95	–	–	ns
	sample rate = 2 fs		48	–	–	ns
	sample rate = 4 fs		24	–	–	ns
Microprocessor interface timing (see Figs 24 and 25)						
Inputs CL and RAB						
t_L	input LOW time					
	single speed		500	–	–	ns
	double speed		260	–	–	ns
t_H	input HIGH time					
	single speed		500	–	–	ns
	double speed		260	–	–	ns
t_r	rise time	single speed	–	–	480	ns
t_f	fall time	double speed	–	–	240	ns
Read mode						
t_{DRD}	delay time RAB to DA valid		0	–	50	ns
t_{DRZ}	delay time RAB to DA HIGH-impedance		0	–	50	ns
t_{DD}	propagation delay CL to DA					
	single speed		700	–	980	ns
	double speed		340	–	500	ns
Write mode						
t_{SD}	set-up time DA to CL	note 2				
	single speed		−700	–	–	ns
	double speed		−340	–	–	ns
t_{HD}	hold time CL to DA					
	single speed		–	–	980	ns
	double speed		–	–	500	ns
t_{SCR}	set-up time CL to RAB					
	single speed		260	–	–	ns
	double speed		140	–	–	ns
t_{DWZ}	delay time DA HIGH-impedance to RAB		50	–	–	ns

Notes to the characteristics

1. Timing reference voltage levels are 0.8 V and V_{DD}−0.8 V.
2. Negative set-up time means that data may change after clock transistion.

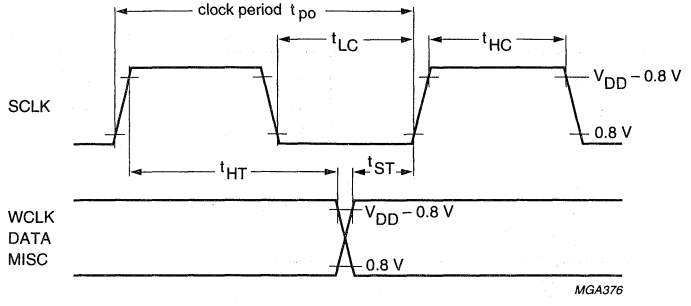


Fig.23 I²S timing.

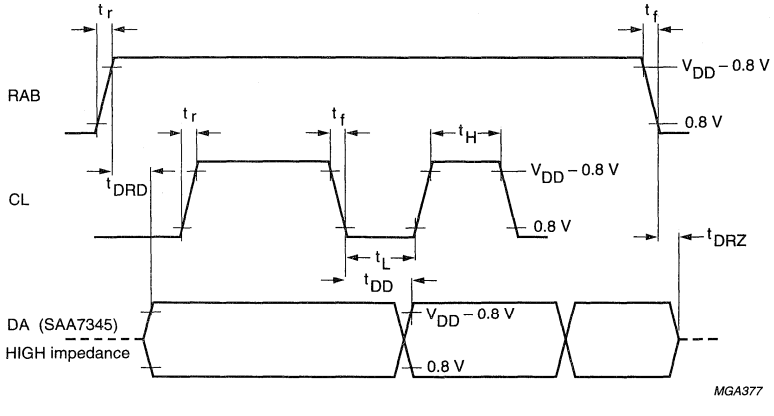


Fig.24 Microprocessor timing; READ mode.

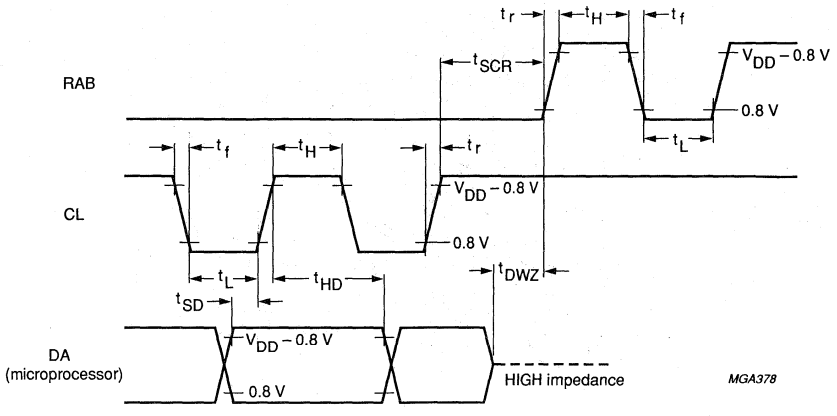


Fig.25 Microprocessor timing; WRITE mode.

APPLICATION INFORMATION

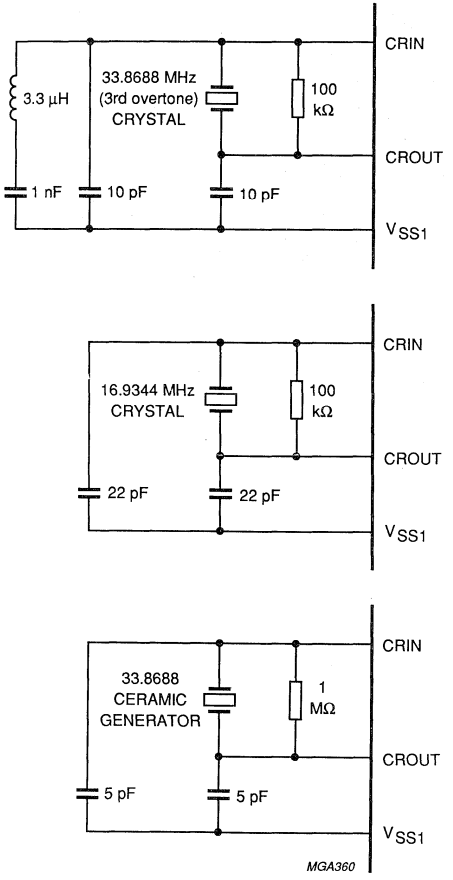


Fig.26 Application circuits for crystal oscillator.

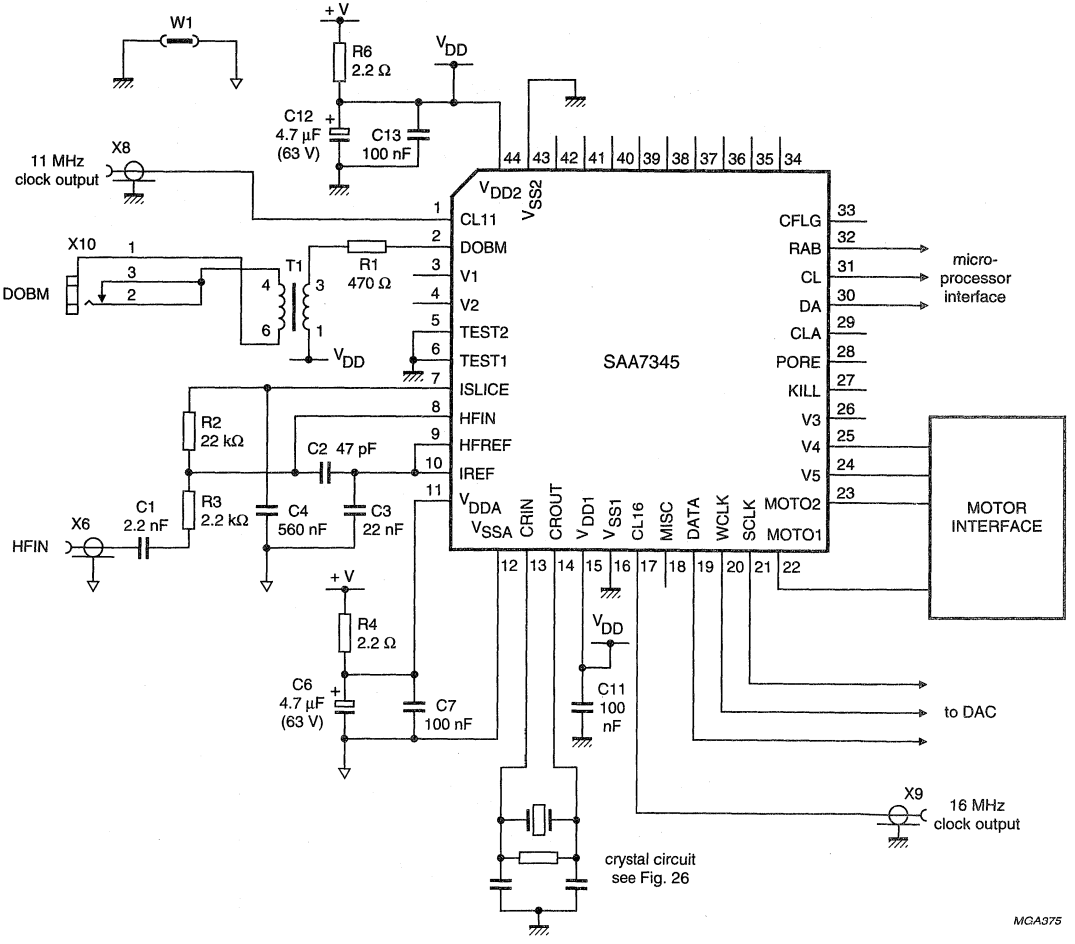
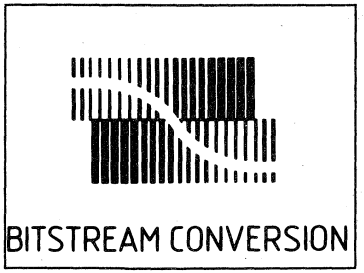


Fig.27 SAA7345 application diagram.

20-bit input bitstream conversion DAC for digital audio systems

SAA7350



FEATURES

- Up to 20-bit input
- Variety of interface formats (Japanese and I²S)
- Choice of two system clock frequencies
- Sampling frequency from 16 kHz to 53 kHz
- Third order noise shaping to increase signal-to-noise ratio
- Bitstream conversion, using switched capacitor one-bit DAC
- Differential mode output configuration
- Single power supply operation (+5 V)
- −10 to +70 °C operating temperature range
- Output interface for TDA1547

GENERAL DESCRIPTION

The SAA7350 is a CMOS digital-to-analog converter using Philips bitstream conversion technique. The device is designed for mid/high performance digital audio systems (particularly compact disc). The device also can be used with the TDA1547 device for top performance digital audio systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
f_{XTAL}	crystal frequency (256 f_s)	-	11.2896	-	MHz
f_{XTAL}	crystal frequency (384 f_s)	-	16.9344	-	MHz
DR	dynamic range	93	98	-	dB
THD	total harmonic distortion	-	−96	−93	dB
	digital silence	-	−103	−100	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7350GP	44	QPF	plastic	SOT205AG

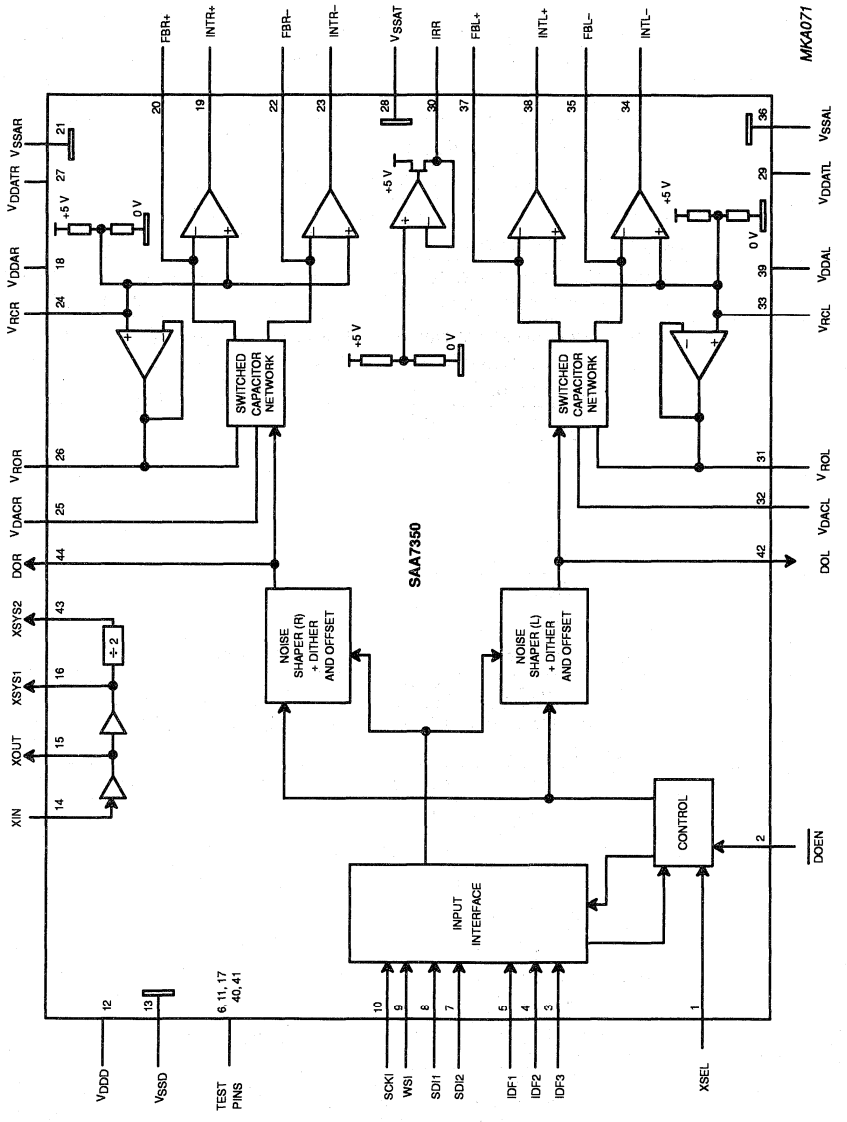


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XSEL	1	crystal frequency select; this pin is used to select the master crystal frequency as follows: XSEL HIGH = 384 f_s, XSEL LOW = 256 f_s; if unconnected the pin will default HIGH
$\overline{DOEN}$	2	one-bit digital output enable; when LOW, the one-bit code outputs are made available for TDA1547; if unconnected the pin will default HIGH
IDF3, IDF2, IDF1	3, 4, 5	input data format; these three pins determine the input format the device is to operate in (see functional description); if unconnected these pins will default HIGH (i.e. burst clock mode)
TEST4	6	test 4; this pin should be left open-circuit
SDI2	7	serial data input; used in simultaneous mode only (for the right channel signal); when not used, this pin will be internally pulled HIGH
SDI1	8	serial data input; this should be a 16, 18 or 20-bit linear 2's complement PCM signal; in simultaneous mode this pin is used for the left channel signal
WSI	9	serial input word select signal; signifies whether data word is for the left or right channel; can be either f_s, 2 f_s, 4 f_s or 8 f_s where f_s is the system sampling frequency; f_s can be between 16 kHz and 53 kHz
SCKI	10	bit clock input for the serial input interface
TEST1	11	test 1; this pin should be left open-circuit
V_{DDD}	12	+5 V power supply for the digital section
V_{SSD}	13	ground connection for the digital section
XIN	14	crystal oscillator input
XOUT	15	crystal oscillator output
XSYS1	16	buffered oscillator output
TEST5	17	test 5; in normal operation this pin should be tied LOW
V_{DDAR}	18	analog 5 V supply for right channel
INTR+	19	output from the right positive switched-capacitor integrator; input to differential operational amplifier
FBR+	20	feedback connection for the right positive switched-capacitor integrator
V_{SSAR}	21	0 V supply for right channel
FBR-	22	feedback connection for the right negative switched-capacitor integrator
INTR-	23	output from the right negative switched-capacitor integrator; input to differential operational amplifier
V_{RCR}	24	high impedance voltage reference for right channel inputs; typically $V_{DDAR}/2$
V_{DACR}	25	reference voltage supply for right channel DAC's; normally this will beconnected to V_{SS}
V_{ROR}	26	right channel voltage reference output; typically $V_{DDAR}/2$
V_{DDATR}	27	5 V supply for right channel analog timing
V_{SSAT}	28	0 V supply for left and right channel analog timing
V_{DDATL}	29	5 V supply for left channel analog timing
IRR	30	24 kΩ bias resistor connection for the reference current generator circuit

PINNING

SYMBOL	PIN	DESCRIPTION
V_{ROL}	31	left channel voltage reference output; typically $V_{DDAL}/2$
V_{DACL}	32	reference voltage supply for left channel DAC; normally this will be connected to V_{SS}
V_{RCL}	33	high impedance voltage reference for left channel inputs and for bias current generator; typically $V_{DDAL}/2$
INTL-	34	output from the left negative switched-capacitor integrator; input to differential operational-amplifier
FBL-	35	feedback connection for the left negative switched-capacitor integrator
V_{SSAL}	36	0 V supply for left channel
FBL+	37	feedback connection for the left positive switched-capacitor integrator
INTL+	38	output from the left positive switched-capacitor integrator; input to differential operational-amplifier
V_{DDAL}	39	analog 5 V supply for left channel
TEST2	40	test 2; this pin should be left open-circuit
TEST3	41	test 3; this pin should be left open-circuit
DOL	42	digital output left; left channel one-bit code for TDA1547; when disabled this pin will be driven LOW
XSYS2	43	output clock at a frequency of half the master clock frequency
DOR	44	digital output right; right channel one-bit code for TDA1547; when disabled this pin will be driven LOW

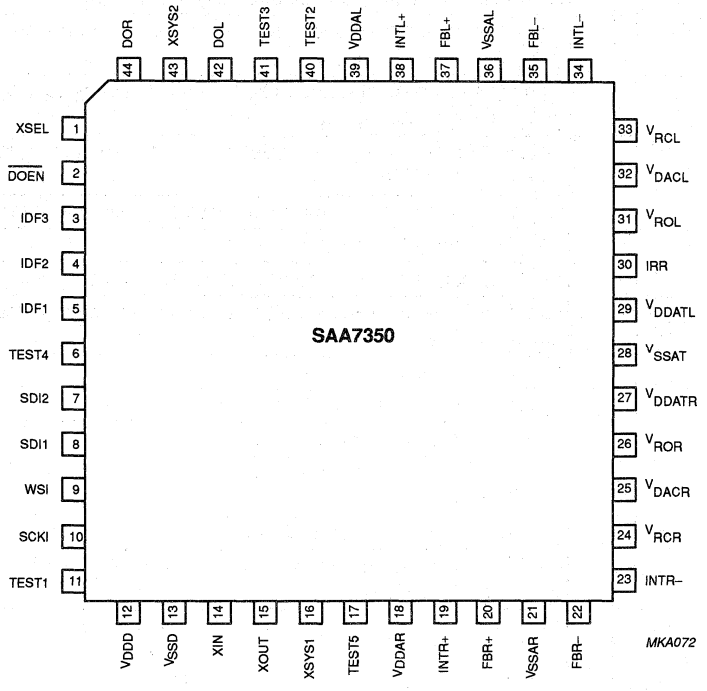


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

General

The SAA7350 bitstream conversion CMOS DAC contains a flexible interface supporting a variety of formats. This enables it to be used with a number of available digital filters with wordlengths of up to 20 bits and upsampling up to 8 f_s. The system sampling frequency (f_s) can be between 16 kHz and 53 kHz.

The analog section contains four one-bit DACs operated in differential mode to achieve high performance signal-to-noise ratio, channel separation and total harmonic distortion.

Input interface

The SAA7350 supports the following modes:

- I²S with dataword rates of f_s, 2 f_s or 4 f_s with wordlengths of up to 20 bits (see Fig. 3). A minimum of 16 bit-clock cycles per word is required.
- Sony serial format for dataword rate of f_s, 2 f_s or 4 f_s with wordlengths of 16, 18 or 20 bits (see Fig. 4). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits idling on the least significant bit (see Fig. 5). A minimum of 16 bit-clock cycles per word is required.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s and 8 f_s with wordlengths of 18 or 20 bits idling on the MSB (see Fig. 6). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits using burst clocks (see Fig. 7). A minimum of 16 bit-clock cycles is required. This mode is restricted to having the bit clock at less than or equal to half the master clock frequency supplied to the SAA7350.

The choice of these formats is given by the pins IDF1 to IDF3 as shown below.

Input data formats

IDF3	IDF2	IDF1	format
0	0	0	I²S format up to 20 bits
0	0	1	Sony serial format 16 bits
0	1	0	Sony serial format 18 bits
0	1	1	Sony serial format 20 bits
1	0	0	simultaneous format idling on LSB up to 20 bits
1	0	1	simultaneous format idling on MSB 18 bits
1	1	0	simultaneous format idling on MSB 20 bits
1	1	1	simultaneous format burst clock up to 20 bits

The transfer on the serial input has to be synchronous to the master clock.

Clock frequency

The device can run at an input clock frequency of either 384 f_s or 256 f_s (pin XSEL) outputting a system clock at the same frequency on XSYS1 and half input clock frequency on XSYS2. f_s can be between 16 kHz and 53 kHz.

Noise shaping

Third order noise shaping is implemented on the SAA7350 to give an improved signal-to-noise ratio. DC offset and out-of-band dither is added to prevent idle patterns in the audio band.

Bitstream conversion DAC

The digital-to-analogue conversion in the SAA7350 is performed using the Philips bitstream conversion technique. The input from the digital filter is oversampled to 8 f_s by means of a digital sample and hold and converted to a 1-bit pulse density modulated (PDM) signal. A switched capacitor technique is used for the bitstream conversion to convert the PDM signal to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of an integrator . As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure.

In order to increase the output signal-to-noise ratio and THD performance, internal operational-amplifiers are provided so that the device is operated in differential mode. With this technique, any common mode signals cancel thus improving the signal-to-noise ratio and total harmonic distortion.

TDA1547 interface

The SAA7350 can also be used to provide oversampling and noise shaping for the TDA1547. One-bit codes and clock outputs are supplied for inputs to the TDA1547.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage; note 1	−0.5	+6.5	V
V_I	DC input voltage	−0.5	+6.5	V
I_{IK}	DC input diode current	-	±20	mA
V_O	DC output voltage	−0.5	+6.5	V
I_O	DC output source or sink current	-	±20	mA
I_{DD} or I_{SS}	DC V_{DD} or V_{SS} current (total)	-	±0.5	A
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature range	−10	+70	°C
V_{es}	electrostatic handling; note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_{XTAL} = 384 f_s; f_s = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	supply voltage (analog)		4.5	5.0	5.5	V
I_{DDA}	supply current (analog)		-	45	70	mA
V_{DDD}	supply voltage (digital)		4.5	5.0	5.5	V
I_{DDD}	supply current (digital)		-	30	50	mA
Digital part:						
Inputs: SCKI, WSI, SDI1						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Inputs: XSEL, SD12, $\overline{\text{DOEN}}$, IDF1, IDF2, IDF3		note 3				
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
Z_I	pull-up impedance		-	50	-	kΩ
C_I	input capacitance		-	-	10	pF
Crystal oscillator input: XIN						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+1.5	V
V_{IH}	HIGH level input voltage	note 1	3.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Outputs: XSYS1						
V_{OL}	LOW level output voltage	note 1	−0.5	-	+0.4	V
V_{OH}	HIGH level output voltage	note 1	2.4	-	V_{DD} + 0.5	V
C_L	load capacitance		-	-	35	pF
Outputs: XSYS2, DOL, DOR						
V_{OL}	LOW level output voltage		-	-	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} - 0.5	-	-	V
C_L	load capacitance		-	-	20	pF
Crystal oscillator: input XIN/output XOUT						
f_{XTAL}	operating frequency XTAL	note 4	4.096	256 f_s or 384 f_s	20.35	MHz
G_m	mutual conductance	100 kHz	1.5	-	-	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	3.5	-	-	V/V
C_I	input capacitance		-	-	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator: input XIN/output XOUT						
C_{FB}	feedback capacitance		-	-	5	pF
C_O	output capacitance		-	-	10	pF
I_{LI}	input leakage current	note 2	−10	-	+10	μA
Timing						
External clock input: XIN						
f_c	input frequency		4.096	256 f_s or 384 f_s	20.35	MHz
t_r	input rise time	note 5	-	-	10	ns
t_f	input fall time	note 5	-	-	10	ns
t_{HIGH}	input HIGH time (relative to clock period)	at 1.5 V	30	-	70	%
System clock output: XSYS1		note 6				
t_r	output rise time	note 5	-	-	10	ns
t_f	output fall time	note 5	-	-	10	ns
t_{HIGH}	output HIGH time (relative to clock period)	note 7	-	50	-	%
Data outputs: DOL, DOR		see Fig.8; note 8				
t_r	data output rise time		-	10	15	ns
t_f	data output fall time		-	10	15	ns
t_{SU}	data output set-up time		0	-	-	ns
t_{HD}	data output hold time		25	-	-	ns
Data clock output: XSYS2		see Fig. 8; note 8				
t_r	clock output rise time		-	5	10	ns
t_f	clock output fall time		-	5	10	ns
t_{HIGH}	clock output HIGH time	note 9	40	-	-	ns
t_{LOW}	clock output LOW time	note 9	40	-	-	ns
Input timing		see Fig.9				
Clock input: SCKI						
f_{ci}	input clock frequency		0.256	-	20.35	MHz
msr	mark space ratio		40:60	-	60:40	
Word select input: WSI						
f_i	input frequency		14.4	-	424	kHz
Data inputs: SDI1, SDI2/word select input: WSI						
$t_{SU;DAT}$	input set-up time		-	20	-	ns
$t_{HD;DAT}$	input hold time (relative to SCKI)		0	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Reference voltage source: VRC						
V_{ref}	high-impedance reference voltage level		-	2.5	-	V
Outputs: INTL+, INTL-, INTR+, INTR-		notes 10 and 11				
$V_{AO(RMS)}$	output level at 0 dB (RMS value)	note 12	-	0.9	-	V
$V_{DIFF(RMS)}$	application output level at 0 dB (RMS value)	note 13	1.62	1.80	1.98	V
DAC performance		note 12				
DR	dynamic range		93	98	-	dB
THD + N	total harmonic distortion	at 0 dB/1 kHz	-	−96	−93	dB
	digital silence		-	−103	−100	dB
a	channel separation	1 kHz	-	100	-	dB
RR	power supply rejection ratio to V_{DD}		-	60	-	dB
	channel matching	note 14	-	-	±0.25	dB
le	linearity	0 to −100 dB	-	±1	-	dB

Notes to the characteristics

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LIMIN} and I_{LOMIN} measured at $V_I = 0$ V; I_{LIMAX} and I_{LOMAX} measured at $V_I = V_{DD}$.
3. Pins XSEL and SDI2 are internally pulled high when not connected. XSEL HIGH indicates a crystal frequency of 384 f_s.
4. f_XTAL is a multiple of the system sampling frequency f_s. f_s can be between 16 and 53 kHz.
5. Reference levels = 0.8 V and 2.0 V.
6. Output times are measured with a capacitve load of 35 pF. XSYS2 is half the master clock frequency. See Fig.10 for relative clock timings.
7. t_{HIGH} valid only when used with XTAL, with 50% input mark space ratio. XSYS1 t_{HIGH} is measured at $V_{DD}/2$.
8. Output times are measured with a capacitive load of 20 pF. XSYS2 is half the master clock frequency. Data output hold time is relative to XSYS2.
9. XSYS2 output HIGH/LOW times are for 20.35 MHz. Minimum value for 16.934 MHz is 49 ns.
10. Device measured in differential mode with external components shown in recommended application diagram (see Figs 13 and 14). It should be noted that for 1.80 mV output, feedback resistors R16a, R17a, R16b, R17b should be 31.6 kΩ. Application diagram shows preferred type range values of 30 kΩ which give 1.80 x 30/31.6 = 1.70 mV.
11. Maximum load (excluding feedback) is 10 kΩ, 100 pF to VRO (V_{ref}). Dynamic output impedance is typically 150 Ω.
12. Output level tracks linearly with sampling frequency (f_s). DAC performance quoted for 18-bit, 4 f_s input.
13. Application output level measured at output from first operational-amplifier stage in Figs 13 and 14.
14. With matched external components.

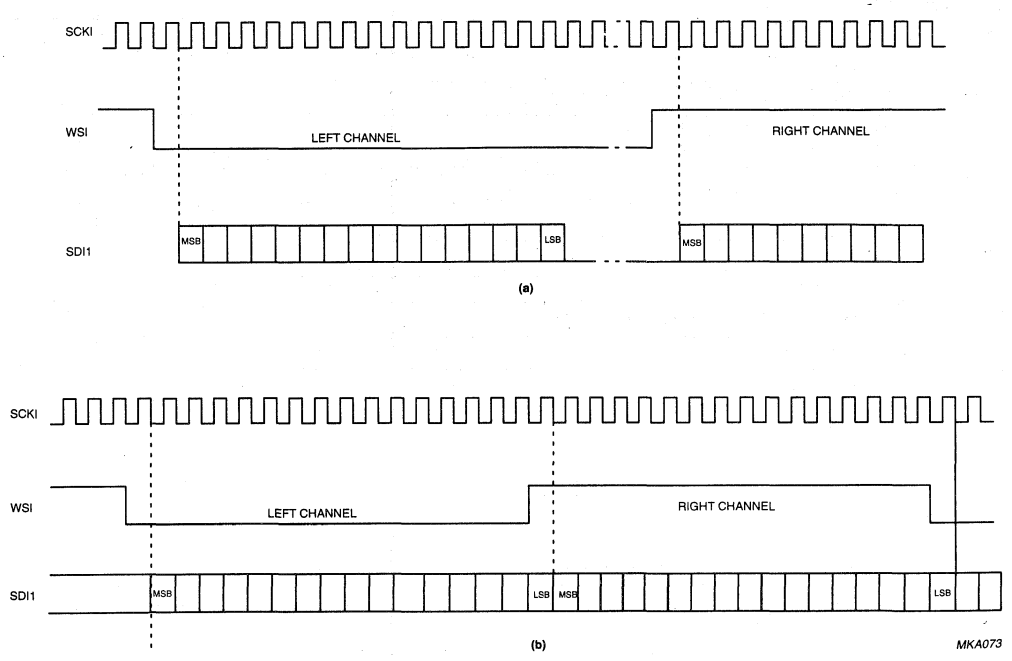


Fig.3 I²S 4 fs input formats.

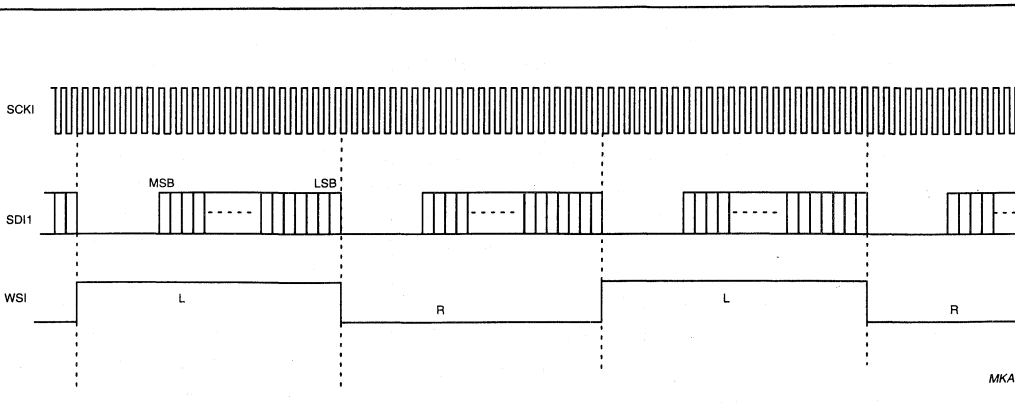


Fig.4 Sony serial input format.

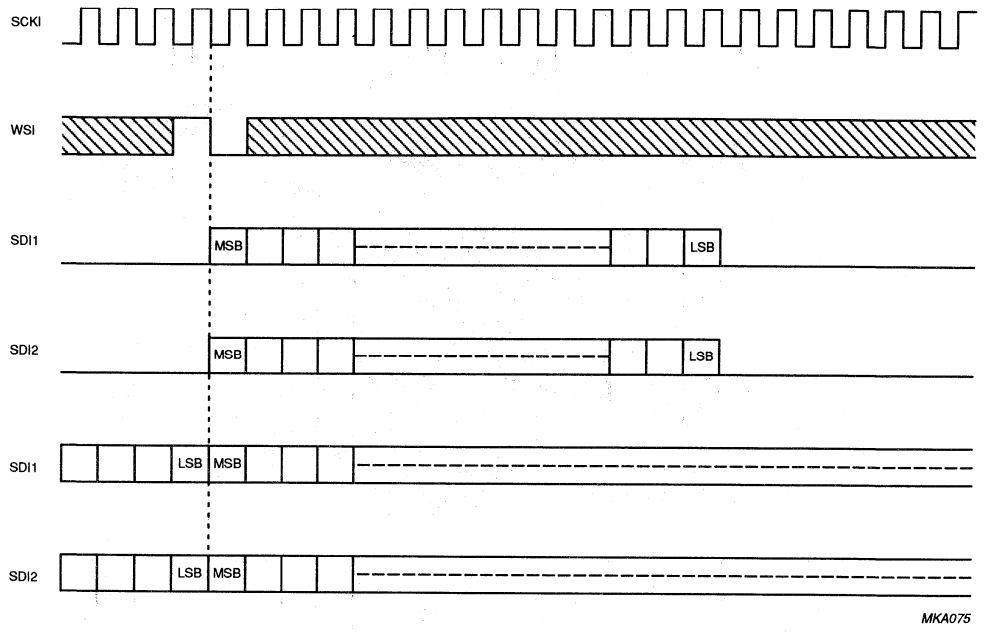


Fig.5 Simultaneous mode input format - continuous clock idling on LSB.

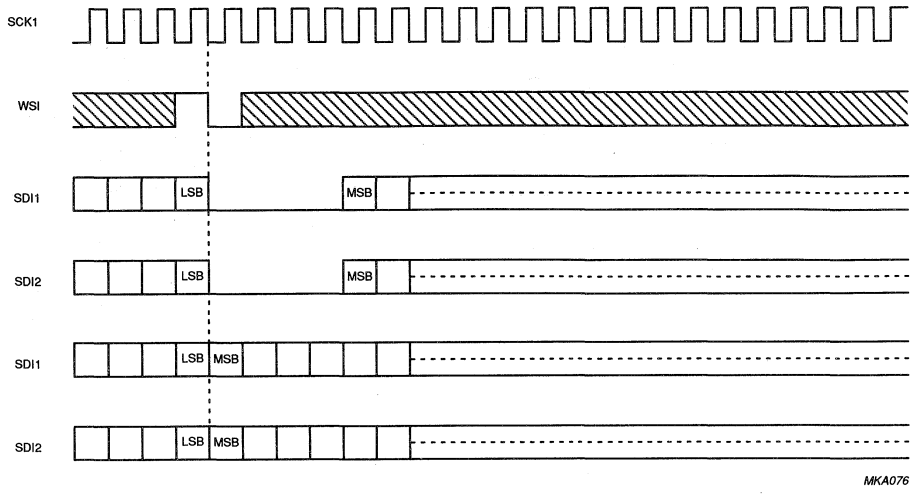


Fig.6 Simultaneous mode input format - continuous clock idling on MSB.

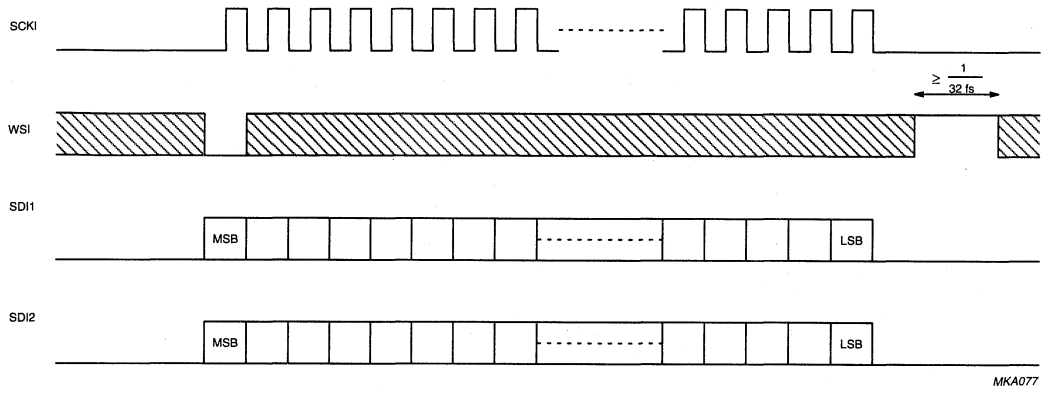


Fig.7 Simultaneous burst clock input format.

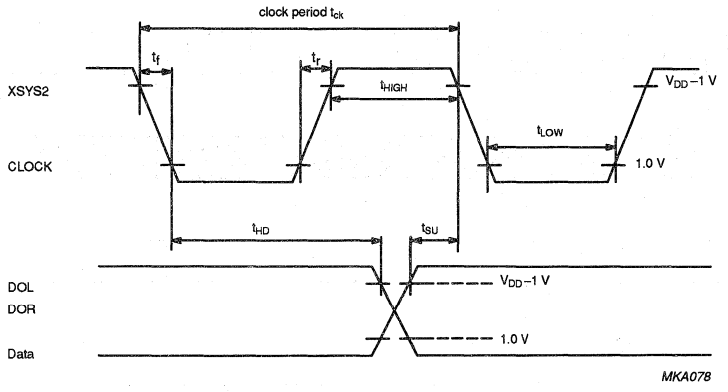


Fig.8 One bit code timing.

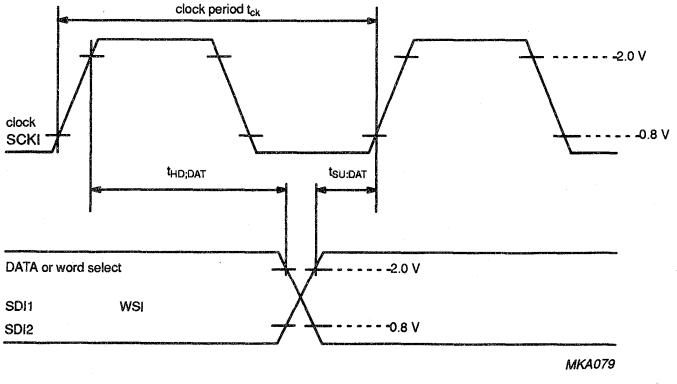


Fig.9 Input timing (valid for all input modes).

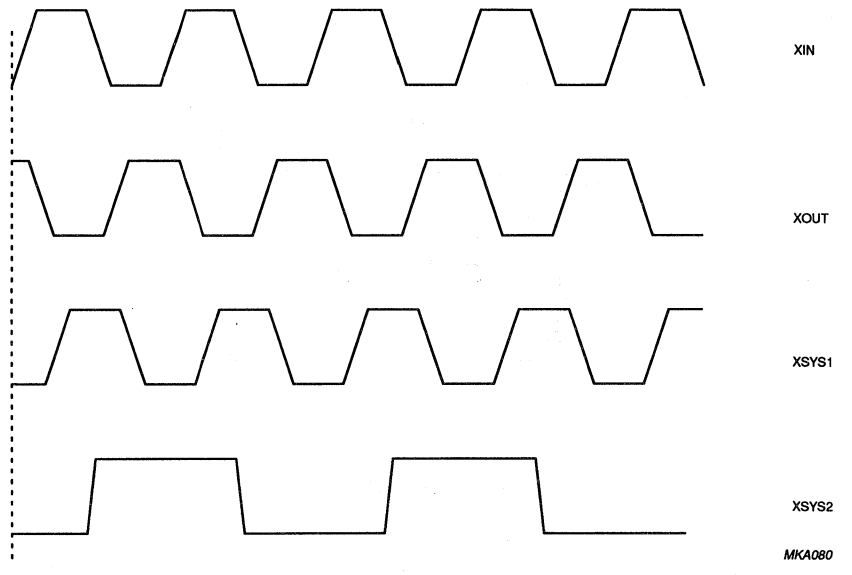


Fig.10 Relative clock timing.

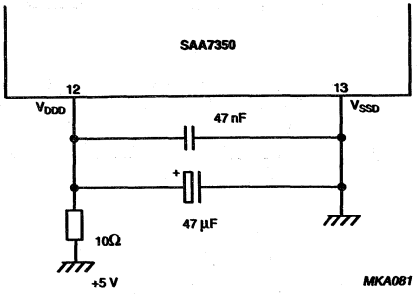


Fig.11 Digital voltage supply.

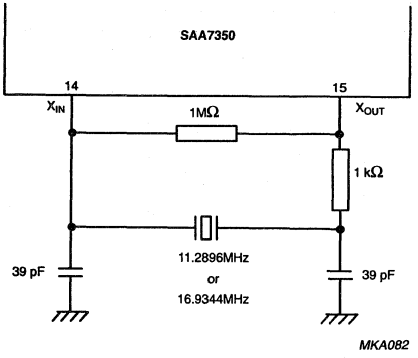


Fig.12 Crystal oscillator.

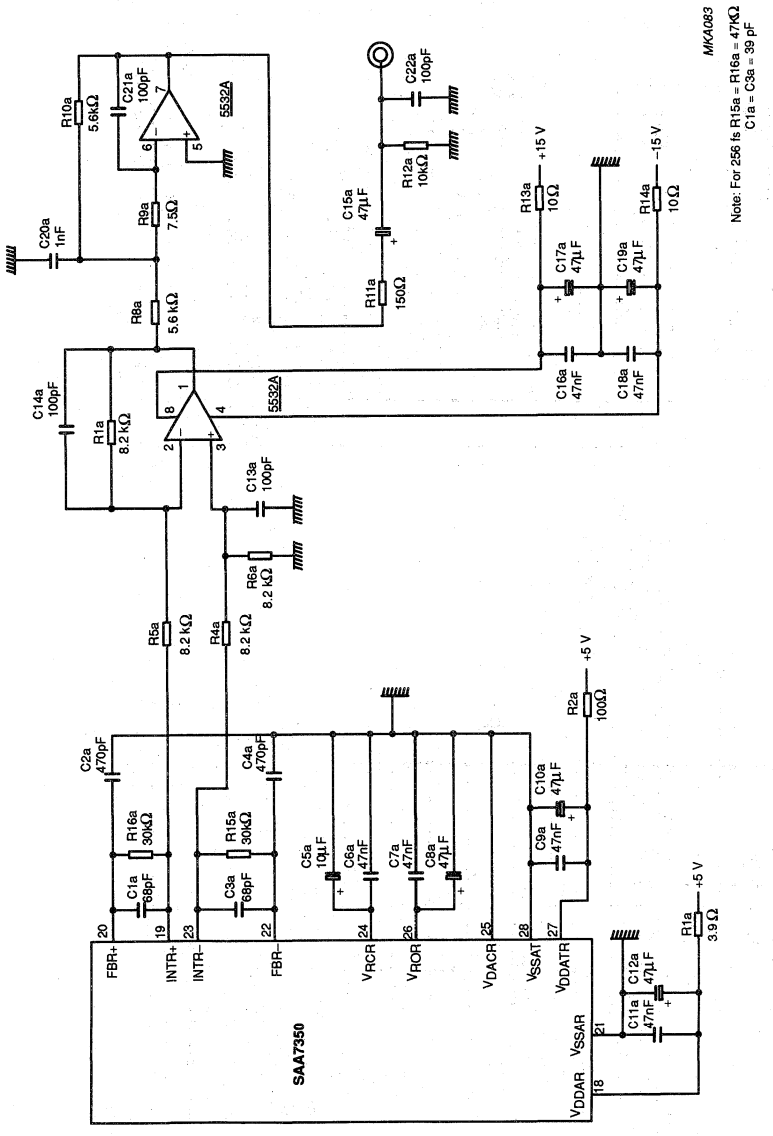


Fig.13 SAA7350 application circuit - analog section right channel (384 fs, 44.1 kHz).

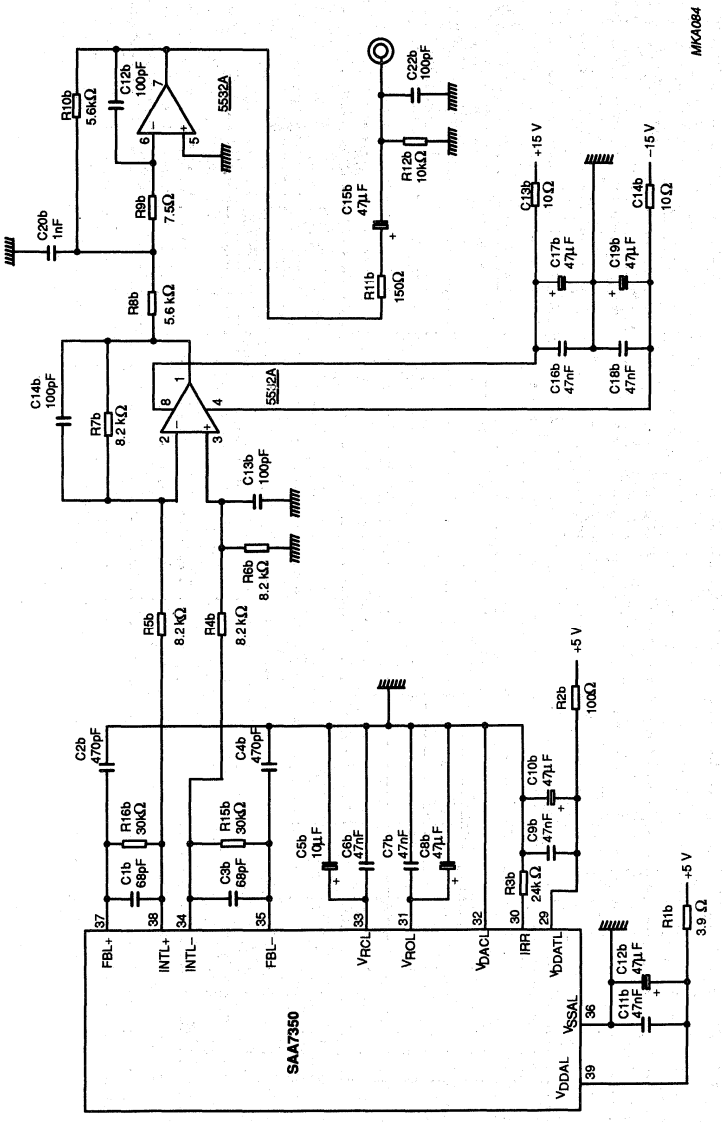
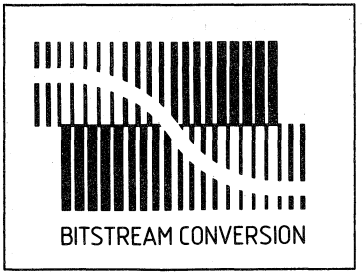


Fig.14 SAA7350 application circuit - analog section left channel (384 fs, 44.1 kHz).

20-bit input bitstream conversion DAC for digital audio systems

SAA7351



FEATURES

- Up to 20-bit input
- Variety of interface formats (Japanese and I²S)
- Choice of two system clock frequencies
- Sampling frequency from 16 kHz to 53 kHz
- Third order noise shaping to increase signal-to-noise ratio
- Bitstream conversion, using switched capacitor one-bit DAC
- Differential mode output configuration
- Single power supply operation (+5 V)
- −10 to +70 °C operating temperature range
- Signal output level constant for different sampling frequencies
- Output interface for TDA1547

GENERAL DESCRIPTION

The SAA7351 is a CMOS digital-to-analog converter using Philips bitstream conversion technique. The device is designed for mid/high performance digital audio systems. The device contains internal switched capacitor resistors in the feedback network around the DAC which enable the signal output level to remain constant for different sampling frequencies, making the SAA7351 particularly suitable for applications such as digital amplifiers. The device also can be used with the TDA1547 device for top performance digital audio systems, although without the benefit of constant output signal level for different sampling frequencies in this case.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range	4.5	5.0	5.5	V
f_{XTAL}	crystal frequency (256 f_s)	-	11.2896	-	MHz
f_{XTAL}	crystal frequency (384 f_s)	-	16.9344	-	MHz
DR	dynamic range	-	98	-	dB
THD	total harmonic distortion	-	−87	−83	dB
	digital silence	-	−100	−98	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7351GP	44	QPF	plastic	SOT205AG

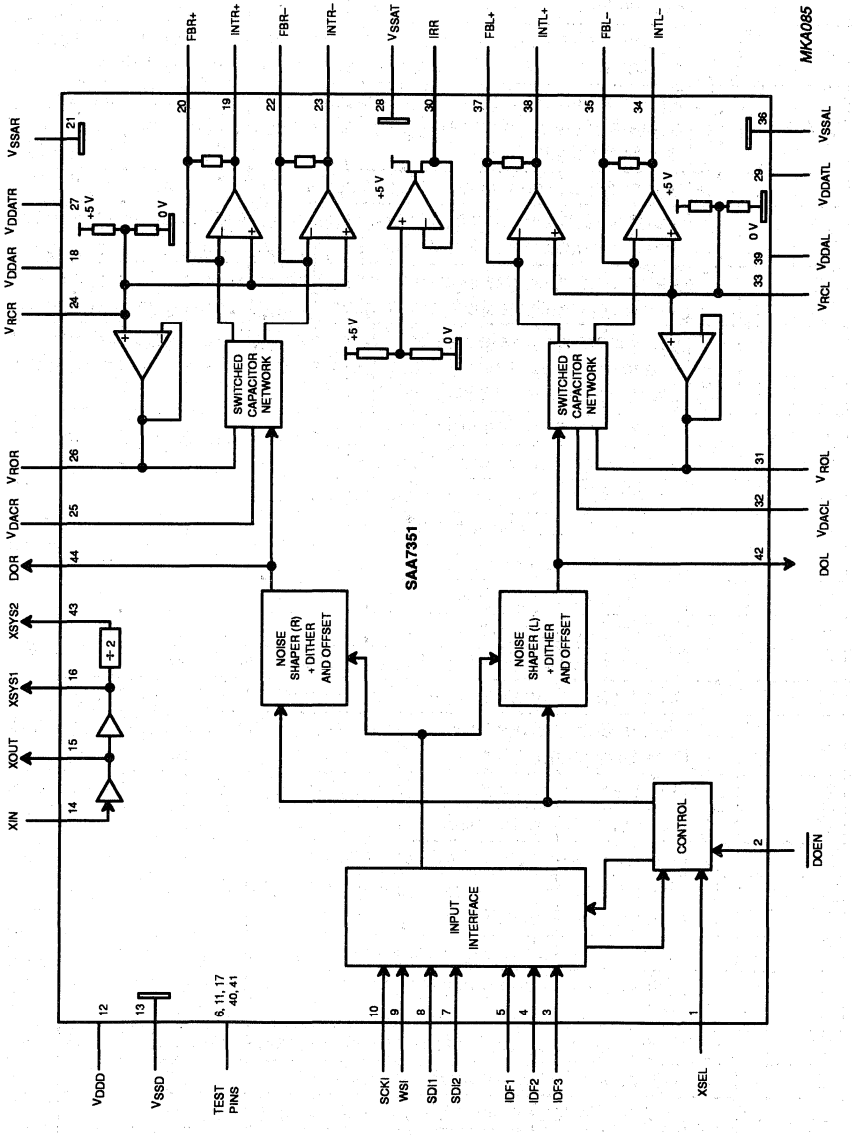


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
XSEL	1	crystal frequency select; this pin is used to select the master crystal frequency as follows: XSEL HIGH = 384 f_s, XSEL LOW = 256 f_s; if unconnected the pin will default HIGH
$\overline{DOEN}$	2	one-bit digital output enable; when LOW, the one-bit code outputs are made available for TDA1547; if unconnected the pin will default HIGH
IDF3, IDF2, IDF1	3, 4, 5	input data format; these three pins determine the input format the device is to operate in (see functional description); if unconnected these pins will default HIGH (i.e. burst clock mode)
TEST4	6	test 4; this pin should be left open-circuit
SDI2	7	serial data input; used in simultaneous mode only (for the right channel signal); when not used, this pin will be internally pulled HIGH
SDI1	8	serial data input; this should be a 16, 18 or 20-bit linear 2's complement PCM signal; in simultaneous mode this pin is used for the left channel signal
WSI	9	serial input word select signal; signifies whether data word is for the left or right channel; can be either f_s, 2 f_s, 4 f_s or 8 f_s where f_s is the system sampling frequency; f_s can be between 16 kHz and 53 kHz
SCKI	10	bit clock input for the serial input interface
TEST1	11	test 1; this pin should be left open-circuit
V_{DDD}	12	+5 V power supply for the digital section
V_{SSD}	13	ground connection for the digital section
XIN	14	crystal oscillator input
XOUT	15	crystal oscillator output
XSYS1	16	buffered oscillator output
TEST5	17	test 5; in normal operation this pin should be tied LOW
V_{DDAR}	18	analog 5 V supply for right channel
INTR+	19	output from the right positive switched-capacitor integrator; input to differential operational amplifier
FBR+	20	feedback connection for the right positive switched-capacitor integrator
V_{SSAR}	21	0 V supply for right channel
FBR-	22	feedback connection for the right negative switched-capacitor integrator
INTR-	23	output from the right negative switched-capacitor integrator; input to differential operational amplifier
V_{RCR}	24	high impedance voltage reference for right channel inputs; typically $V_{DDAR}/2$
V_{DACR}	25	reference voltage supply for right channel DAC's; normally this will beconnected to V_{SS}
V_{ROR}	26	right channel voltage reference output; typically $V_{DDAR}/2$
V_{DDATR}	27	5 V supply for right channel analog timing
V_{SSAT}	28	0 V supply for left and right channel analog timing
V_{DDATL}	29	5 V supply for left channel analog timing
IRR	30	24 kΩ bias resistor connection for the reference current generator circuit

SYMBOL	PIN	DESCRIPTION
V_{ROL}	31	left channel voltage reference output; typically $V_{DDAL}/2$
V_{DACL}	32	reference voltage supply for left channel DAC; normally this will be connected to V_{SS}
V_{RCL}	33	high impedance voltage reference for left channel inputs and for bias current generator; typically $V_{DDAL}/2$
INTL-	34	output from the left negative switched-capacitor integrator; input to differential operational-amplifier
FBL-	35	feedback connection for the left negative switched-capacitor integrator
V_{SSAL}	36	0 V supply for left channel
FBL+	37	feedback connection for the left positive switched-capacitor integrator
INTL+	38	output from the left positive switched-capacitor integrator; input to differential operational-amplifier
V_{DDAL}	39	analog 5 V supply for left channel
TEST2	40	test 2; this pin should be left open-circuit
TEST3	41	test 3; this pin should be left open-circuit
DOL	42	digital output left; left channel one-bit code for TDA1547; when disabled this pin will be driven LOW
XSYS2	43	output clock at a frequency of half the master clock frequency
DOR	44	digital output right; right channel one-bit code for TDA1547; when disabled this pin will be driven LOW

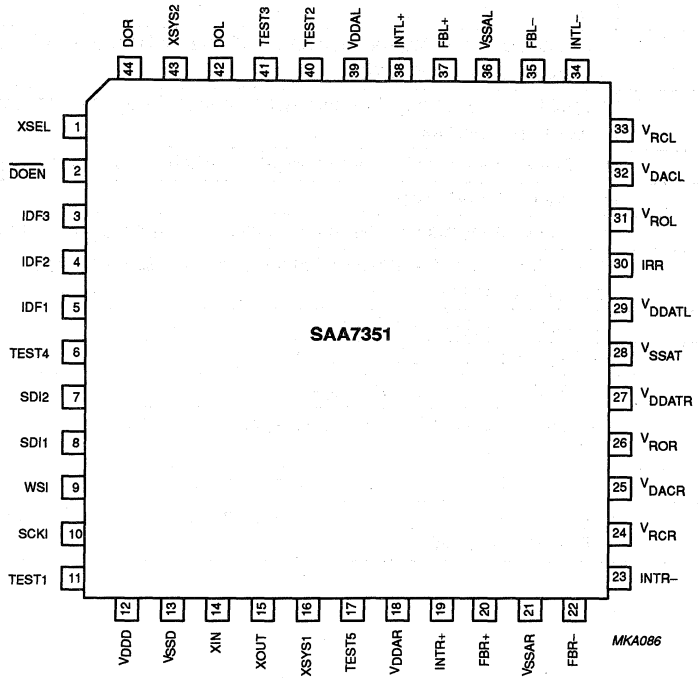


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

General

The SAA7351 bitstream conversion CMOS DAC contains a flexible interface supporting a variety of formats. This enables it to be used with a number of available digital filters with wordlengths of up to 20 bits and upsampling up to 8 f_s. The system sampling frequency (f_s) can be between 16 kHz and 53 kHz.

The analog section contains four one-bit DACs operated in differential mode to achieve high performance signal-to-noise ratio, channel separation and total harmonic distortion.

Input interface

The SAA7351 supports the following modes:

- I²S with dataword rates of f_s, 2 f_s or 4 f_s with wordlengths of up to 20 bits (see Fig. 3). A minimum of 16 bit-clock cycles per word is required.
- Sony serial format for dataword rate of f_s, 2 f_s or 4 f_s with wordlengths of 16, 18 or 20 bits (see Fig. 4). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits idling on the least significant bit (see Fig. 5). A minimum of 16 bit-clock cycles per word is required.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s and 8 f_s with wordlengths of 18 or 20 bits idling on the MSB (see Fig. 6). As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of f_s, 2 f_s, 4 f_s or 8 f_s with wordlengths of up to 20 bits using burst clocks (see Fig. 7). A minimum of 16 bit-clock cycles is required. This mode is restricted to having the bit clock at less than or equal to half the master clock frequency supplied to the SAA7351.

The choice of these formats is given by the pins IDF1 to IDF3 as shown below.

Input data formats

IDF3	IDF2	IDF1	format
0	0	0	I²S format up to 20 bits
0	0	1	Sony serial format 16 bits
0	1	0	Sony serial format 18 bits
0	1	1	Sony serial format 20 bits
1	0	0	simultaneous format idling on LSB up to 20 bits
1	0	1	simultaneous format idling on MSB 18 bits
1	1	0	simultaneous format idling on MSB 20 bits
1	1	1	simultaneous format burst clock up to 20 bits

The transfer on the serial input has to be synchronous to the master clock.

Clock frequency

The device can run at an input clock frequency of either 384 f_s or 256 f_s (pin XSEL) outputting a system clock at the same frequency on XSYS1 and half input clock frequency on XSYS2. f_s can be between 16 kHz and 53 kHz.

Noise shaping

Third order noise shaping is implemented on the SAA7351 to give an improved signal-to-noise ratio. DC offset and out-of-band dither is added to prevent idle patterns in the audio band.

Bitstream conversion DAC

The digital-to-analogue conversion in the SAA7351 is performed using the Philips bitstream conversion technique. The input from the digital filter is oversampled to 8 f_s by means of a digital sample and hold and converted to a 1-bit pulse density modulated (PDM) signal. A switched capacitor technique is used for the bitstream conversion to convert the PDM signal to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of an integrator . As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure.

In order to increase the output signal-to-noise ratio and THD performance, internal operational-amplifiers are provided so that the device is operated in differential mode. With this technique, any common mode signals cancel thus improving the signal-to-noise ratio and total harmonic distortion.

The SAA7351 also contains internal switched capacitor resistors in the feedback loop around the DAC which enables the signal output level to remain constant with different sampling frequencies.

TDA1547 interface

The SAA7351 can also be used to provide oversampling and noise shaping for the TDA1547. One-bit codes and clock outputs are supplied for inputs to the TDA1547.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage; note 1	−0.5	+6.5	V
V_I	DC input voltage	−0.5	+6.5	V
I_{IK}	DC input diode current	-	±20	mA
V_O	DC output voltage	−0.5	+6.5	V
I_O	DC output source or sink current	-	±20	mA
I_{DD} or I_{SS}	DC V_{DD} or V_{SS} current (total)	-	±0.5	A
T_{stg}	storage temperature range	−65	+150	°C
T_{amb}	operating ambient temperature range	−10	+70	°C
V_{es}	electrostatic handling; note 2	−1000	+1000	V

Notes to the limiting values

1. All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_{XTAL} = 384 f_s; f_s = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	supply voltage (analog)		4.5	5.0	5.5	V
I_{DDA}	supply current (analog)		-	45	70	mA
V_{DDD}	supply voltage (digital)		4.5	5.0	5.5	V
I_{DDD}	supply current (digital)		-	30	50	mA
Digital part:						
Inputs: SCKI, WSI, SDI1						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Inputs: XSEL, SD12, $\overline{\text{DOEN}}$, IDF1, IDF2, IDF3		note 3				
V_{IL}	LOW level input voltage	note 1	−0.5	-	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	-	V_{DD} + 0.5	V
Z_I	pull-up impedance		-	50	-	kΩ
C_I	input capacitance		-	-	10	pF
Crystal oscillator input: XIN						
V_{IL}	LOW level input voltage	note 1	−0.5	-	+1.5	V
V_{IH}	HIGH level input voltage	note 1	3.5	-	V_{DD} + 0.5	V
I_{LI}	input leakage current	note 2	−10	0	+10	µA
C_I	input capacitance		-	-	10	pF
Outputs: XSYS1						
V_{OL}	LOW level output voltage	note 1	−0.5	-	+0.4	V
V_{OH}	HIGH level output voltage	note 1	2.4	-	V_{DD} + 0.5	V
C_L	load capacitance		-	-	35	pF
Outputs: XSYS2, DOL, DOR						
V_{OL}	LOW level output voltage		-	-	0.5	V
V_{OH}	HIGH level output voltage		V_{DD} - 0.5	-	-	V
C_L	load capacitance		-	-	20	pF
Crystal oscillator: input XIN/output XOUT						
f_{XTAL}	operating frequency XTAL	note 4	4.096	256 f_s or 384 f_s	20.35	MHz
G_m	mutual conductance	100 kHz	1.5	-	-	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	3.5	-	-	V/V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal oscillator: input XIN/output XOUT						
C_I	input capacitance		-	-	10	pF
C_{FB}	feedback capacitance		-	-	5	pF
C_O	output capacitance		-	-	10	pF
I_{LI}	input leakage current	note 2	−10	-	+10	μA
Timing						
External clock input: XIN						
f_c	input frequency		4.096	256 f_s or 384 f_s	20.35	MHz
t_r	input rise time	note 5	-	-	10	ns
t_f	input fall time	note 5	-	-	10	ns
t_{HIGH}	input HIGH time (relative to clock period)	at 1.5 V	30	-	70	%
System clock output: XSYS1		note 6				
t_r	output rise time	note 5	-	-	10	ns
t_f	output fall time	note 5	-	-	10	ns
t_{HIGH}	output HIGH time (relative to clock period)	note 7	-	50	-	%
Data outputs: DOL, DOR		see Fig.8; note 8				
t_r	data output rise time		-	10	15	ns
t_f	data output fall time		-	10	15	ns
t_{SU}	data output set-up time		0	-	-	ns
t_{HD}	data output hold time		25	-	-	ns
Data clock output: XSYS2		see Fig. 8; note 8				
t_r	clock output rise time		-	5	10	ns
t_f	clock output fall time		-	5	10	ns
t_{HIGH}	clock output HIGH time	note 9	40	-	-	ns
t_{LOW}	clock output LOW time	note 9	40	-	-	ns
Input timing		see Fig.9				
Clock input: SCKI						
f_{ci}	input clock frequency		0.256	-	20.35	MHz
msr	mark space ratio		40:60	-	60:40	
Word select input: WSI						
f_i	input frequency		14.4	-	424	kHz
Data inputs: SDI1, SDI2/word select input: WSI						
$t_{SU;DAT}$	input set-up time		-	20	-	ns
$t_{HD;DAT}$	input hold time (relative to SCKI)		0	-	-	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Reference voltage source: VRC						
V_{ref}	high-impedance reference voltage level		-	2.5	-	V
Outputs: INTL+, INTL-, INTR+, INTR-		notes 10 and 11				
$V_{AO(RMS)}$	output level at 0 dB (RMS value)	note 12	-	1.9	-	V
$V_{DIFF(RMS)}$	application output level at 0 dB (RMS value)	note 13	1.9	2.0	2.1	V
DAC performance		note 12				
DR	dynamic range		-	98	-	dB
THD + N	total harmonic distortion	at 0 dB/1 kHz	-	–87	–83	dB
	digital silence		-	–100	–98	dB
a	channel separation	1 kHz	-	100	-	dB
RR	power supply rejection ratio to V_{DD}		-	60	-	dB
	channel matching	note 14	-	-	±0.25	dB
le	linearity	0 to –100 dB	-	±1	-	dB

Notes to the characteristics

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LIMIN} and I_{LOMIN} measured at V_I = 0 V; I_{LIMAX} and I_{LOMAX} measured at $V_I = V_{DD}$.
3. Pins XSEL and SDI2 are internally pulled high when not connected. XSEL HIGH indicates a crystal frequency of 384 f_s.
4. f_XTAL is a multiple of the system sampling frequency f_s. f_s can be between 16 and 53 kHz.
5. Reference levels = 0.8 V and 2.0 V.
6. Output times are measured with a capacitve load of 35 pF. XSYS2 is half the master clock frequency. See Fig.10 for relative clock timings.
7. t_{HIGH} valid only when used with XTAL, with 50% input mark space ratio. XSYS1 t_{HIGH} is measured at $V_{DD}/2$.
8. Output times are measured with a capacitive load of 20 pF. XSYS2 is half the master clock frequency. Data output hold time is relative to XSYS2.
9. XSYS2 output HIGH/LOW times are for 20.35 MHz. Minimum value for 16.934 MHz is 49 ns.
10. Device measured in differential mode with external components shown in recommended application diagram (see Figs 13 and 14).
11. Maximum load (excluding feedback) is 10 kΩ, 100 pF to VRO (V_{ref}). Dynamic output impedance is typically 150 Ω.
12. DAC performance quoted for 18-bit, 4 f_s input.
13. Application output level measured at output from first operational-amplifier stage in Figs 13 and 14.
14. With matched external components.

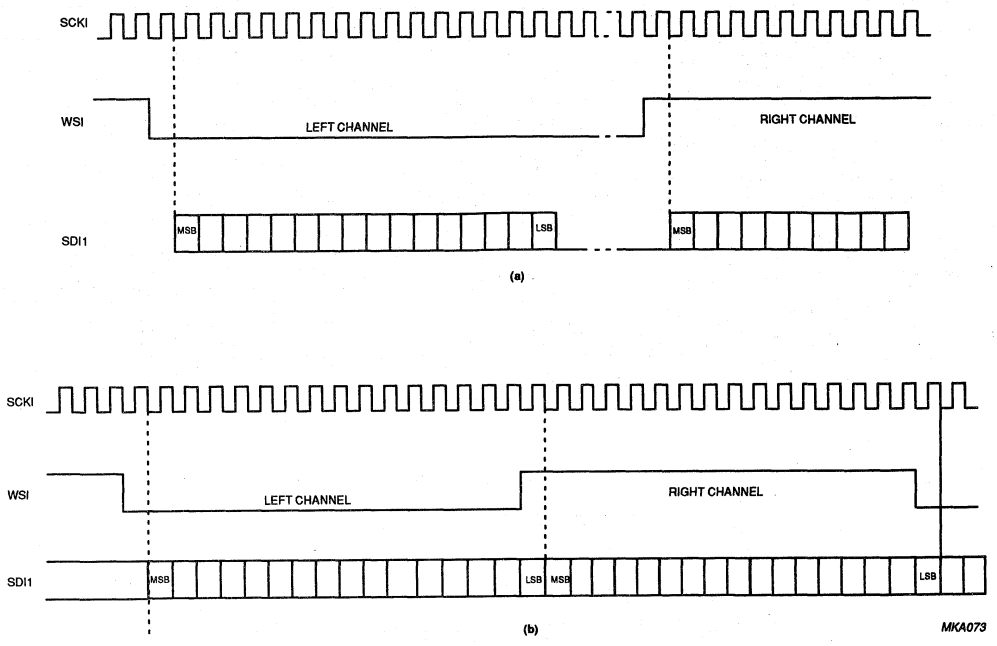


Fig.3 I²S 4 fs input formats.

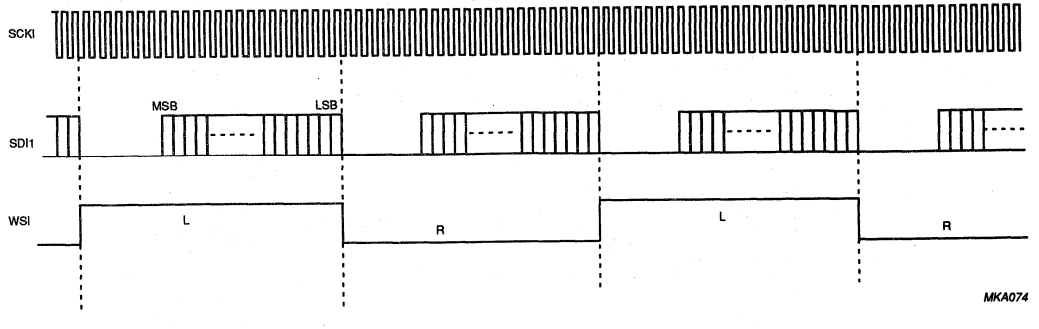


Fig.4 Sony serial input format.

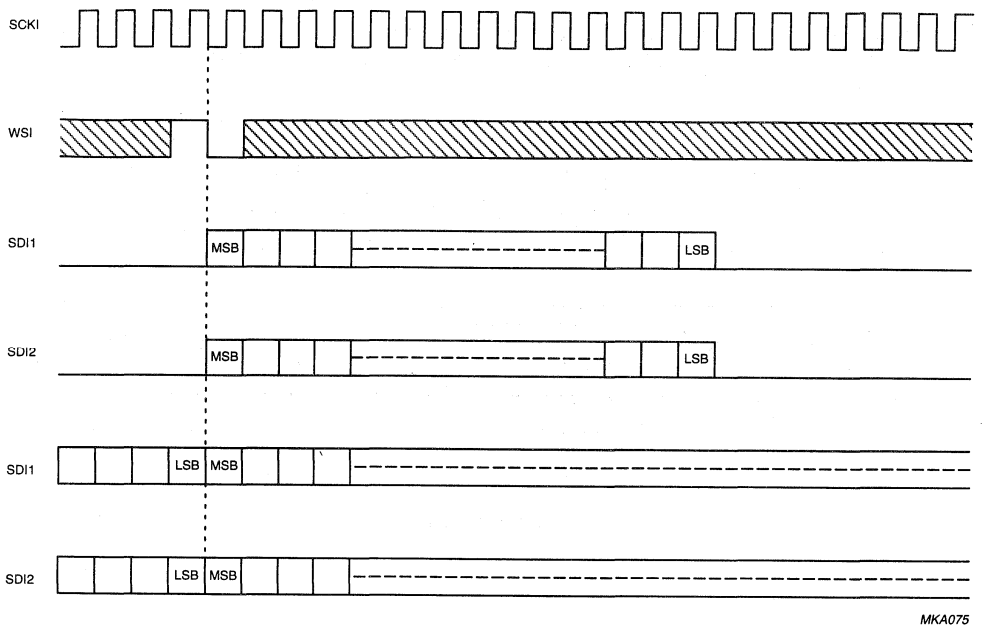


Fig.5 Simultaneous mode input format - continuous clock idling on LSB.

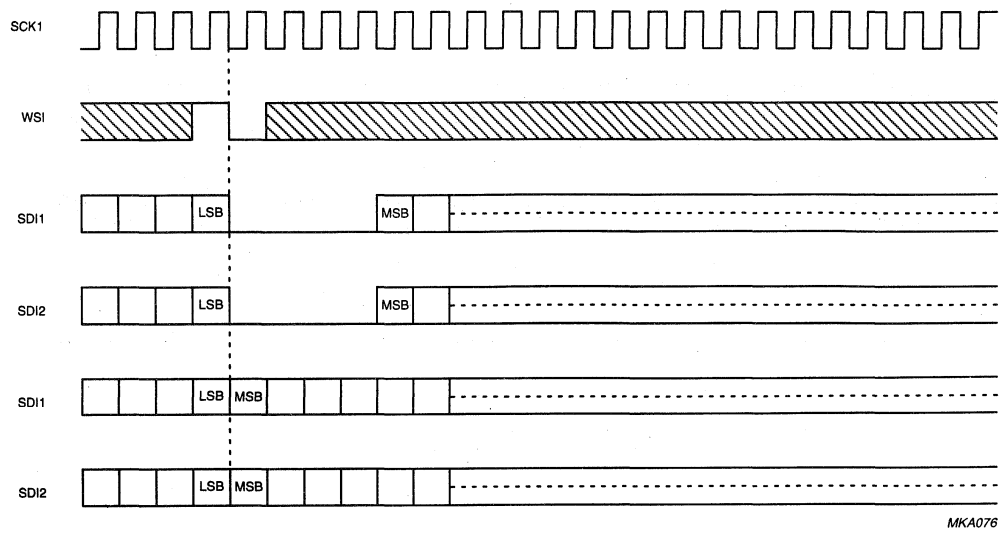


Fig.6 Simultaneous mode input format - continuous clock idling on MSB.

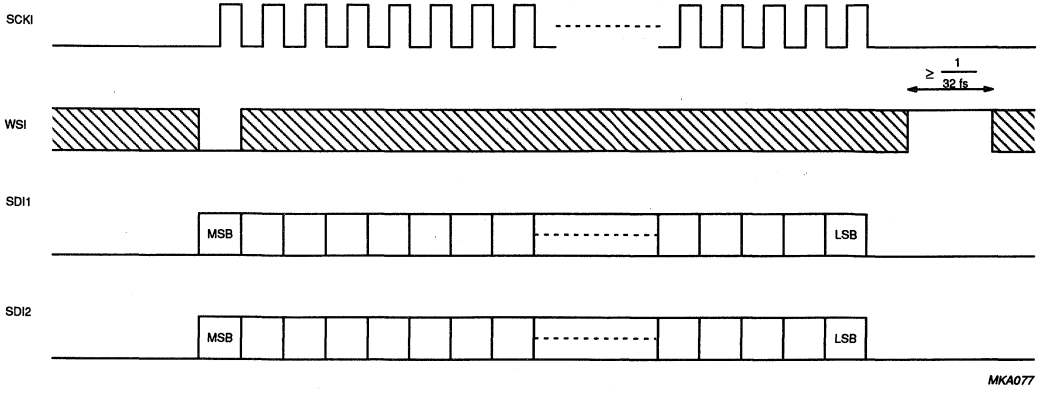


Fig.7 Simultaneous burst clock input format.

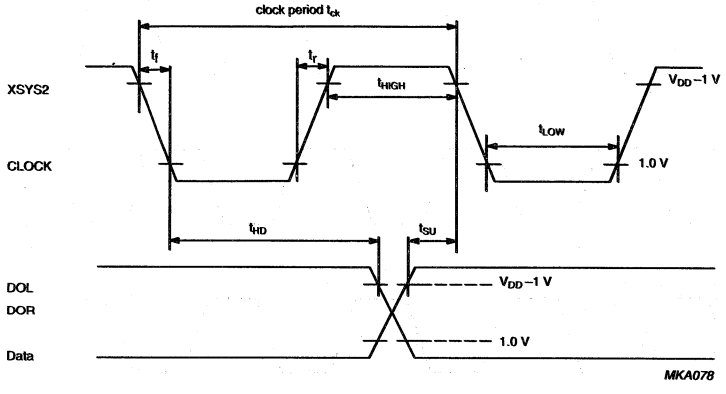


Fig.8 One bit code timing.

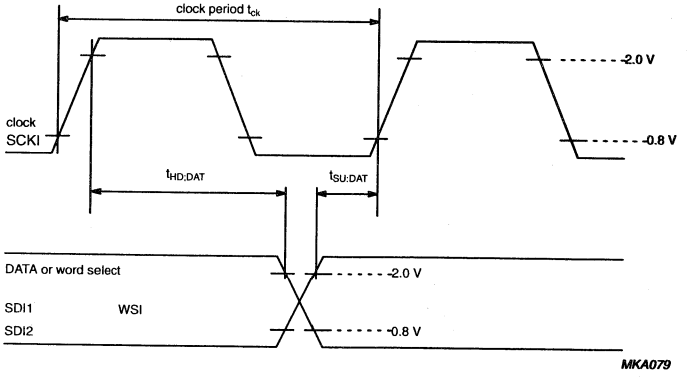


Fig.9 Input timing (valid for all input modes).

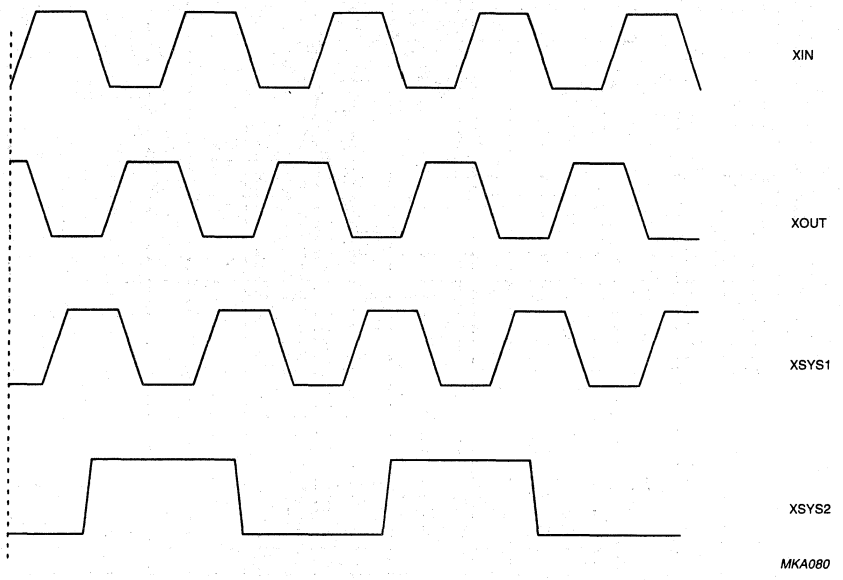


Fig.10 Relative clock timing.

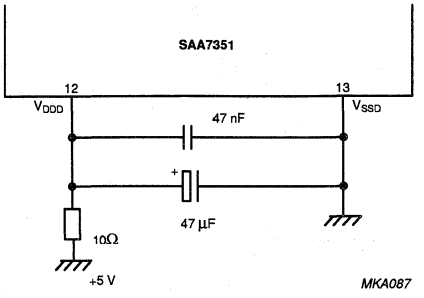


Fig.11 Digital voltage supply.

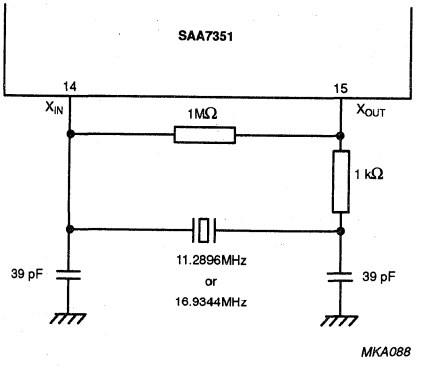


Fig.12 Crystal oscillator.

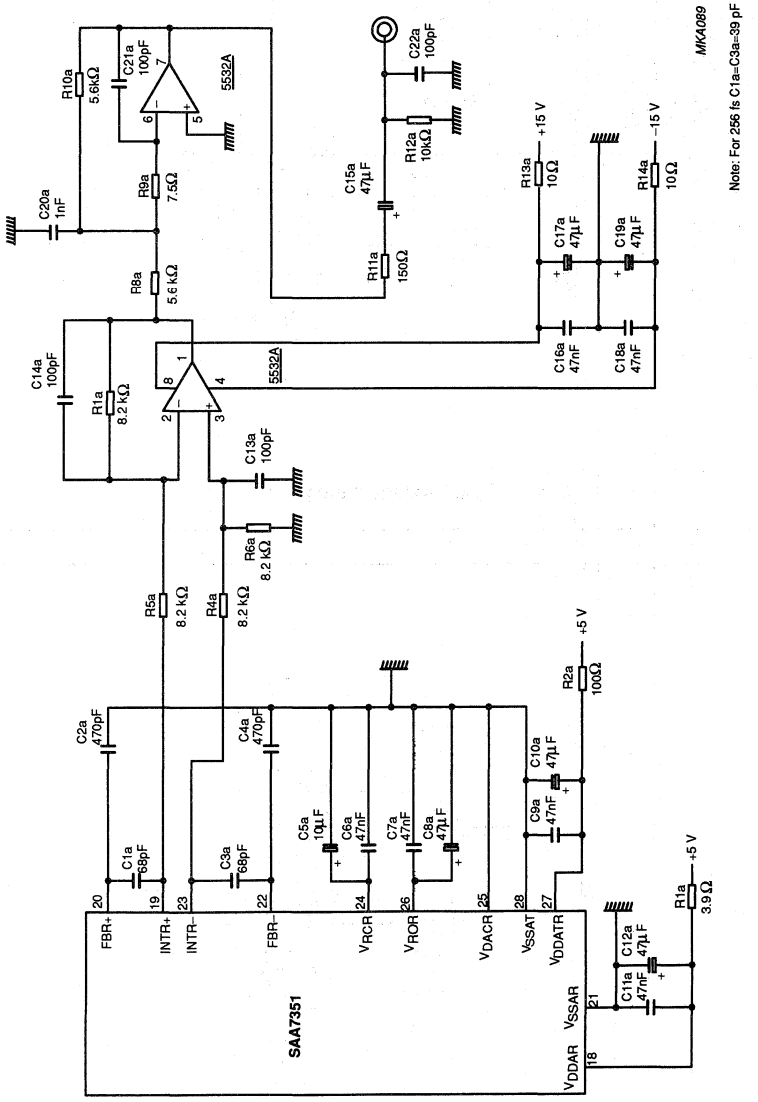


Fig.13 SAA7351 application circuit - analog section right channel (384 fs, 44.1 kHz).

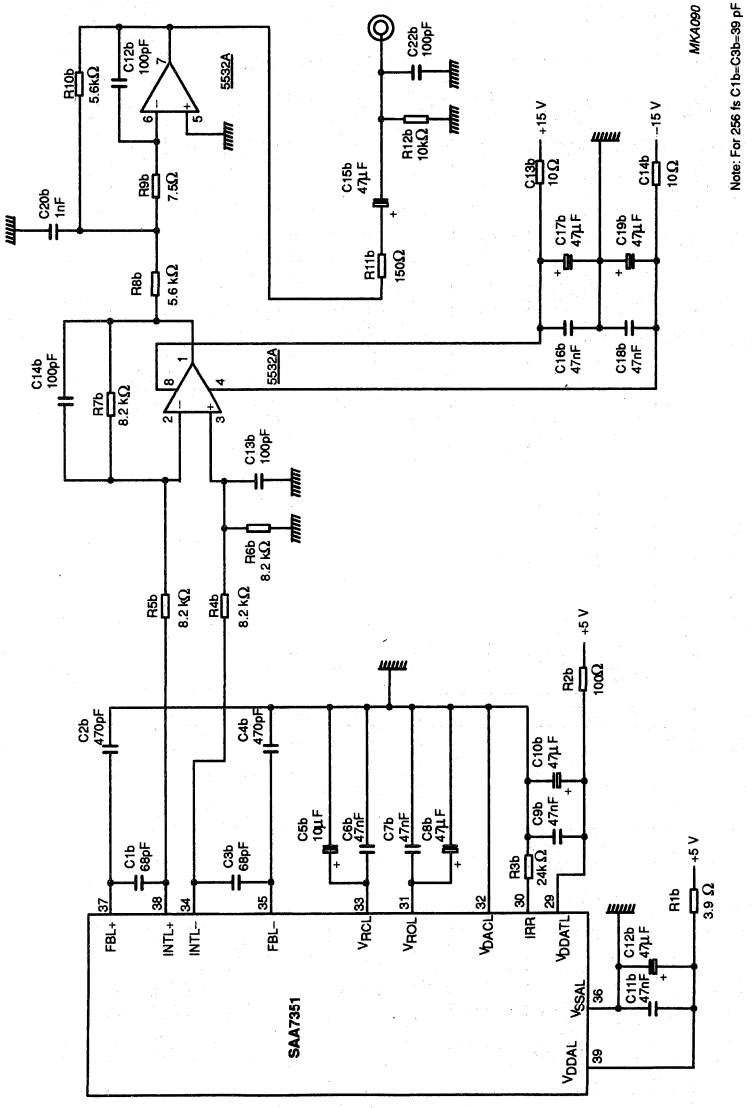
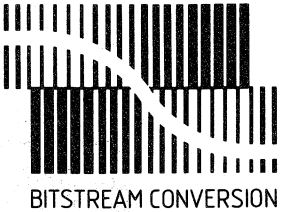


Fig.14 SAA7351 application circuit - analog section left channel (384 fs, 44.1 kHz).

Bitstream conversion ADC for digital audio systems

SAA7360

FEATURES



- Stereo input
- Single-ended input
- Uncommitted input buffer for filtering and pre-scaling
- Fully differential ADC using 3rd order Sigma-Delta modulation
- 128 times oversampling
- Four stage digital decimation filter
- Switchable high pass filter to remove DC offsets
- 16-bit or 18-bit selectable output in a multiple of formats
- Sampling rates between 18 kHz and 53 kHz supported
- Master or slave operation
- Choice of 2 crystal frequencies
- Single power supply operation (+5 V)

GENERAL DESCRIPTION

The SAA7360 is a CMOS analog-to-digital converter using Philips bitstream conversion technique. The device is designed for digital audio playback systems, such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). The device is a complementary device to the SAA7350 bitstream conversion DAC.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5.0	5.5	V
f_{XTAL}	crystal frequency				
	256 fs	–	11.2896	–	MHz
	512 fs	–	22.5792	–	MHz
THD + N	total harmonic distortion + noise	–	–90	–	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7360GP	44	QFP	plastic	SOT205A

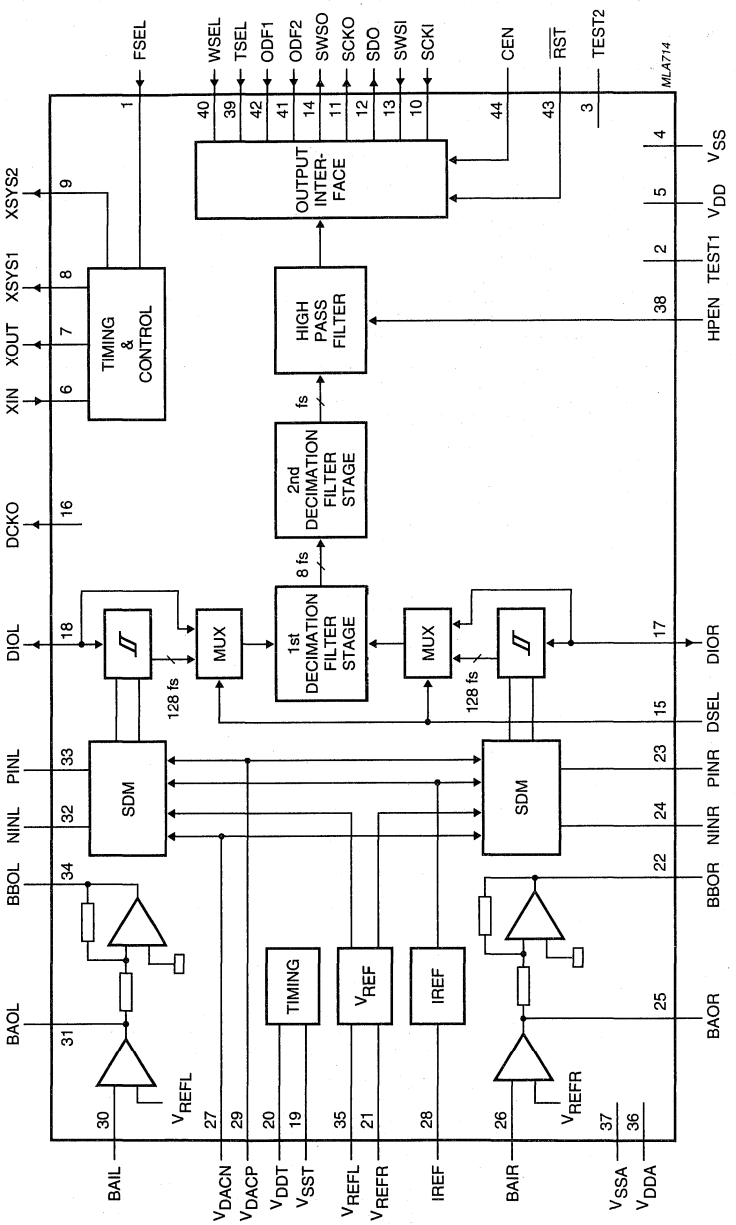


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSEL	1	crystal frequency select input. This pin is used to select the master crystal frequency as follows: FSEL HIGH = 256 fs, FSEL LOW = 512 fs. If unconnected the pin will default HIGH
TEST1	2	test input. This pin should be left open-circuit
TEST2	3	test input. This pin should be left open-circuit
V_{SS}	4	ground supply for the digital section
V_{DD}	5	+5 V supply for the digital section
XIN	6	crystal oscillator input
XOUT	7	crystal oscillator output
XSYS1	8	system clock output
XSYS2	9	output clock at a frequency half the system clock frequency
SCKI	10	serial interface clock input
SCKO	11	serial interface clock output
SDO	12	serial interface data output
SWSI	13	serial interface word select input
SWSO	14	serial interface word select output
DSEL	15	input for selecting between the internally generated 1-bit code (DSEL HIGH) or an externally generated 1-bit code (DSEL LOW). If unconnected this pin defaults HIGH
DCKO	16	1-bit code clock output
DIOR	17	1-bit code input/output (right channel)
DIOL	18	1-bit code input/output (left channel)
V_{SST}	19	ground supply for the analog timing section
V_{DDT}	20	+5 V supply for the analog timing section
V_{REFR}	21	+2.5 V reference generator for the right channel analog section
BBOR	22	output of right channel buffer operational amplifier "B"
PINR	23	positive input to right channel Sigma-Delta modulator
NINR	24	negative input to right channel Sigma-Delta modulator
BAOR	25	output of right channel buffer operational amplifier "A"
BAIR	26	input of right channel buffer operational amplifier "A"
V_{DACN}	27	negative voltage reference level input for the DACs
IREF	28	current reference output
V_{DACP}	29	positive voltage reference level input for the DACs
BAIL	30	input of left channel buffer operational amplifier "A"
BAOL	31	output of left channel buffer operational amplifier "A"
NINL	32	negative input to left channel Sigma-Delta modulator
PINL	33	positive input to left channel Sigma-Delta modulator
BBOL	34	output of left channel buffer operational amplifier "B"
V_{REFL}	35	+2.5 V reference generator for the left channel analog section
V_{DDA}	36	+5 V supply for the analog section

SYMBOL	PIN	DESCRIPTION
HPEN	38	high pass filter enable input. (HPEN HIGH = enabled). If unconnected this pin defaults HIGH
TSEL	39	input to select master (TSEL LOW) or slave (TSEL HIGH) operation of the serial interface. If unconnected this pin defaults HIGH
WSEL	40	input to indicate 16-bit (WSEL HIGH) or 18-bit (WSEL LOW) output data word length of the serial interface. If unconnected this pin defaults HIGH
ODF2, ODF1	41, 42	serial interface format inputs. These two pins determine the interface format in which the device will operate (see functional description). If unconnected these pins will default HIGH (I^2S format)
$\overline{RST}$	43	power on-reset input (active LOW) to mute the digital output during power on
CEN	44	chip enable input. This pin, when LOW, disables the operation of the device and 3-states the outputs of the serial interface bus. This enables the connection of one of more devices to the output bus. If unconnected this pin defaults HIGH

PIN CONFIGURATION

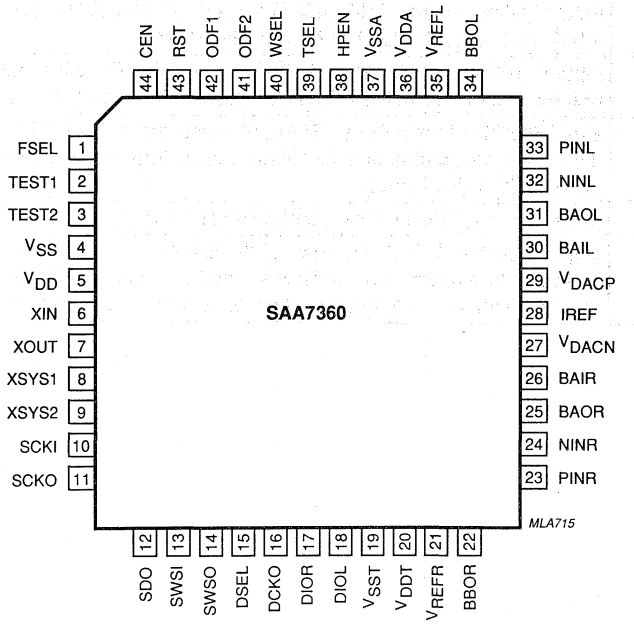


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7360 is a bitstream conversion CMOS ADC for digital audio systems. The device consists of a input buffer which can be configured by the user for pre-scaling and anti-aliasing, a third order sigma delta modulator with a performance of better than 90 dB THD + Noise, and decimation filters with anti-aliasing suppression of greater than 93 dB and in band ripple of less than 0.0002 dB. The device outputs data in a number of formats compatible with a range of manufacturers.

Clock Frequency

The SAA7360 can operate in either master or slave mode (CMOS input drive levels). The clock can be either 256 fs or 512 fs (where fs is the sampling frequency) indicated via pin FSEL. System clock outputs equal to the input frequency (XSYS1) and half the input frequency (XSYS2) are provided to drive other ICs in the system. All performance parameters track with fs which can vary between 18 kHz and 53 kHz without degradation of performance.

Input Buffer

The input buffer stage consists of an uncommitted input operational amplifier ("A") and a committed unity gain operational amplifier ("B") to perform a single-to-double ended conversion for the differential ADC. The input buffer can be configured for pre-scaling and second order anti-aliasing filtering. The scaling should be performed so as to provide a maximum of 1 V RMS at the output of the operational amplifier.

Sigma-Delta Modulator

The analog-to-digital conversion is performed by a third order Sigma-Delta modulator, which outputs a 1-bit code at 128 fs with a distortion plus noise figure of greater than 90 dB. The modulator is scaled so that a 0 dB input results in an output of –3 dB, at the 1-bit outputs.

Digital Decimation Filter

The left and right channel 1-bit codes from the ADC are decimated from 128 fs to 1 fs in four stages of filtering. The first filter stage decimates by a factor of 16 fs to 8 fs using a fourth order comb type filter. The other three filter stages consist of three cascaded half-band filters each decimating by a factor of two. The half-band filter decimating from 8 fs to 4 fs has a gain of +2 dB to compensate for the –3 dB through the analog part and allow a headroom of 1 dB to prevent clipping with DC offsets.

The overall response of the digital decimation filter is a passband from 0 fs to 0.454 fs (20 kHz at fs = 44.1 kHz fs) with ripple less than 0.0002 dB and a transition band of 0.454 fs to 0.544 fs. All frequencies between 0.544 fs and 64 fs which could result in aliasing into the baseband are attenuated by greater than –93 dB.

Table 1 Output data formats

ODF2	ODF1	MODE
0	0	test
0	1	format 1
1	0	format 2
1	1	I^2S

High Pass Filter

The operational amplifiers in the Sigma-Delta modulator can cause a small DC offset to be present in the 1-bit code passed to the digital section. This can result in the possibility of clicks when switching between devices and the recording of DC offsets which can upset offsets introduced in filters and noise shaping DACs in the playback path. A switchable high pass filter is included on the IC after the decimation filter stage to allow the user to remove these DC offsets (selectable via pin HPEN). The filter does not affect the decimation process. The filter is 1st order high pass with the following specification:

Corner frequency (-3 dB) : 1.7 Hz
Ripple: none
At 20 Hz: -0.03 dB, 5 degree phase deviation
Above 100 Hz: < 0.00002 dB, < 1 degree
Noise floor: -116 dB

Output Interface

The output interface can operate in master or slave mode selectable by pin TSEL. Master mode drives pins SWSO (word select), SCKO (bit clock) and SDO (data output). Slave mode receives the word clock on pin SWSI and the bit clock on pin SCKI. In slave mode the internal circuitry runs on the incoming bit clock and cannot therefore operate with burst clocks. Slave mode causes the pins SWSO and SCKO to be 3-stated allowing systems to connect SWSO and SCKO to pins SWSI and SCKI respectively for applications where the device has to operate in master and slave modes. The bit clock in master mode is at 32 fs for 16-bit output, and 64 fs for 18-bit output. In slave mode the bit clock is a minimum of 32 fs and a maximum of 64 fs.

Three output formats are supported, IIS and two pseudo I²S modes common in digital audio ADC systems. These formats are shown in figure 3. Selection of the three formats is given in Table 1. 16-bit or 18-bit output words can be chosen (via pin WSEL).

Reset

When pin $\overline{RST}$ is held low then the data outputs are set to zero. The $\overline{RST}$ pin operates as a Schmitt trigger, enabling a power-on-reset function by using an external RC circuit.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD(A)}$	supply voltage	note 1	−0.5	+6.5	V
V_I	DC input voltage		−0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		−0.5	V_{DD}+0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DD} or I_{SS}	total DC V_{DD} or V_{SS} current		–	±0.5	A
T_{amb}	operating ambient temperature range		−40	+85	°C
T_{stg}	storage temperature range		−65	+150	°C
V_{es}	electrostatic handling	note 2	−2000	+2000	V
V_{es}	electrostatic handling	note 3	−200	+200	V

Notes to the Limiting values

1. All V_{DD} and V_{SS} pins must be externally connected to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 1.5 μH series inductor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; f_{XTAL} = 256 fs; fs = 44.1 kHz unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	tbf	–	mA
V_{DD}	digital supply voltage		4.5	5.0	5.5	V
I_{DD}	digital supply current		–	tbf	–	mA
P_{tot}	total power consumption		–	500	–	mW
Digital part: Inputs						
FSEL, HPEN, DSEL, TSEL, WSEL, ODF2, ODF1, CEN						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DD} +0.5	V
Z_I	input impedance		–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
$\overline{RST}$						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.4V_{DD}	V
V_{IH}	HIGH level input voltage	note 1	0.6V_{DD}	–	V_{DD} +0.5	V
ΔV_I	input hystersis		0.2V_{DD}	–	–	V
C_I	input capacitance		–	–	10	pF
Crystal oscillator input XIN						
V_{IL}	LOW level input voltage		–0.5	–	+1.5	V
V_{IH}	HIGH level input voltage		3.5	–	V_{DD} +0.5	V
I_{LI}	input leakage current	note 2	–10	0	+10	µA
C_I	input capacitance		–	–	10	pF
Outputs						
SWSO, SCKO, SDO						
V_{OL}	LOW level output voltage	–400 µA; note 1	–	–	+0.4	V
V_{OH}	HIGH level output voltage	20 µA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	50	pF
I_{LI}	leakage current in 3-state	note 2	–10	0	+10	µA
DCKO, XSYS, XSYS2						
V_{OL}	LOW level output voltage	–400 µA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	20 µA; note 1	2.4	–	–	V
C_L	load capacitance					
	DCKO		–	–	50	pF
	XSYS1, XYS2		–	–	35	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/Outputs						
DIOR, DIOL						
V_{IL}	LOW level input voltage	note 1	−0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DD} +0.5	V
Z_I	input impedance		–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	−400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	20 μA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	50	pF
Crystal oscillator						
INPUT XIN; OUTPUT XOUT						
f_{XTAL}	crystal operating frequency	note 3	4.608	256 fs or 512 fs	27.136	MHz
G_m	mutual conductance	100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	3.5	–	–	V/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_O	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 2	−10	–	+10	μA
Timing						
EXTERNAL CLOCK INPUT XIN						
f_c	input frequency	note 3	4.608	256 fs or 512 fs	27.136	MHz
t_r	input rise time	note 4	–	–	10	ns
t_f	input fall time	note 4	–	–	10	ns
msr	mark-space ratio					
	in slave mode	256 fs	45	–	55	%
	in slave mode	512 fs	40	–	60	%
System clock output						
XSYS1, XSYS2 (NOTE 5)						
t_r	output rise time	note 4	–	–	15	ns
t_f	output fall time	note 4	–	–	15	ns
t_{HIGH}	output HIGH time (relative to clock period)	note 6	40	50	60	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
1-bit code outputs (see Fig.4) 1-bit code inputs (see Fig.5)						
CLOCK: DCKO						
t_{cor}	clock output rise time	note 7	–	5	10	ns
t_{cof}	clock output fall time	note 7	–	5	10	ns
t_{coh}	clock output HIGH time		45	–	–	ns
t_{col}	clock output LOW time		45	–	–	ns
DATA: DIOL, DIOR						
t_{dor}	data output rise time	note 7	–	10	15	ns
t_{dof}	clock output fall time	note 7	–	10	15	ns
t_{dod}	data output delay time (relative to DCKO)	note 7	–30	–	30	ns
t_{dir}	data input rise time		–	tbf	–	ns
t_{dif}	data input fall time		–	tbf	–	ns
t_{dis}	data input set-up time (relative to DCKO)		30	–	–	ns
t_{dih}	data input hold time (relative to DCKO)		30	–	–	ns
Serial data outputs (see Fig.6)						
CLOCK: SCKO						
t_r	clock output rise time	note 8	–	–	30	ns
t_f	clock output fall time	note 8	–	–	30	ns
WORD SELECT: SWSO						
t_r	word select output rise time	note 8	–	–	30	ns
t_f	word select output fall time	note 8	–	–	30	ns
t_{SR}	word select output set-up time	note 9	100	–	–	ns
t_{HR}	word select output hold time	note 9	100	–	–	ns
CLOCK: SCKI (NOTE 10)						
t_r	clock input rise time		–	–	100	ns
t_f	clock input fall time		–	–	100	ns
t_{HC}	clock input HIGH time		50	–	–	ns
t_{LC}	clock input LOW time		50	–	–	ns
WORD SELECT: SWSI (NOTE 10)						
t_r	word select input rise time		–	–	100	ns
t_f	word select input fall time		–	–	100	ns
t_{SR}	word select input set-up time	note 11	100	–	–	ns
t_{HR}	word select input hold time	note 11	100	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA: SDO						
t_r	data output rise time	note 8	–	–	30	ns
t_f	data output fall time	note 8	–	–	30	ns
t_{SR}	data output set-up time	notes 9 and 11	100	–	–	ns
t_{HR}	data output hold time	notes 9 and 11	100	–	–	ns
Analog part						
VOLTAGE REFERENCE						
VREFL, VREFR						
V_I	input voltage		–5%	$V_{DD}/2$	5%	V
Current Reference						
IREF (NOTE 12)						
I_O	output current		–	V_{DD}/ (2 x 15 kΩ)	–	A
DAC Reference						
INPUT: VDACN						
V_I	input voltage		–	V_{SS}	–	V
INPUT: VDACP						
V_I	input voltage		–	V_{DD}	–	V
Input Buffer						
INPUTS: BAIL, BAIR OUTPUTS: BAOL, BAOR, BBOL, BBOR (NOTE 13)						
G_{ol}	open loop gain		–	tbf	–	dB
G_f	unity-gain frequency	no load	–	tbf	–	MHz
ϕ	phase margin	no load	–	tbf	–	deg
Sigma-Delta Modulator						
INPUTS: PINR, NINR, PINL, NINL						
$V_{I(RMS)}$	input voltage (sinusoidal)		–	1	–	V
ADC performance (note 14)						
THD + N	total harmonic distortion	at –1 dB digital output	–	–	–90	dB
α	channel separation		–	tbf	–	dB

Notes to the characteristics

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LI} minimum and I_{LO} minimum measured at $V_I = 0$ V; I_{LI} maximum and I_{LO} maximum measured at $V_I = V_{DD}$.
3. f_{XTAL} is a multiple of the system sampling frequency fs which can vary between 18 kHz and 53 kHz.
4. Reference levels = 0.8 V and 2.0 V.
5. Output times are measured with a capacitve load of 35 pF. XSYS2 is half the master clock frequency.

Notes to the characteristics

6. t_{HIGH} valid only when used with XTAL, with 50% input mark space ratio. XSYS1 t_{HIGH} is measured at $V_{DD}/2$.
7. Output times are measured with a capacitive load of 20 pF.
8. Output times are measured with a capacitive load of 50 pF.
9. Relative to SCKO in master mode.
10. In slave mode the number of SCKI clocks in each channel should be less than 60 and the same in both. The polarity of SWSI indicates left/right channel.
11. Relative to SCKI in slave mode.
12. IREF connected to 0 V via a 15 kΩ resistor.
13. BBOL, BBOR are the inverted outputs of BAOL, BAOR respectively.
14. Device measured in with external components shown in recommended application diagram Fig.7.

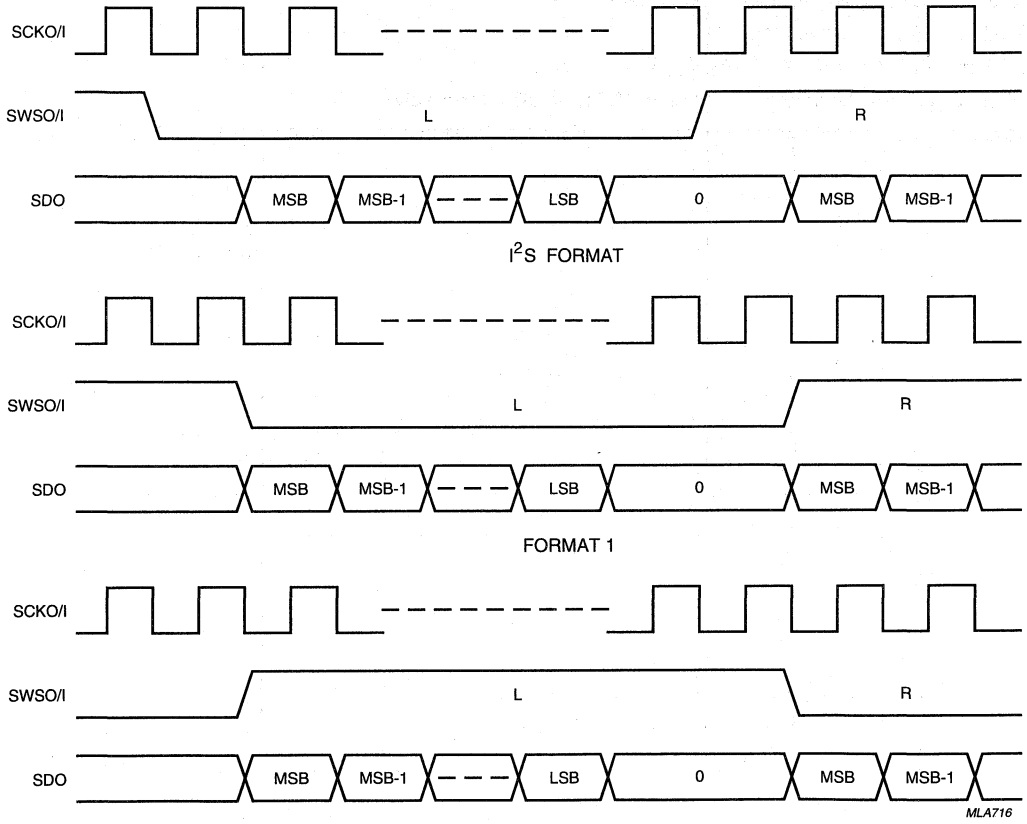


Fig.3 Output interface modes.

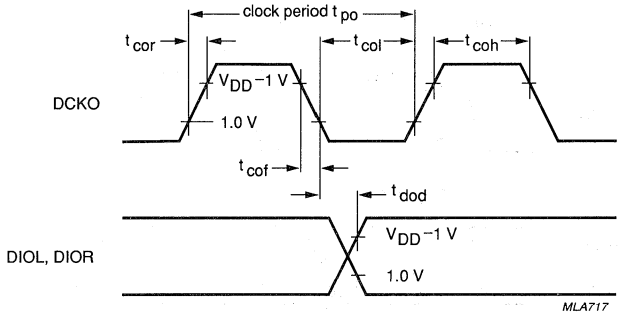


Fig.4 One bit code output timing.

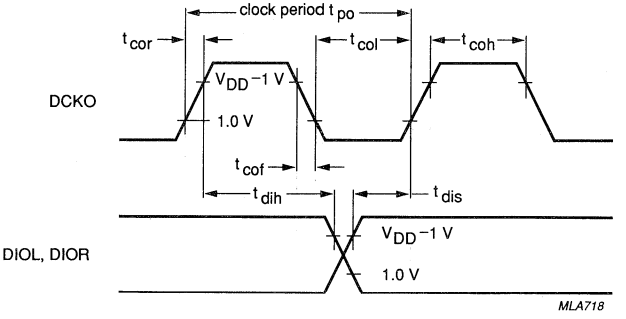


Fig.5 One bit code input timing.

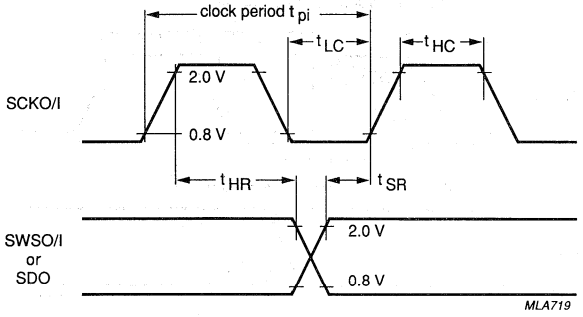


Fig.6 Serial output timing.

APPLICATION INFORMATION

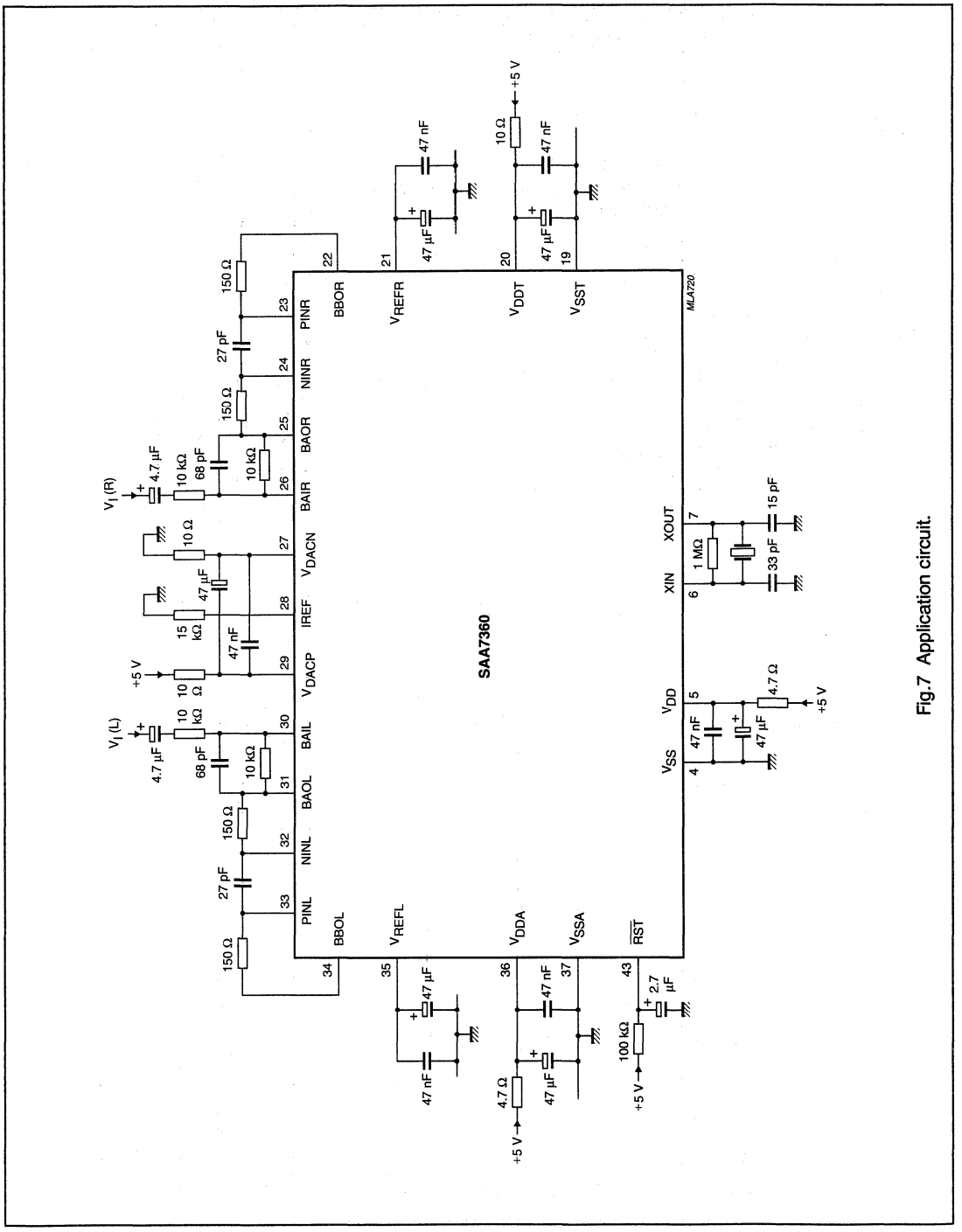


Fig.7 Application circuit.

DIGITAL SATELLITE RADIO BROADCASTING TUNER DECODER (SAT-2)

GENERAL DESCRIPTION

The SAA7500 performs a decoder function for digital satellite sound broadcasting tuners. It is designed to decode one of 16 stereo channels broadcasting audio signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.**

Features

- Clock recovery
- Differential decoding
- Main frame synchronization
- Swapping half-frames in case of inversion
- Unscrambling
- Demultiplexing
- Subframe synchronization
- Error correction and concealment
- Scale factor decoding with error correction
- Shift into the original values using the scale factors
- Mute in case of synchronization loss

QUICK REFERENCE DATA

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	4.5	5.5	V
Power dissipation	P_{tot}		500	mW
Clock frequency	T_{20N}	20.48		MHz

PACKAGE OUTLINE

68-lead plastic leaded chip carrier (PLCC); 'pocket' version (SOT188AA).

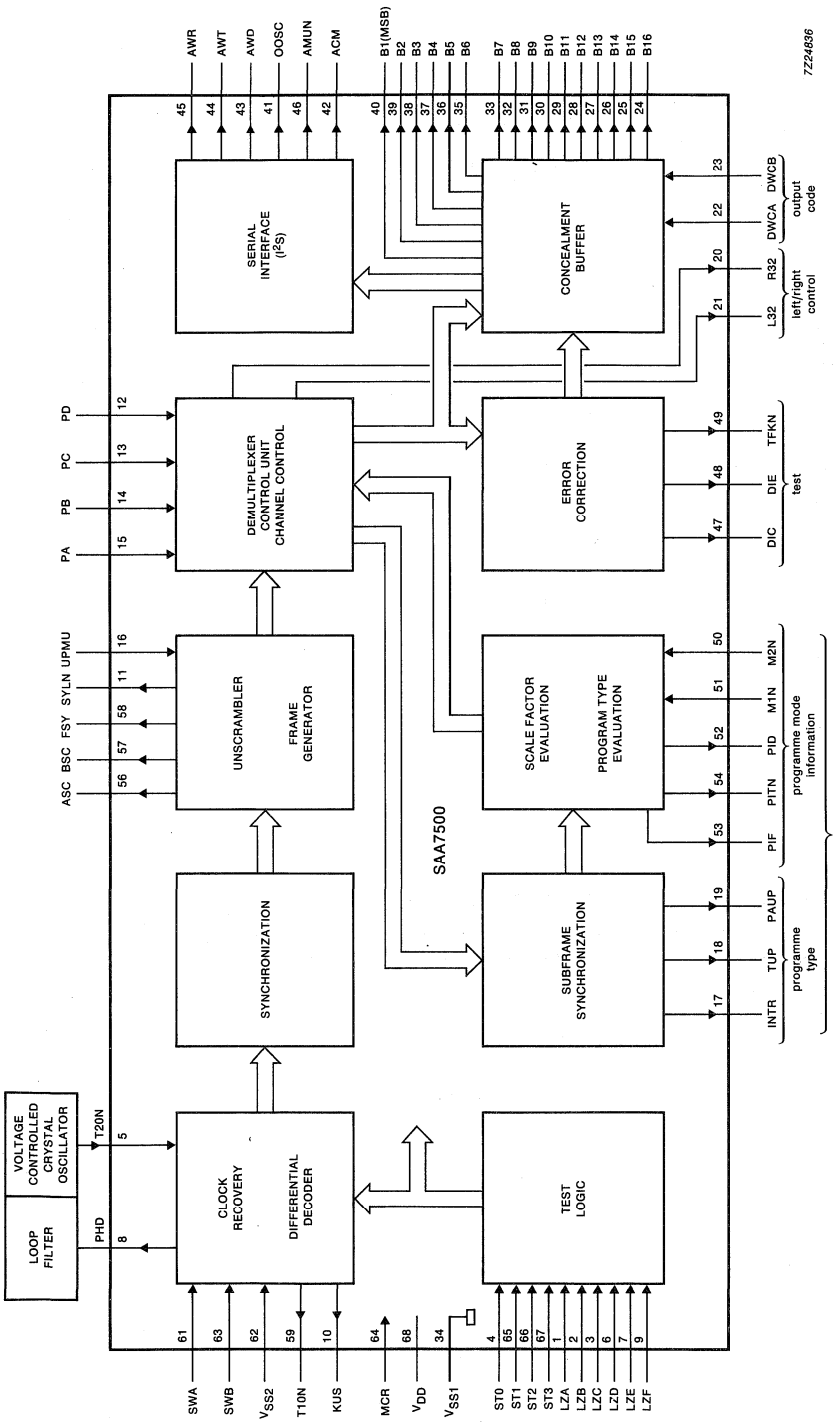


Fig.1 Block diagram.

PINNING

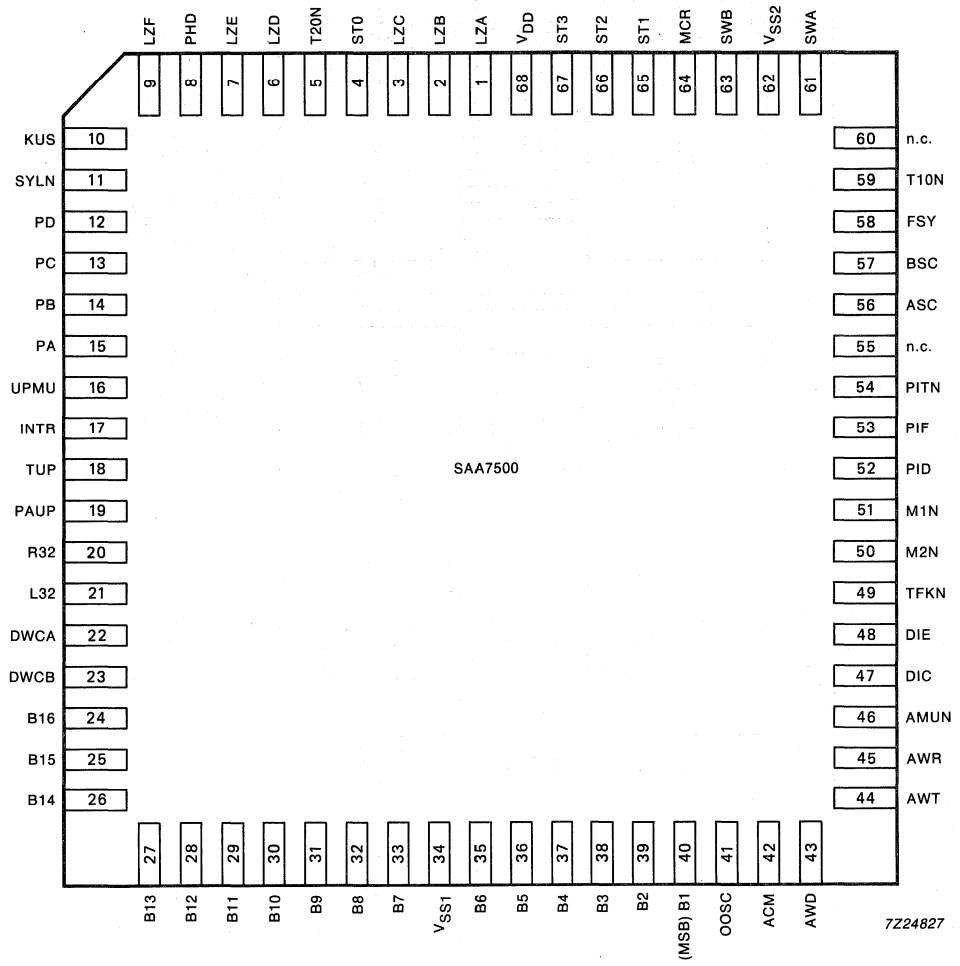


Fig.2 Pinning diagram; for pin functions see next page.

Pin functions

(1) = CMOS level input. (2) = TTL level input. (3) = CMOS level input with pull down resistor.

pin no.	mnemonic		description
1	LZA	I(3)	phase adjustment for the internal clock.
2	LZB	I(3)	phase adjustment for the internal clock.
3	LZC	I(3)	phase adjustment for the internal clock.
4	ST0	I(3)	control input for testing.
5	T20N	I(1)	20.48 MHz clock input from voltage controlled oscillator (VCX).
6	LZD	I(3)	control input for testing.
7	LZE	I(3)	control input for testing.
8	PHD	O	phase control signal for VCX.
9	LZF	I(3)	control input for testing.
10	KUS	O	test output (A'B' swap).
11	SYLN	O	synchronization indication flag.
12	PD	I(2)	programme number input selector (MSB)
13	PC	I(2)	programme number input selector.
14	PB	I(2)	programme number input selector.
15	PA	I(2)	programme number input selector (LSB).
16	UPMU	I(2)	mute input (controlled by microcomputer).
17	INTR	O	interrupt flag for microcomputer.
18	TUP	O	programme type interface (clock).
19	PAUP	O	programme type interface (data).
20	R32	O	multiplex control signal for right channel.
21	L32	O	multiplex control signal for left channel.
22	DWCA	I(3)	DA-converter mode select input.
23	DWCB	I(3)	DA-converter mode select input.
24-33	B16-7	O	audio data for parallel interface, bits 16 (LSB) to 7.
34	V_{SS1}	I	ground (supply).
35-40	B6-1	O	audio data for parallel interface, bits 6 to 1 (MSB).
41	OOSC	O	4.096 MHz clock output.
42	ACM	O	concealment flag (for SAA7220P/C).
43	AWD	O	audio data (for SAA7220P/C).
44	AWT	O	bit clock (for SAA7220P/C).
45	AWR	O	word select signal (for SAA7220P/C).
46	AMUN	O	mute signal (for SAA7220P/C).
47	DIC	O	data output for testing.
48	DIE	O	data output for testing.

pin no.	mnemonic		description
49	TFKN	O	burst clock for test data.
50	M2N	I(2)	channel mode select input.
51	M1N	I(2)	channel mode select input.
52	PID	O	programme information (PI) interface output (data).
53	PIF	O	programme information (PI) interface output (window signal).
54	PITN	O	programme information (PI) interface output (clock).
55	n.c.		not connected.
56	ASC	O	data output for 10.24 Mbit/s interface.
57	BSC	O	data output for 10.24 Mbit/s interface.
58	FSY	O	window signal for 10.24 Mbit/s interface.
59	T10N	O	10.24 MHz clock output.
60	n.c.		not connected.
61	SWA	I(2)	10.24 Mbit/s data input.
62	V_{SS2}	I	ground (screen).
63	SWB	I(2)	10.24 Mbit/s data input.
64	MCR	I(1)	master reset.
65	ST1	I(3)	control input for testing.
66	ST2	I(3)	control input for testing.
67	ST3	I(3)	control input for testing and mode select for 10.24 Mbit/s interface.
68	V_{DD}	I	power supply.

FUNCTIONAL DESCRIPTION

General

The SAA7500 has been designed to decode 16 stereo channel sound broadcasting signals in accordance with the German standard - **Technische Richtlinie ARD/ZDF Nr. 3R1.** The channel carrying the sound broadcast programme is selected and converted into an intermediate frequency by a frontend. The signal is then amplified and demodulated (4 PSK (Phase Shift Keying) with carrier recovery). The outputs from the demodulator are two differential coded signals that are input into the SAA7500. The SAA7500 decoder outputs the audio data, of the selected stereo or mono channel, as linear quantized 16-bit audio samples.

Selection of the desired audio channel, as well as stereo or mono mode, is controlled by inputs PA, PB, PC and PD. These inputs may be driven directly by switches or controlled by a microcomputer.

When under the control of a microcomputer, the SAA7500 transmits serial data to the microcomputer on the type of programme (16 stereo or 32 mono). The corresponding synchronization of the subframe is partly performed by the SAA7500 (every 2 ms) and at a higher level by the microcomputer (every 16 ms). The SAA7500 also sends to the microcomputer, programme information code data together with its clock and window signal.

The circuit automatically performs the system error correction and concealment. In the transmit error rate range of 0 to 3×10^{-3} a theoretical C/N (carrier-to-noise ratio) gain of about 6 dB is obtained. The residual error rate is nearly zero for transmit error rates $\leqslant 3 \times 10^{-4}$.

The remaining functions, such as clock recovery, main and subframe synchronization and scale factor decoding, are protected in a similar manner so that they will not influence the residual error rate.

Clock recovery

The baseband signals A' and B' are connected to the SWA and SWB inputs of the SAA7500. For clock recovery, the phase of the incoming data streams is compared with T10N (half the oscillator frequency). The output of the phase comparator (PHD) controls, by means of the loop filter, the voltage controlled oscillator (both are external to the IC) and thus its output signal T20N.

For energy dispersal, for example, in modulation pauses or with constant signals, the data streams are scrambled during generation. The exceptions are the synchronization words and the special service bits. In order that the phase correspondence between the recovered system clock (T10N) and the input signals A' and B' can be adjusted to a minimum bit error rate (BER), a programmable phase shifter is provided (inputs LZA, LZB, LZC and ST3).

The differential decoder logic delivers the original data streams which may be exchanged depending on the number of mixer stages on the transmission channel. The polarity of the two synchronization words will indicate if this is necessary, if so the two data streams will be automatically switched over.

Synchronization

Using the synchronization circuit, the incoming data streams are first searched for 11-bit Barker codewords. The synchronization circuit permits two errors for both synchronization words, which guards against failure of the synchronization word. If the synchronization word has been detected, the following data is examined at frame length intervals to see if the synchronization word is repeated. If it is repeated, it is acknowledged as a synchronization word (window check) and an internal frame pulse generator takes over further control. There is also a synchronization word failure control which initiates a renewed synchronization word search and mutes the AF output if four successive synchronization word failures occur.

To enhance the performance the result from the error correction circuit is used as an additional input to the synchronization circuit. This is to avoid extra errors through synchronization loss in the case of relative high, but for reception acceptable, bit error rates. This will not affect the rapid detection of

a very high bit error rate or the non-synchronization of the data stream. The decoder will function correctly with a bit error rate up to 3×10^{-3}.

Demultiplexer

After synchronization, the beginning of a frame is marked and the digital signals are defined as to their assignment. First the non-scrambled special service bit from the half frame A is taken out. The rest of both half frames are unscrambled and demultiplexed so that each half frame is split into two substreams with a rate of 5.12 Mbit/s (see Technische Richtlinie ARD/ZDF Nr. 3R1, main frame specification). Using the inputs from the synchronization circuit and the programme selector (inputs PA, PB, PC and PD) the demultiplexer locks on to the selected programme block and generates all the control signals required for further signal processing.

Error correction

The error correction circuit provides for exact identification of two errors in a 63/44 BCH block and correction of the incorrect bits. In the event of more than two errors the identification circuit can identify incorrect BCH blocks with up to five errors.

The BCH block is operated on by a syndrome calculator, the result controls the lines of an error correction matrix. The output of this matrix corrects (inverts) the incorrect bits when data is shifted out from its buffer. The BCH block is then fed through a second syndrome calculator. In the event of more than two errors the result of the whole calculation will be other than zero. This information provides the concealment in the next stages.

The two adjacent samples related to the detected incorrect sample are added and divided by two, the result replaces the incorrect sample (interpolation). In the event of successive bad samples the last corrected sample is held until a good sample is detected (hold function). A high error frequency in the event of synchronization loss will activate the muting function and set the output data to zero.

This information, if concealment is not active, is used in the synchronization circuit as described in that section. When the samples are correct it can be assumed that the synchronization is also correct.

Scale factor, programme type evaluation and shift sunction

The transmitted samples are returned to their original range of values by the scale factor, which is obtained by decoding the ZI-subframe. The start of this frame is coupled to the start of the special services frame, synchronization for this frame uses the same principle as for the main frame. In the scale factor evaluation unit the BCH 14/6 code words (three times transmitted) are fed into a majority selection circuit working at bit level. Subsequently the error check and the correction of a maximum of two errors is carried out.

The SAA7500 contains the synchronization word detection and error check for the subframe synchronization word with its repetition time of 2 ms. The programme type evaluation with its superior synchronization has to be performed external to the chip, for example, by a microcomputer. For this purpose data is available in 8-bit blocks at a serial interface (INTR, PAUP and TUP; block rate = 4000/s). The same microcomputer can also perform the programme selection (inputs PA, PB, PC and PD).

At the input to the concealment buffer the corrected 11 bits (MSB) are combined with the 3 unprotected transmitted bits (LSB). The scale factor determines the required shift-back operations needed to convert the transmitted values back into the original values. Voids that occur are filled with noughts or ones corresponding to the sign bit. The shift-back and filling of voids ensures that no incorrect bits occur above the range defined by the scale factor. The upper 16 bits represent the regenerated audio sample.

FUNCTIONAL DESCRIPTION (continued)

Digital-to-analogue conversion and interfaces

The SAA7500 enables different DAC systems to be used. For control of the SAA7220P/C and TDA1541 a 2.5 external divider must be connected to the 20.48 MHz clock signal to produce the required 8.192 MHz clock signal.

A serial interface is built in with the following outputs: bit clock (AWT), word select (AWR) and audio data (AWD). In addition the mute signal (AMUN) and the concealment flag (ACM) are also available. The SAA7220P/C and TDA1541 are equipped with a digital audio interface for domestic use equivalent to 'IEC proposal No. 84 (secretariat 28; from June 1985)'.
For DACs with a parallel interface in a multiplex mode the audio data are available at the B1(MSB)-B16 outputs. The multiplexing is controlled by the L32 and R32 outputs. Using the mode outputs DWCA and DWCB the code (offset binary or two's complement) and polarity can be selected.

Additional information, including the scale factor is available through the programme information (PI) interface (PID, PITN and PIF). Another interface, using the ASC, BSC and T10N outputs, makes available signals from the differential decoder. These signals are used for bit error measurement and an optimized phase adjustment of the internal clock (refer to 'clock recovery' section).

An optional application of the control signals for mute and concealment operations is possible using the outputs AMUN and ACM. For the mute signal a different time relationship to the unwanted unwanted pulse with very low C/N values may be obtained.

The external application of the concealment signal is recommended; if an additional interpolation is required between additional samples with different levels in the external circuitry (such as the SAA7220P/C).

Truth tables

Table 1 Delay adjustment

pins 1 to 3

LZC	LZB	LZA	delay
0	0	0	$4 \times \tau$
0	0	1	$3 \times \tau$
0	1	0	$2 \times \tau$
0	1	1	$1 \times \tau$
1	0	0	$0 \times \tau$
1	0	1	$-1 \times \tau$
1	1	0	$-2 \times \tau$
1	1	1	$-3 \times \tau$

$\tau \approx 1.5$ x gate delay time (NAND)

Table 2 Master reset

pin 64

MCR	function
0	operation
1	master reset

Table 3 Mute

pin 16

UPMU	function
0	no
1	yes

Table 4 Programme number

pins 12 to 15

PD	PC	PB	PA	programme no.
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.	.	.	.	.
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

Table 5 Phase control signal

pin 8

PHD	phase
0	lead phase
1	lag phase

Table 6 Synchronization indication

pin 11

SYLN	synchronization
0	yes
1	no

Table 7 Mode select for data outputs ASC and BSC for 10.24 Mbit/s interface

pin 67

ST3	data ASC/BSC
0	after unscrambler
1	before unscrambler

Table 8 Data converter mode select B1(MSB) to B16

pins 22 and 23

DWCB	DWCA	DA converter mode
0	0	compl. offset binary
0	1	offset binary
1	0	compl. 2's complement
1	1	2's complement

Table 9 Channel mode select

pins 50 and 51

M2N	M1N	channel mode
0	0	mono (1+2)
0	1	mono R(2)
1	0	mono L(1)
1	1	stereo

Table 10 Concealment

pin 42

ACM	function
0	no
1	yes

Table 11 Mute

pin 46

AMUN	mute
0	yes
1	no

Table 12 Interrupt

pin 47

INTR	interrupt
0	no
1	yes

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0.5	7.0	V
Input voltage range*	V_I	−0.5	V_{DD} + 0.5	V
Input current	I_I	−	± 10	mA
Output current	I_O	−	± 10	mA
Supply current in V_{SS}	I_{SS}	−	28	mA
Supply current in V_{DD}	I_{DD}	−	28	mA
Total power dissipation	P_{tot}	−	500	mW
Operating ambient temperature range	T_{amb}	−25	+85	°C
Storage temperature range	T_{stg}	−55	+150	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling, however, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices (see Handling MOS Devices).

The PLCC-68 package can only be guaranteed with soldering temperatures up to a maximum of 235 °C.

* V_{DD} + 0.5 must not exceed 7.0 V.

DC CHARACTERISTICS

T_{amb} = 0 °C to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	4.5	–	5.5	V
Supply current	Fig.10	I_{DD}	–	12.5	–	mA
Quiescent supply current	note 1	I_{DDq}	–	–	50	μA
Inputs I(1)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(2)						
Input voltage LOW		V_{IL}	–	–	0.8	V
Input voltage HIGH		V_{IH}	2.0	–	–	V
Input current LOW	note 2	$-I_{IL}$	–	–	10	μA
Input current HIGH	note 2	I_{IH}	–	–	10	μA
Inputs I(3)						
Input voltage LOW		V_{IL}	–	–	0.3 V_{DD}	V
Input voltage HIGH		V_{IH}	0.7 V_{DD}	–	–	V
Pull down resistor		R_I	25	50	100	kΩ
Outputs O						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	–	–	0.5	V
Output voltage HIGH	I_{OH} = 1 mA	V_{OH}	4.0	–	–	V

Notes to DC characteristics

1. T_{amb} = 25 °C, all inputs at V_{SS} or V_{DD}, all outputs open.
2. At 25 °C max. 1 μA.

AC CHARACTERISTICS

T_{amb} = 0 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
T20N clock pulse	Fig.3					
Pulse width HIGH		t_{WH}	15	20	–	ns
Pulse width LOW		t_{WL}	15	22	–	ns
T20N pulse period		t_{P20}	48	48.8	–	ns
Data input timing	Fig.4					
Set-up time for data SWA and SWB to T10N	note 1	t_{SWL}	–	50	–	ns
T10N pulse period T_{PSW}	note 2	t_{P10}	–	97.6	–	ns
Main frame timing	Fig.5					
Main frame sync pulse		t_{SYNC}	–	$11t_{P10}$	–	ns
Audio data timing	Fig.6					
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
Load pulse width HIGH		t_{LPH}	–	6.25	–	μs
Audio data hold		t_{ADH}	–	1	–	μs
I²S timing	Fig.7					
Frequency AWT signal		f_{AWT}	–	1.024	–	MHz
Audio sample repetition time		t_{SAMP}	–	31.25	–	μs
PI interface timing	Fig.8					
Frequency PITN signal		f_{PITN}	–	32	–	kHz
PITN pulse period		t_{PITN}	–	31.25	–	μs
PIF pulse width HIGH		t_{PIFH}	–	$22t_{PITN}$	–	μs
PIF pulse period		t_{ZI}	–	2	–	ms
Output timing Programme type interface	Fig.9					
INTR pulse period		t_{INTR}	–	250	–	μs
INTR pulse width HIGH		t_{PINH}	–	31.25	–	μs

Notes to AC characteristics

1. Due to noise, the period t_{SWL} may occasionally vary between 30 and 70 ns.
2. Due to noise, the period time t_{PSW} may occasionally vary between 77.6 and 117.6 ns.

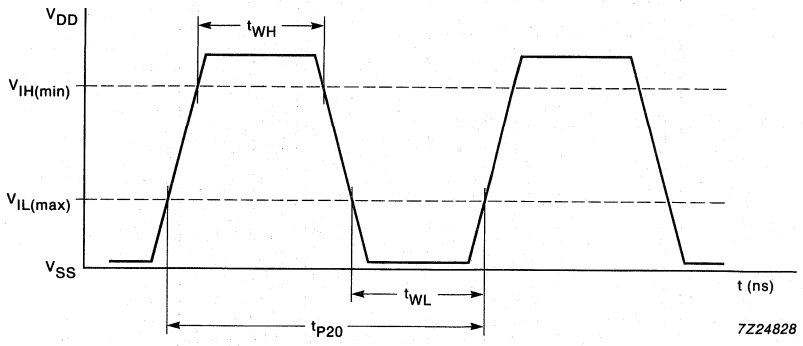


Fig.3 Waveform at clock input T20N (pin 5).

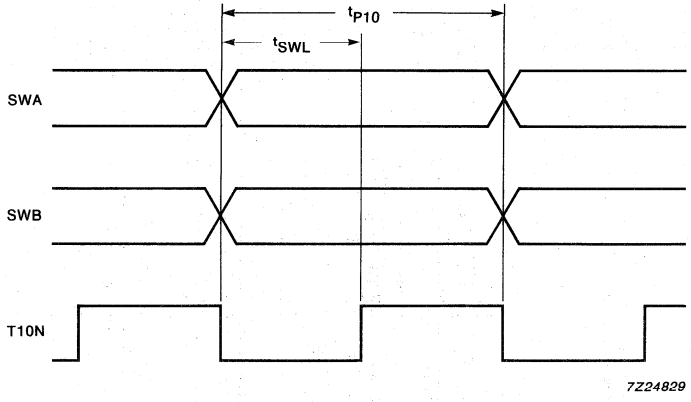


Fig.4 Data input timing (pins 59, 61 and 63).

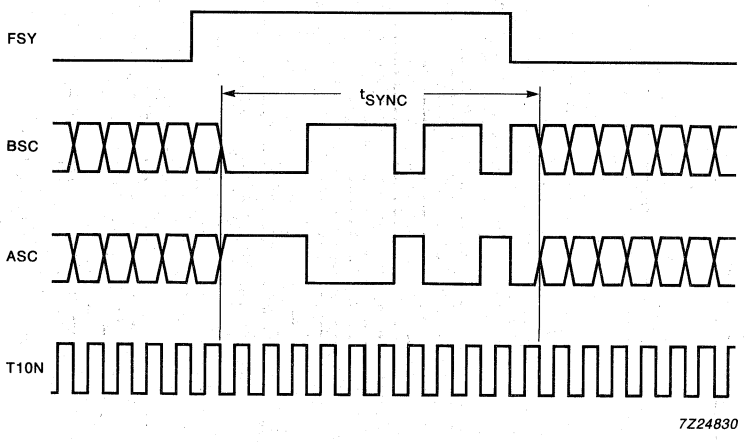


Fig.5 Output timing for 10.24 Mbit/s interface (pins 56, 57, 58 and 59).

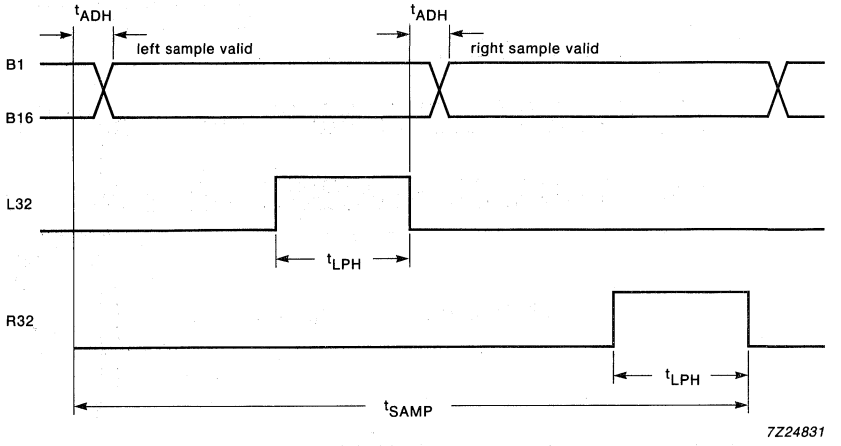


Fig.6 Audio data timing parallel out (pins 40 to 35, 33 to 24, 21 and 20).

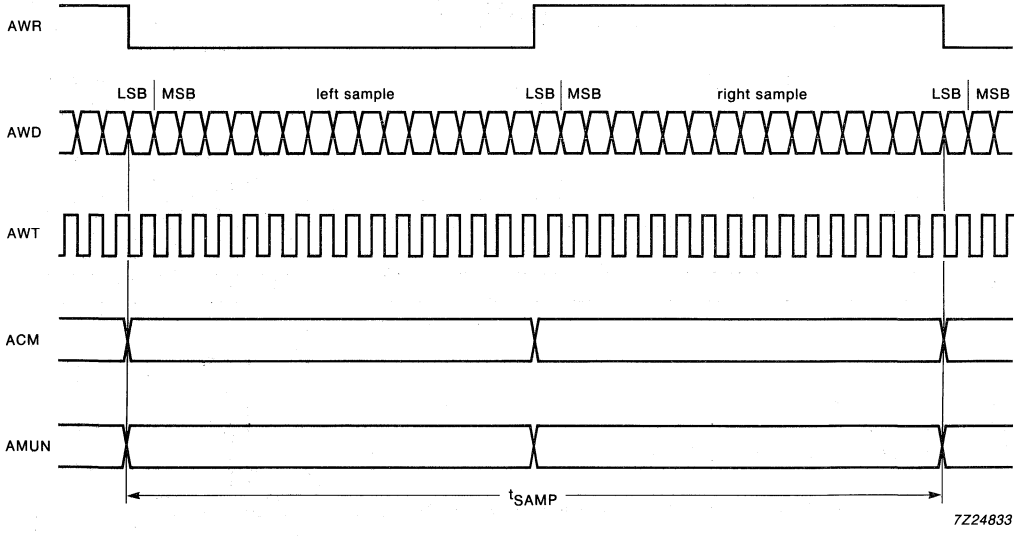


Fig.7 Inter-IC Sound (I²S) timing and mute and interpolation flags (pins 42 to 46).

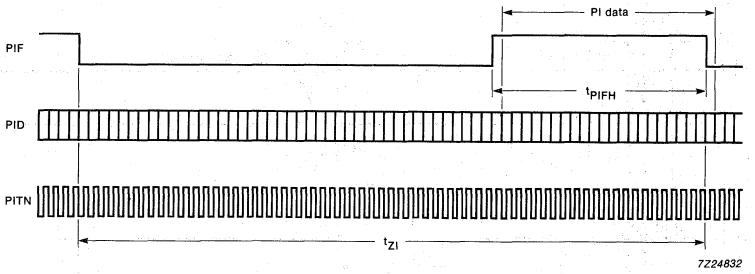
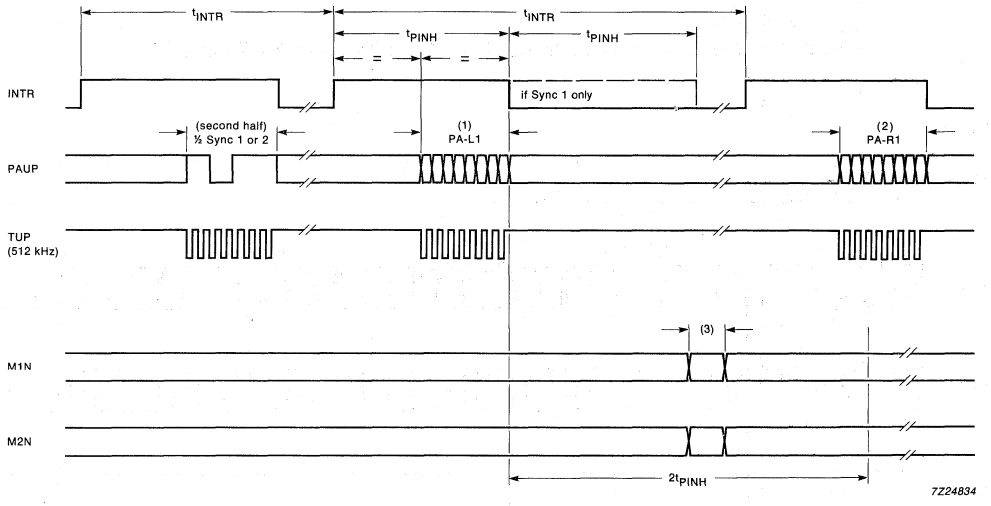


Fig.8 PI interface timing (pins 52 to 54).



(1) Programme type - left
(2) Programme type - right
(3) This time is approximately 10 μs

Fig.9 Output timing programme type interface (pins 17 to 19).

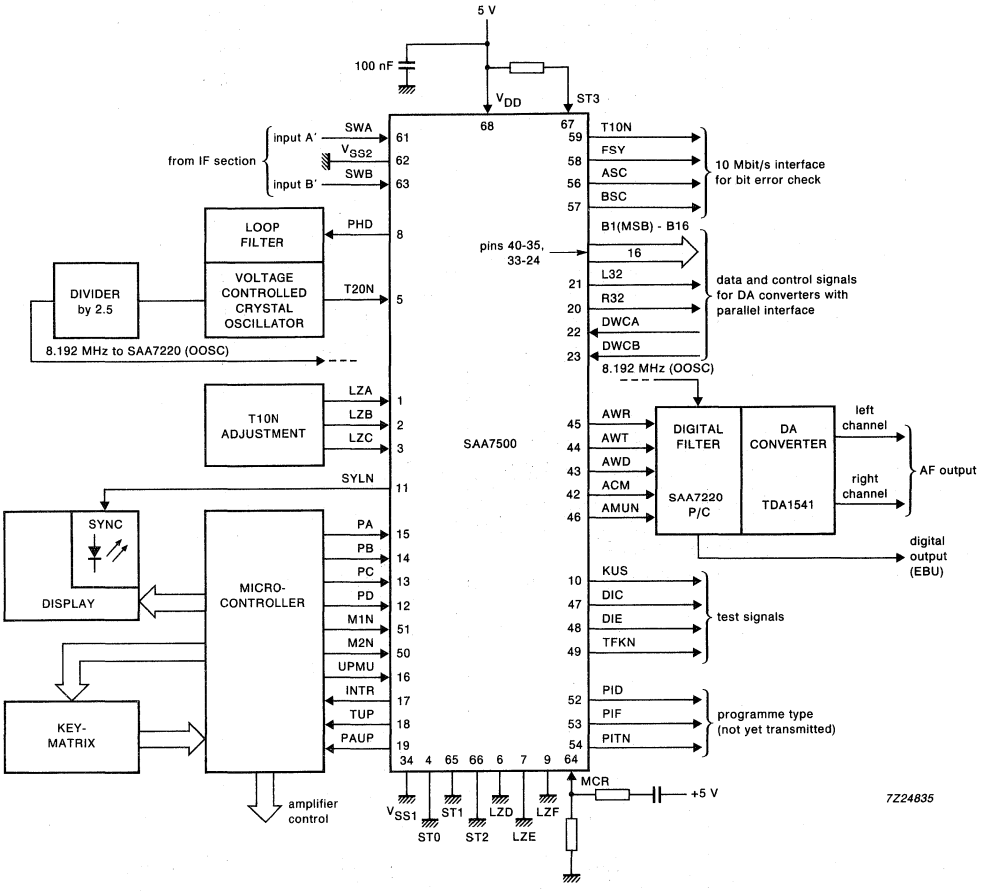


Fig.10 Application proposal.

RADIO DATA SYSTEM (RDS) DEMODULATOR

GENERAL DESCRIPTION

The CMOS IC, SAF7579, recovers the additional inaudible information from the Radio Data System (RDS) which is transmitted on FM sound channels.

The data signal, RDDA, and the clock signal, RDCL, are provided as outputs for further processing by a suitable microcomputer.

The operating functions within the device are in accordance with the EBU specification TECH 3244-E.

Features

- 57 kHz carrier regeneration (Costas loop)
- Synchronous demodulator for 57 kHz modulated RDS signals
- 4.332 MHz crystal oscillator with variable dividers
- Clock generation with lock on and biphase data rate
- Biphase symbol decoder with "Integrate and Dump" function
- Differential decoder
- Indicator output for ARI (Autofahrer Rundfunk Information) detection and RDS signal quality

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (at idle, oscillator on)	I_{DD}	–	1.5	–	mA
Oscillator frequency	f_{osc}	–	4.332	–	MHz
Operating ambient temperature range	T_{amb}	−40	–	+85	°C

PACKAGE OUTLINES

SAF7579T: 16-lead mini-pack; plastic (SO16L; SOT162A).
SAF7579U/F: chips uncased, on foil.
SAF7579U/T: chips on wafer.

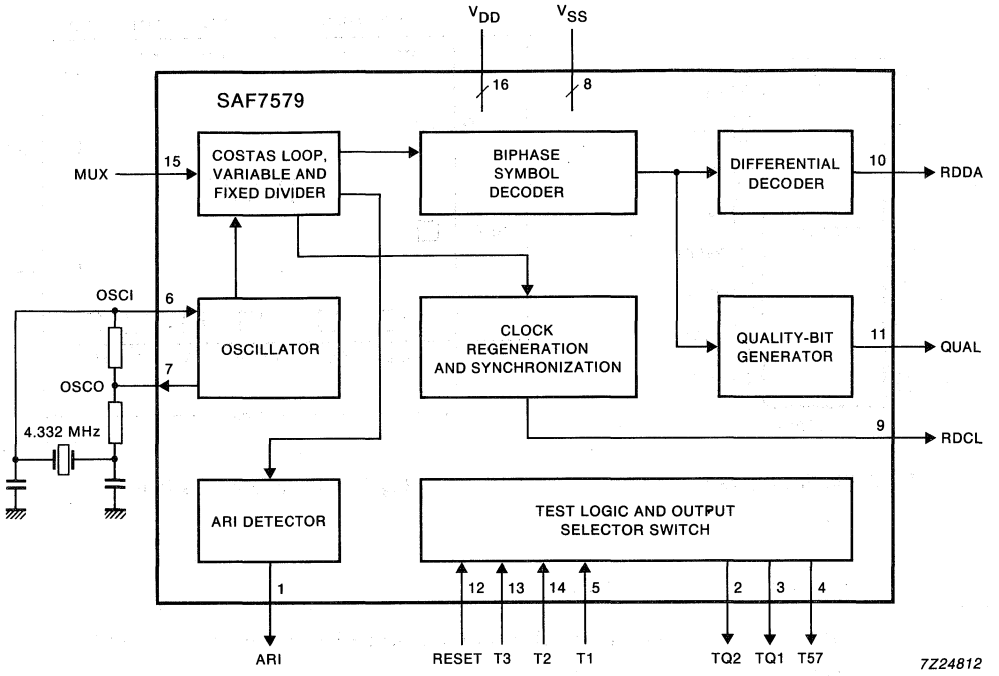


Fig.1 Block diagram.

PINNING

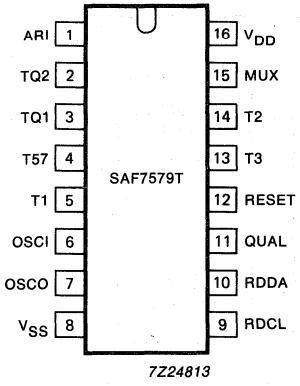


Fig.2 Pinning diagram.

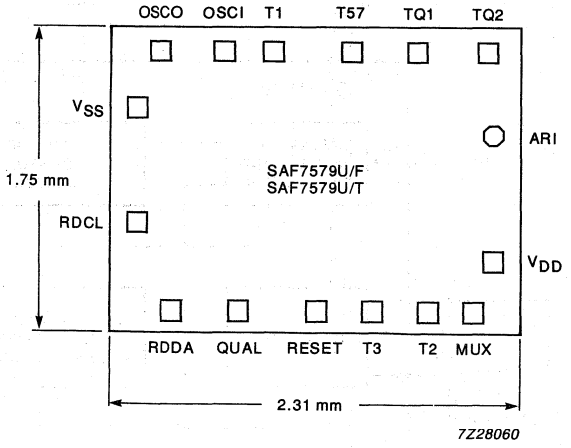


Fig.3 Bonding pad locations.

pin	mnemonic	description
1	ARI	Output for ARI indication (ARI = HIGH when ARI present)
2	TQ2	Test output 2
3	TQ1	Test output 1
4	T57	57 kHz output
5	T1	Test input 1
6	OSCI	Oscillator input
7	OSCO	Oscillator output
8	V_{SS}	Ground
9	RDCL	Output for RDS clock
10	RDDA	Output for RDS data
11	QUAL	Output for signal quality indication (HIGH = good)
12	RESET	Reset input for test logic
13	T3	Test input 3
14	T2	Test input 2
15	MUX	RDS input signal (band and amplitude limited)
16	V_{DD}	Supply voltage

FUNCTIONAL DESCRIPTION

The multiplex output signal from the FM demodulator is passed through a narrow band-pass filter to produce the 57 kHz RDS and ARI information. This signal is then limited and amplified to TTL levels. The resultant 57 kHz square wave is fed to the MUX input of the SAF7579.

The RDS information is demodulated by a synchronous demodulator with carrier regeneration and the suppressed carrier is recovered from the two received sidebands (Costas loop). This demodulated signal is then low-pass filtered in such a way that the overall pulse shape approaches a cosine. This occurs in conjunction with the following "Integrate and Dump" circuit.

The data-spectrum shaping has been split equally between the transmitter and receiver so that, ideally, the data filtering at the receiver should be the same as that of the transmitter. The overall data-channel spectrum shaping of the transmitter and receiver should then be 100% roll-off.

The "Integrate and Dump" circuit performs an integration over a clock period. This results in a demodulated and valid RDS signal in the form of biphase symbols being outputted from the "Integrate and Dump" circuit. The final stages of RDS data processing are biphase symbol decoding and differential decoding. After synchronization with the clock the RDS data appears at the RDDA output of the device.

The output of the biphase symbol decoder is evaluated by a special circuit to provide an indication of good or corrupt data at the QUAL output (HIGH = good data, LOW = corrupt data).

The existence of an ARI signal in the multiplex signal is indicated by a HIGH on the ARI output (pin 1).

A 4.332 MHz ($\pm 10^6$ absolute maximum)* crystal oscillator is used (with both, fixed and variable dividing) to run the SAF7579. This oscillator also produces the 1187.5 Hz RDS clock (RDCL), which is synchronized with the incoming data. Which ever clock edge is considered (positive or negative) the data will remain valid for 417 μs after the clock transition. The timing of a data change is 4 μs before a clock change. Which clock transition (positive or negative edge) the data change occurs in, depends on the lock conditions and is arbitrary (bit-slip).

During poor reception it is possible for phase faults to occur. In this situation the clock signal will continue uninterrupted and the data will be constant for 1.5 clock periods. In normal conditions phase faults do not occur on a cyclic basis. If however, phase faults do occur in this way, the minimum spacing between two possible phase faults will depend on the data being transmitted. The minimum spacing cannot be shorter than 16 clock periods.

The quality signal (QUAL) will only change at the time of a data change.

* Philips Components part no. 9922 520 00189.

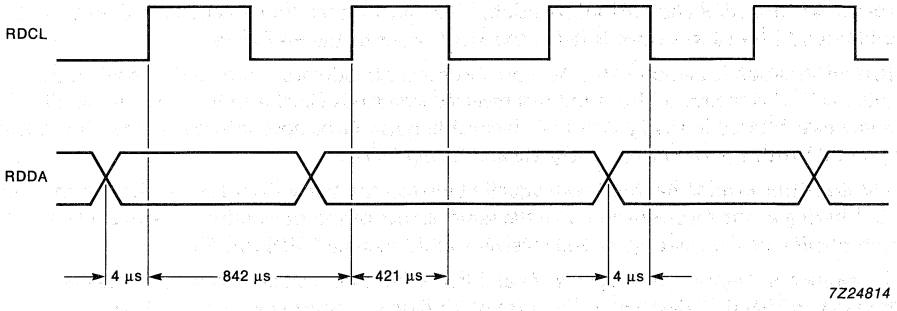


Fig. 4 Timing diagram for RDS signals with phase shift (bit-slip).

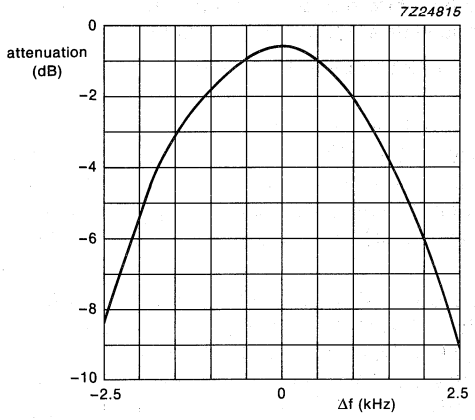
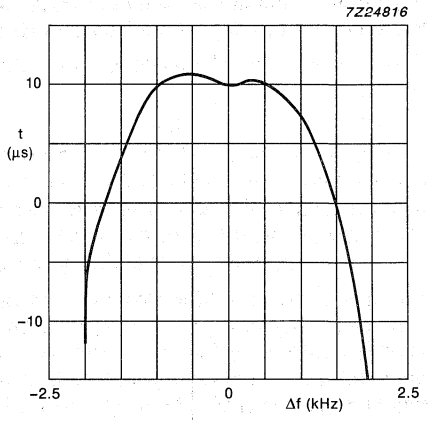


Fig. 5 Transmission curve.



0 ≙ +200 µs.

Fig. 6 Relative group delay.

RATINGS

Limiting values in accordance with Absolute Maximum System (IEC 134)

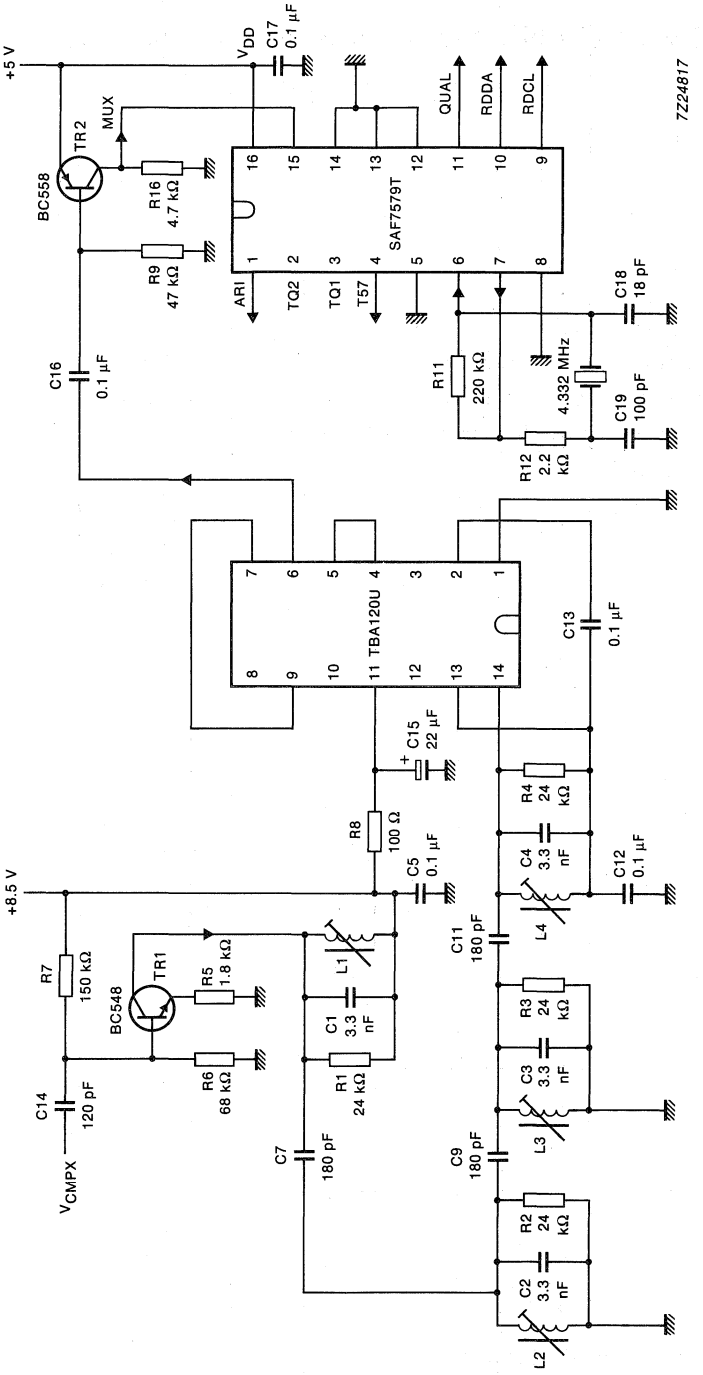
parameter	symbol	min.	typ.	max.	unit
Supply current	V_{DD}	−0.5	–	7	V
Supply current	I_{DD}, I_{SS}	–	–	60	mA
Input and output voltage	V_I, V_O	−0.5	–	V_{DD} + 0.5 (max. 7 V)	V
Input and output currents	$\pm I_I$, $\pm I_O$	–	–	10	mA
Total power dissipation*	P_{tot}	–	–	500	mW
Operating ambient temperature range	T_{amb}	−40	–	+85	°C
Storage temperature range	T_{stg}	−65	–	+150	°C

* Above +70 °C derate linearly with 8 mW/K.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_{DD}	4.5	5	5.5	V
Supply current	no load-current but oscillator on; T_{amb} = 25 °C; V_{DD} = 5 V	I_{DD}	–	1.5	–	mA
Quiescent supply current	all inputs at V_{DD} or V_{SS}, all outputs open	I_{DD}	–	–	50	μA
MUX RESET and OSCI inputs (inputs with hysteresis)						
Input voltage						
HIGH		V_{IH}	80% V_{DD}	–	V_{DD}	V
LOW		V_{IL}	0	–	20% V_{DD}	V
Hysteresis		V_{hyst}	–	0.5	–	V
Input leakage current		$\pm I_{LI}$	–	–	1	μA
Inputs T1, T2 and T3						
Input voltage						
HIGH		V_{IH}	70% V_{DD}	–	V_{DD}	V
LOW		V_{IL}	0	–	30% V_{DD}	V
Input leakage current		$\pm I_{LI}$	–	–	1	μA
Outputs RDDA, RDCL, QUAL, ARI, TQ1, TQ2 and T57						
Output voltage						
HIGH	$-I_O$ = 3.2 mA	V_{OH}	V_{DD}−0.4	–	–	V
LOW	I_O = 3.2 mA	V_{OL}	–	–	0.4	V
Output OSCO						
Output voltage						
HIGH	$-I_O$ = 1.6 mA	V_{OH}	V_{DD}−0.4	–	–	V
LOW	I_O = 1.6 mA	V_{OL}	–	–	0.4	V
Data rate for RDS data		f_{RDCL}	–	1187.5	–	Hz
Carrier frequency		f_{T57}	–	57	–	kHz



TOKO coils: 126 ANS/A 3561 HM

Fig.6 Application diagram.

INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12 V
Supply current (pin 9)	I_P	typ.	14 mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1 V
Input resistance (pin 1)	R_i	min.	35 kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5 dB
Total harmonic distortion	THD	typ.	0,25 %
Bandwidth	B	typ.	70 kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19 mV
Suppression pulse duration	t_s	typ.	27 μs
Supply voltage range (pin 9)	V_P		7,5 to 16 V
Operating ambient temperature range	T_{amb}		−30 to +80 °C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT38).
TDA1001BT: 16-lead mini-pack; plastic (SO16; SOT109A).

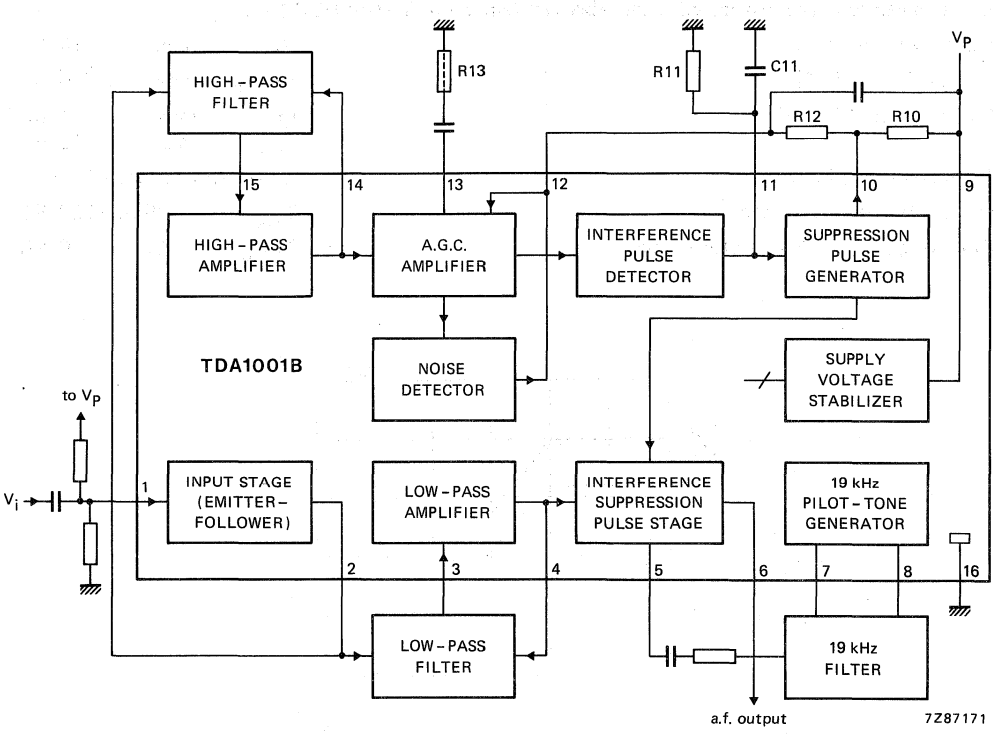


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18 V
Input voltage (pin 1)	V_{1-16}	max.	V_P V
Output current (pin 6)	I_6	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−65 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +80	°C

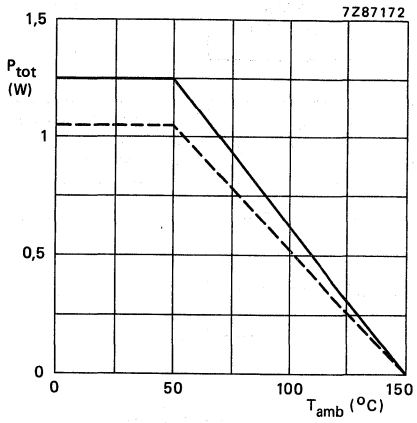


Fig. 2 Power derating curves.
——— in plastic DIL (SOT-38) package (TDA1001B)
– – – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\|Z_{i1}\|$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$	–	6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\|Z_{i8}\|$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\|Z_{o7}\|$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14) of the interference pulse detector	$\pm V_{14int\ m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\ m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
($V_{i(tr)O}$ + 3 dB)	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11) 1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\lvert Z_{i1}\rvert$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4) $V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a de-emphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

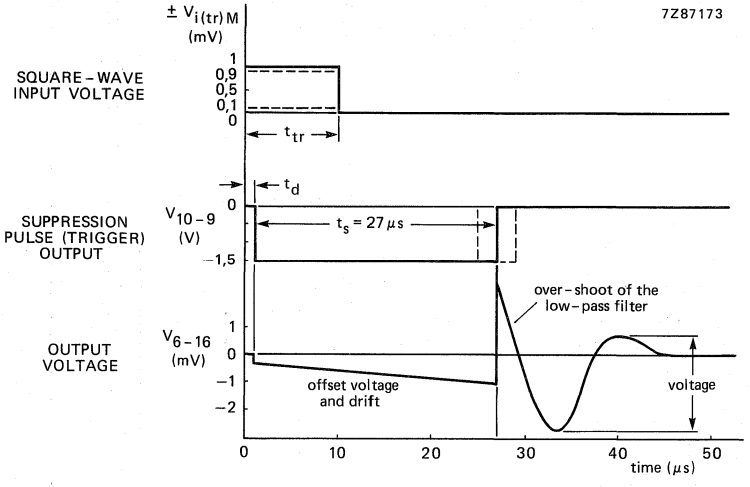


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

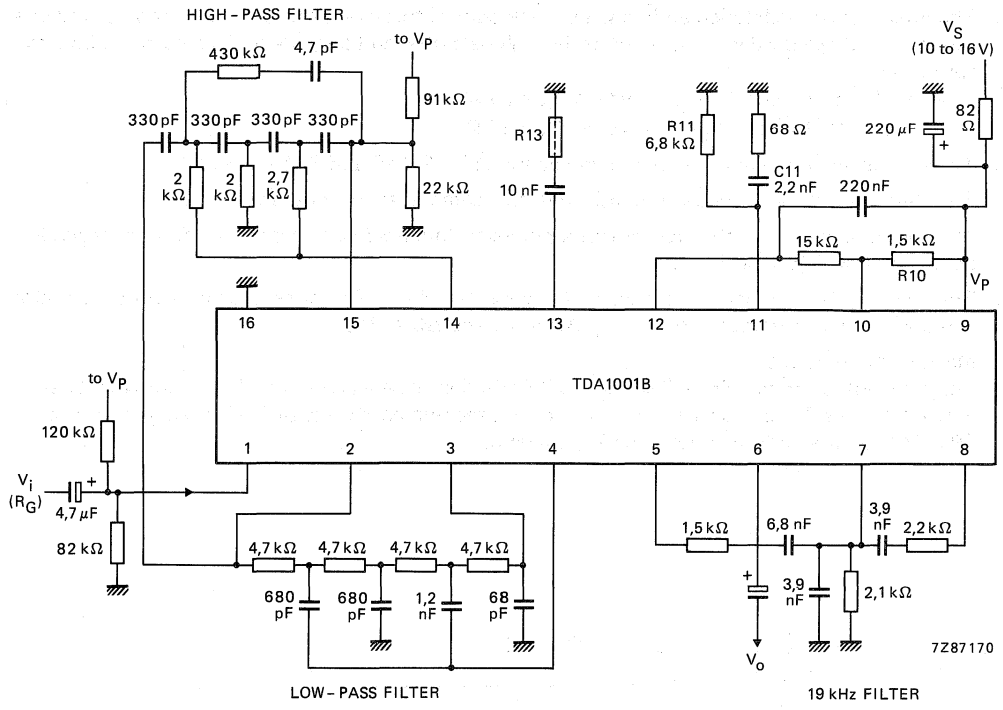


Fig. 4 Application circuit diagram.

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24 V
Repetitive peak output current	I_{ORM}	max.	3 A
Output power at pin 2; d_{tot} = 10%			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4 W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9 W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2 %
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30 kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20 kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31 mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10 mV
Operating ambient temperature	T_{amb}		−25 to + 150 °C
Storage temperature	T_{stg}		−55 to + 150 °C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

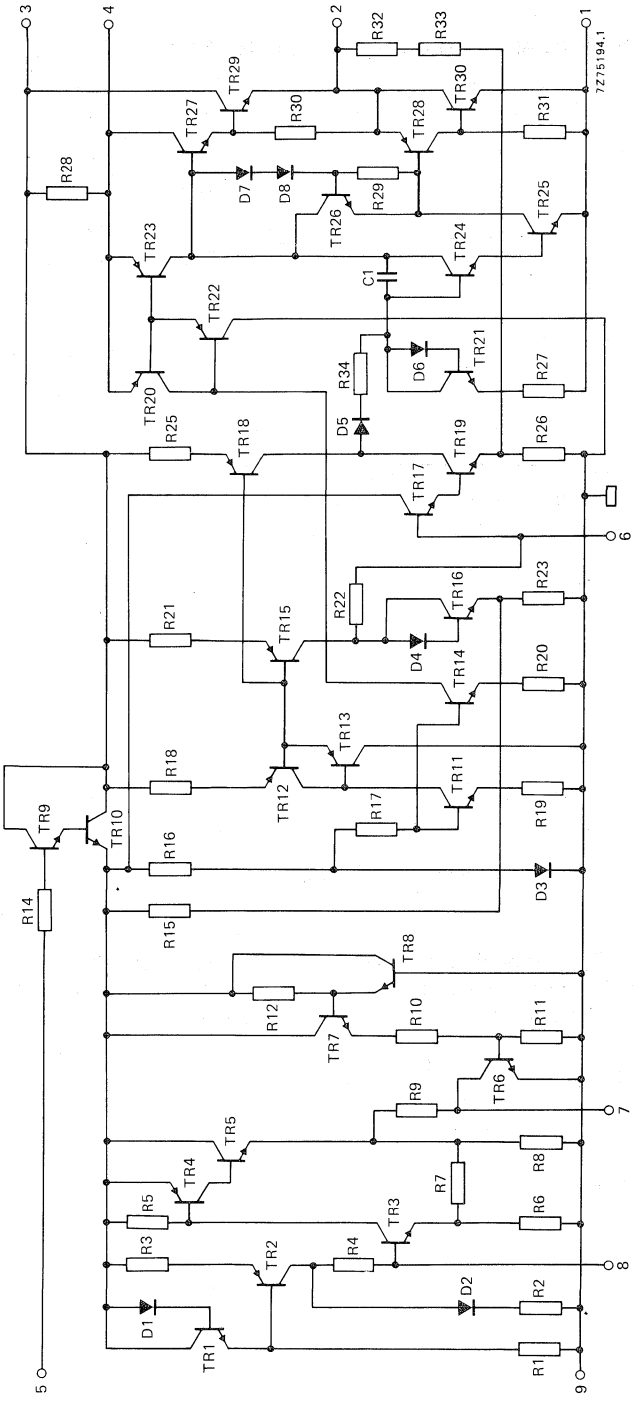


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	5	A
Repetitive peak output current	I_{ORM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100	hours

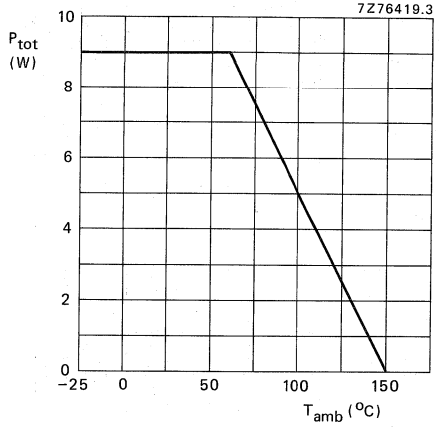


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$R_{th\ h\text{-}a}$ = 23 − (10 + 1) = 12 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P	6 to 24	V
Repetitive peak output current	I_{ORM}	< 3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ. 31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap			
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ. 6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	> 5,9 typ. 6,2	W W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ. 3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ. 5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ. 9	W
Voltage gain			
preamplifier (note 3)	G_{v1}	typ. 24 21 to 27	dB dB
power amplifier	G_{v2}	typ. 30 27 to 33	dB dB
total amplifier	$G_{v\,tot}$	typ. 54 51 to 57	dB dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ. 0,2	%
Efficiency at P_o = 6 W	η	typ. 75	%
Frequency response (−3 dB)	B	80 Hz to 15	kHz
Input impedance			
preamplifier (note 4)	$\lvert Z_i \rvert$	typ. 30 20 to 40	kΩ kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ. 20 14 to 26	kΩ kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ. 20 14 to 26	kΩ kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	> 0,7	V
Noise output voltage (r.m.s. value; note 6)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ. 0,7 < 1,4	mV mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	> 42	dB
at f = 100 Hz; C2 = 1 μF	RR	> 37	dB
Sensitivity for P_o = 5,8 W	V_i	typ. 10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ. 30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

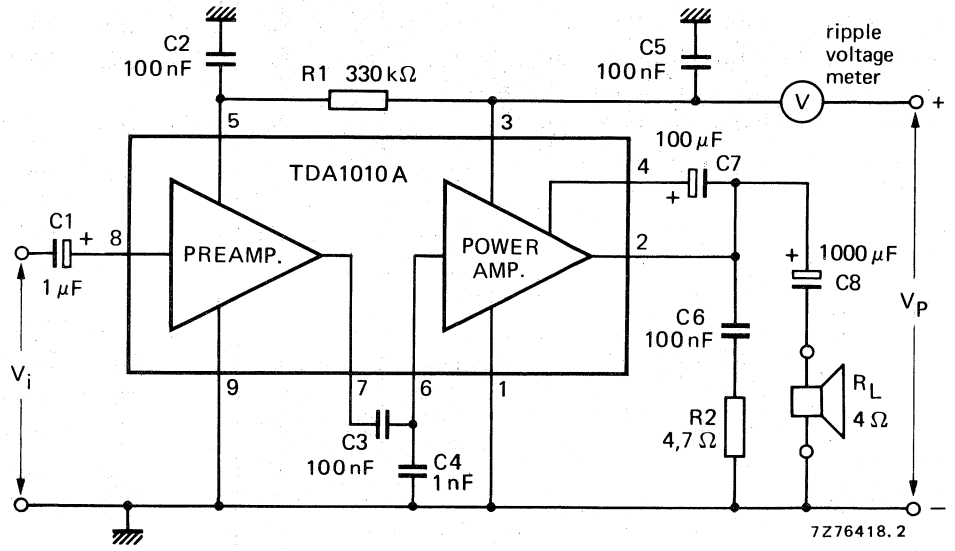


Fig. 3 Test circuit.

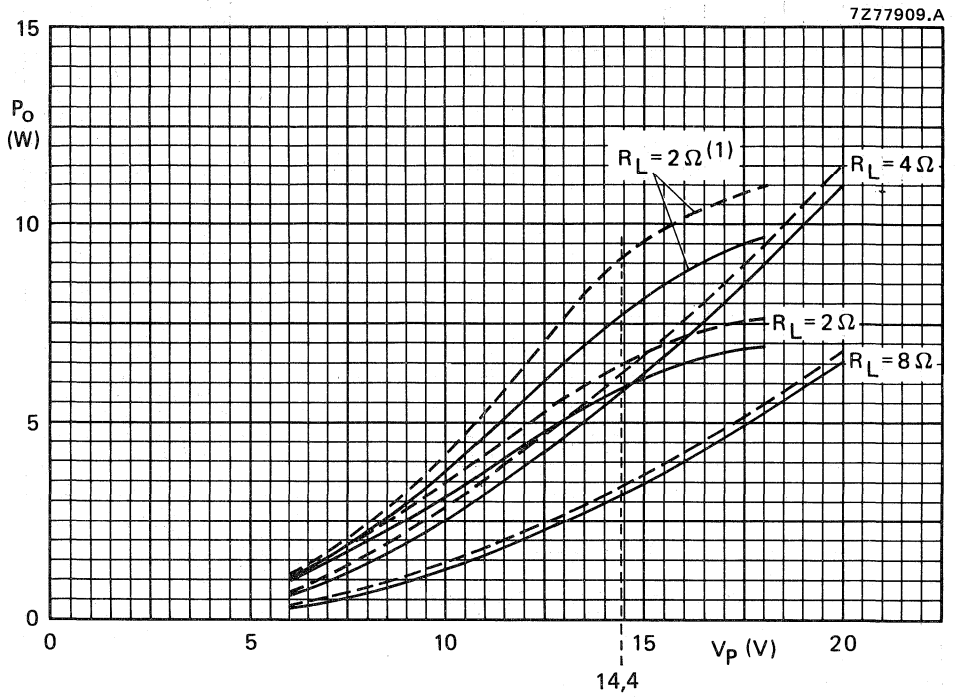


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega$ (1) has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

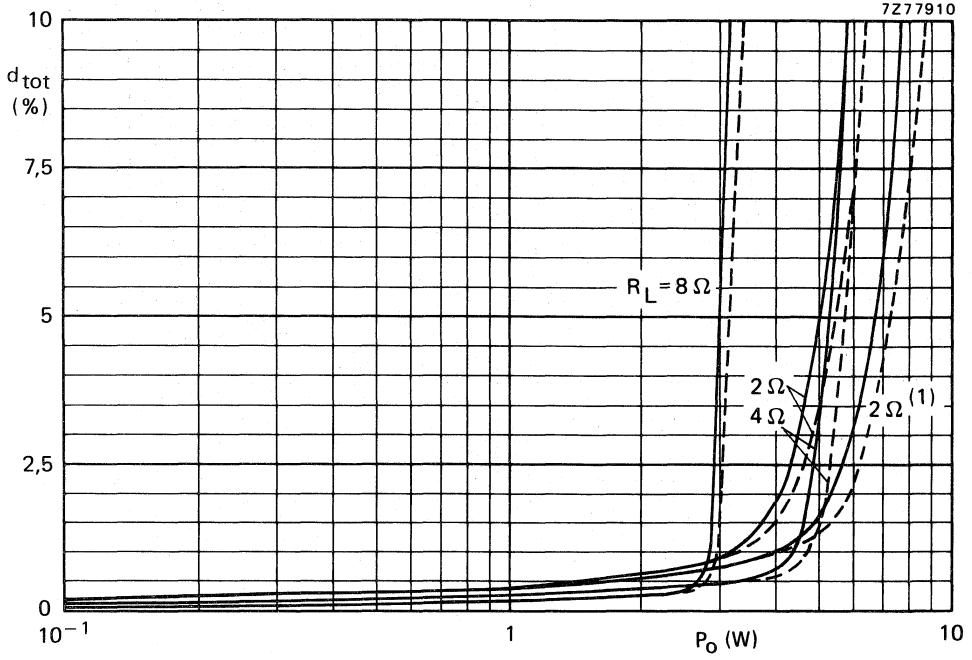


Fig. 5 For caption see preceding page.

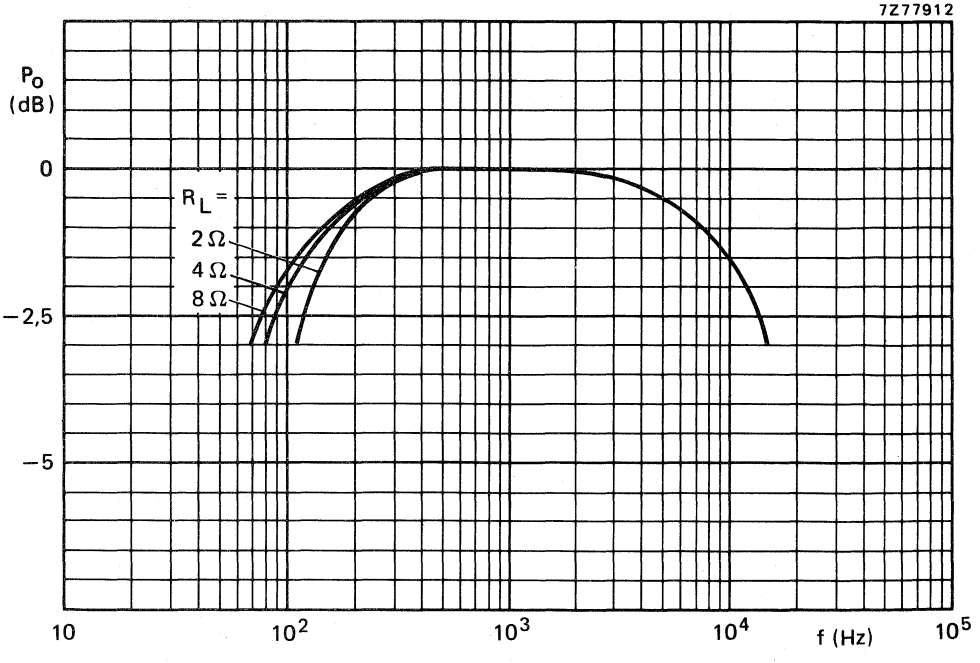


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

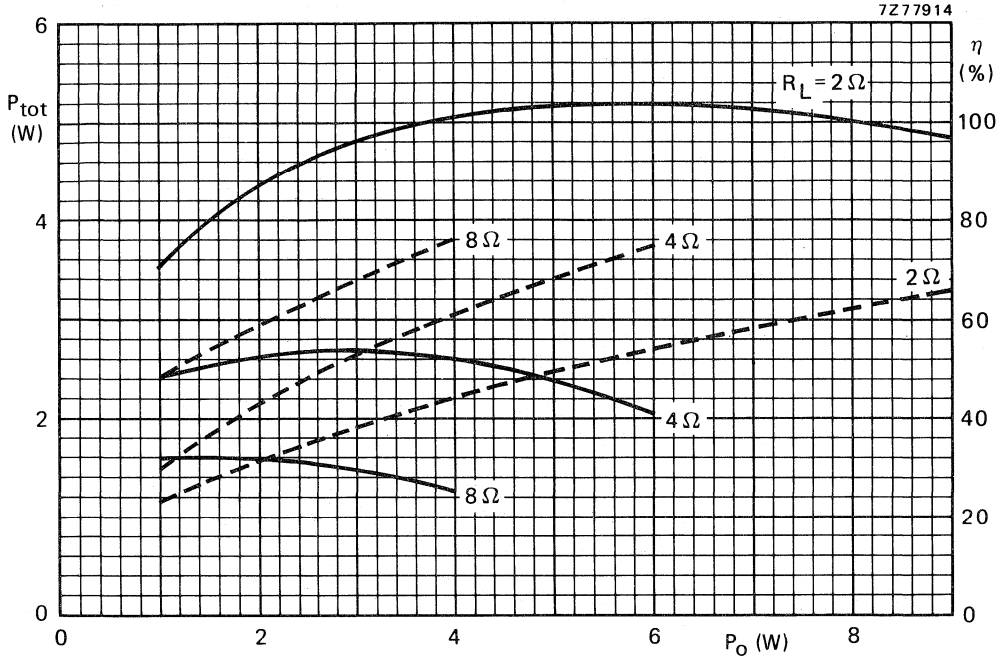


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\,\Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

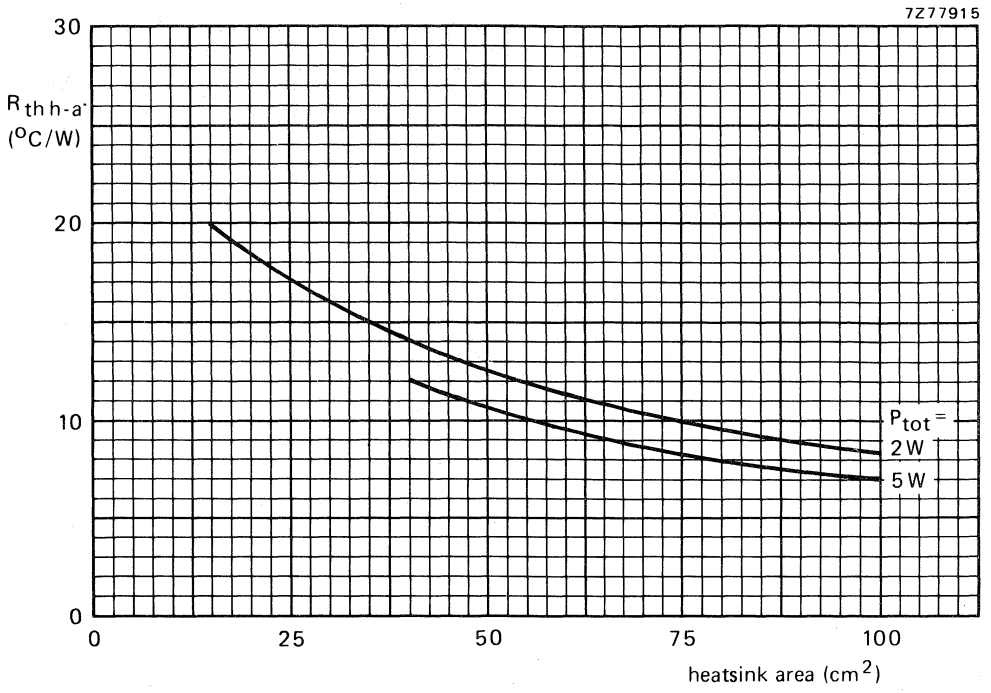


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

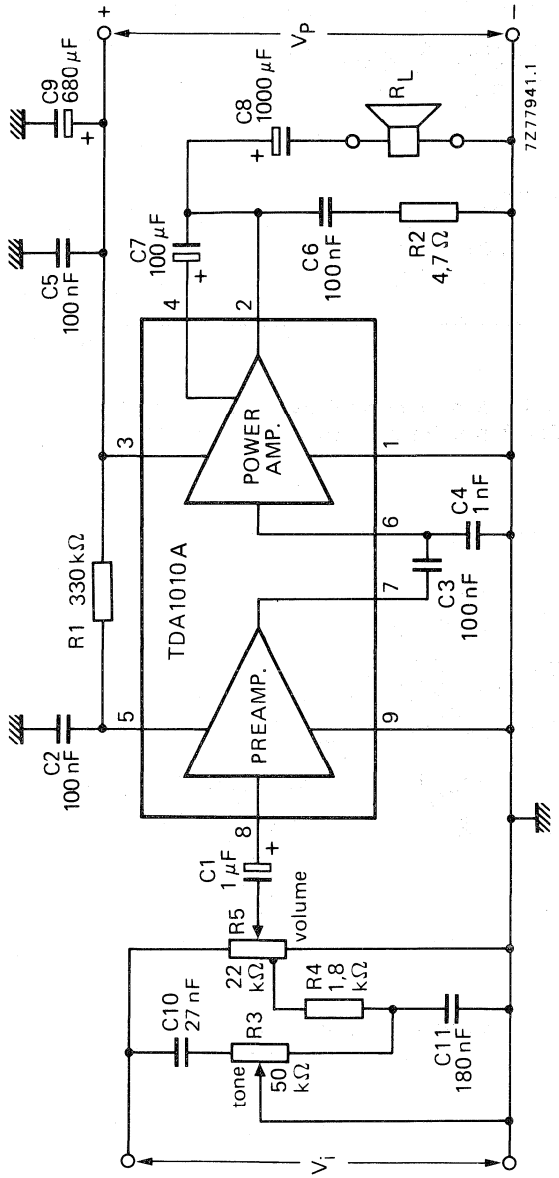


Fig. 9 Complete mono audio amplifier of a car radio.

APPLICATION INFORMATION

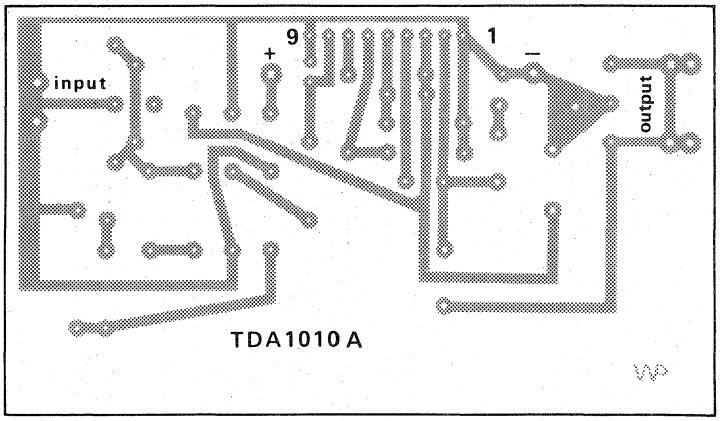


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

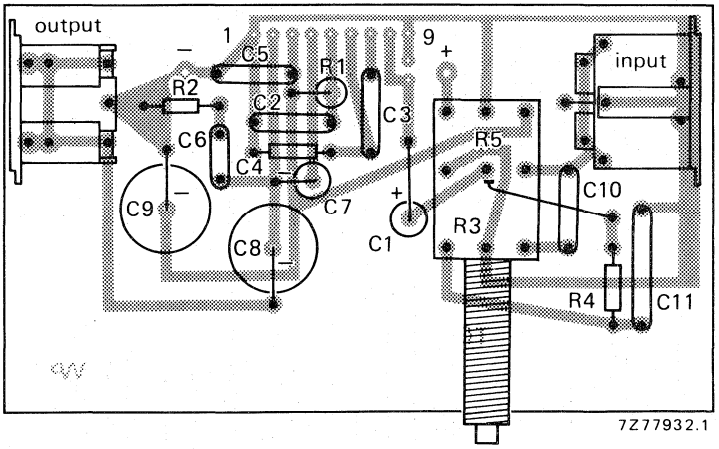


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

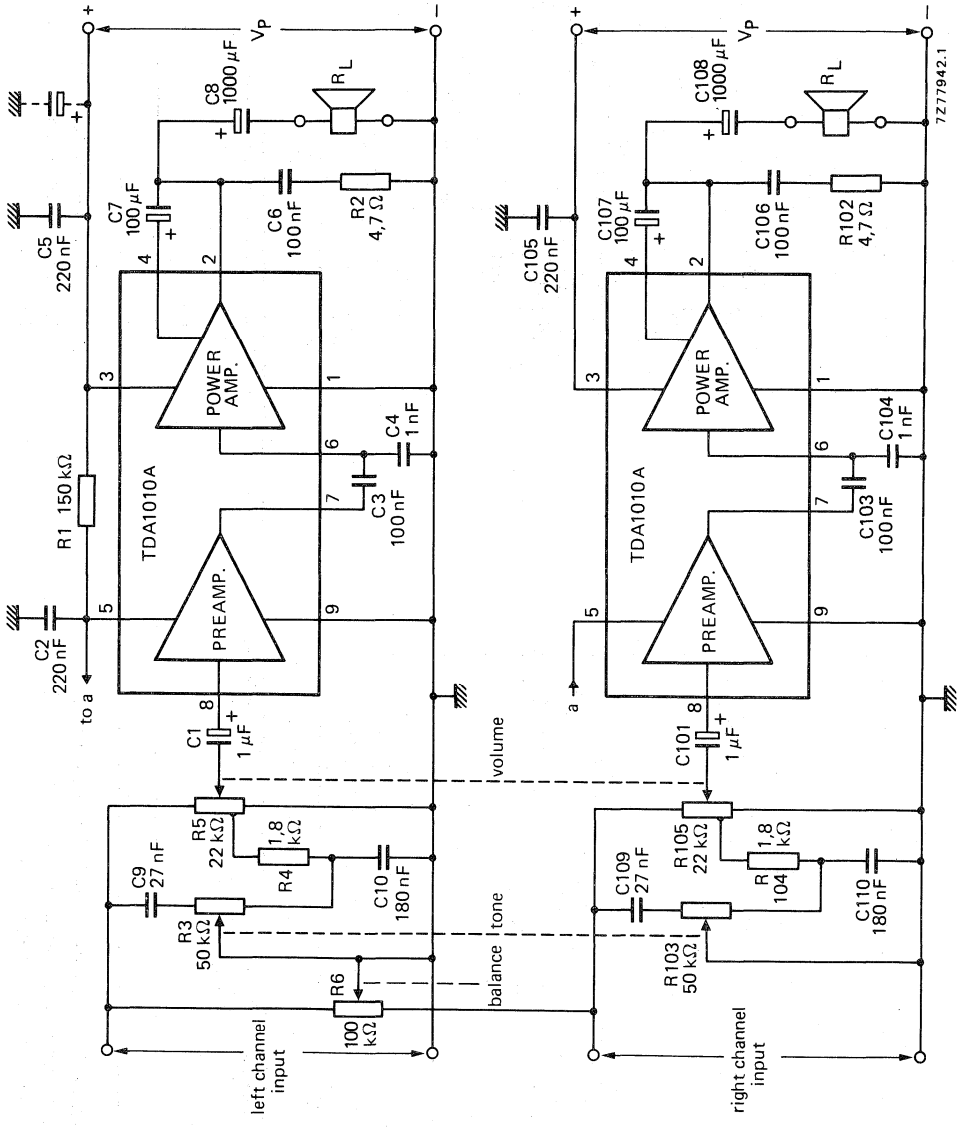


Fig. 12 Complete stereo car radio amplifier.

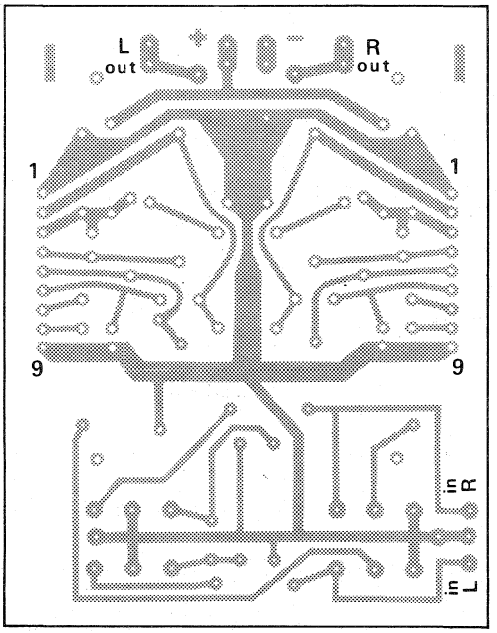


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

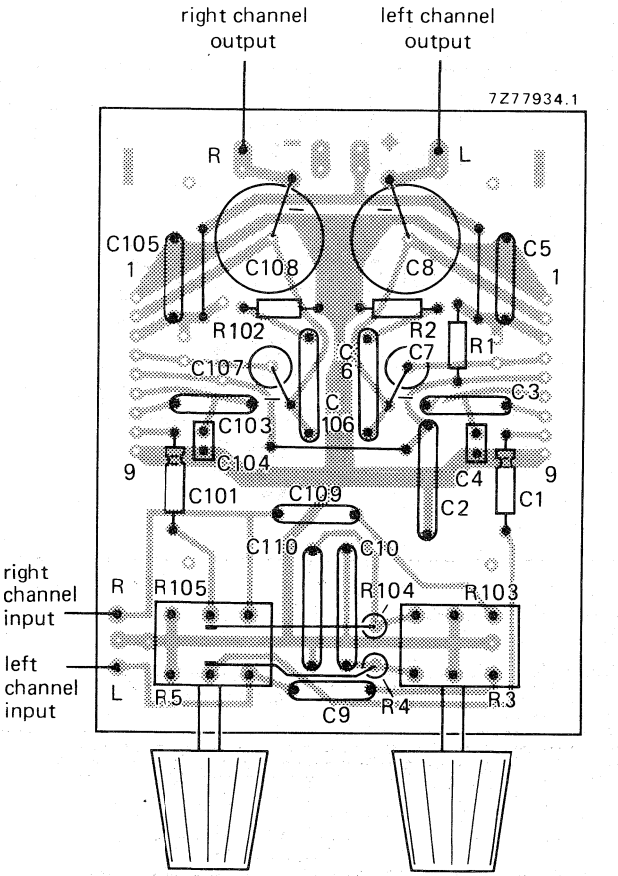


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

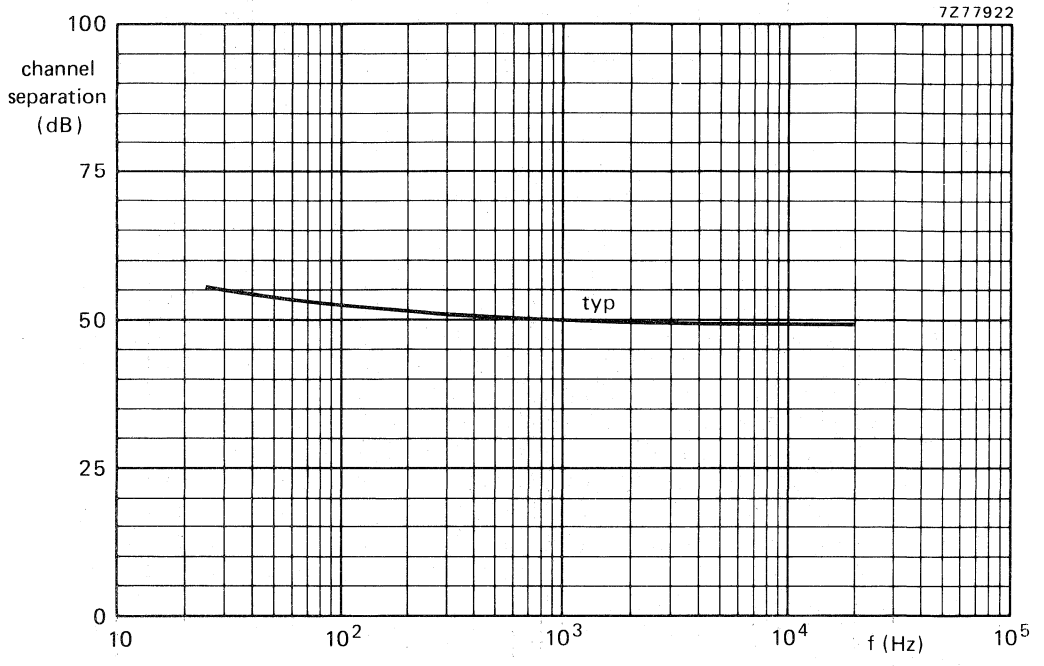


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

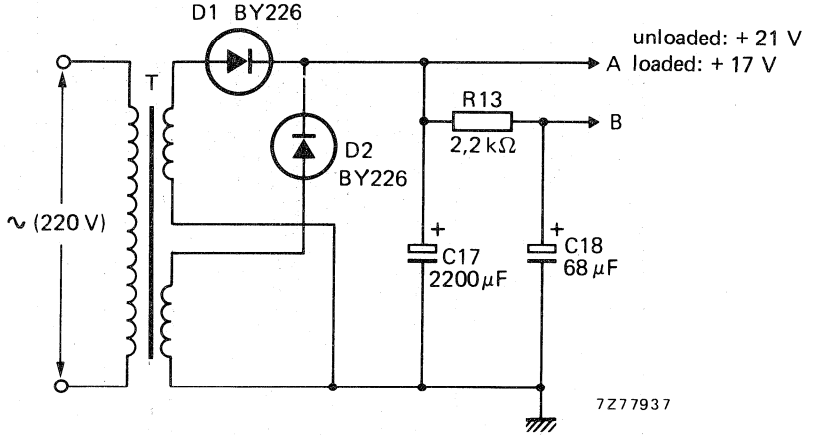


Fig. 16 Power supply of circuit of Fig. 17.

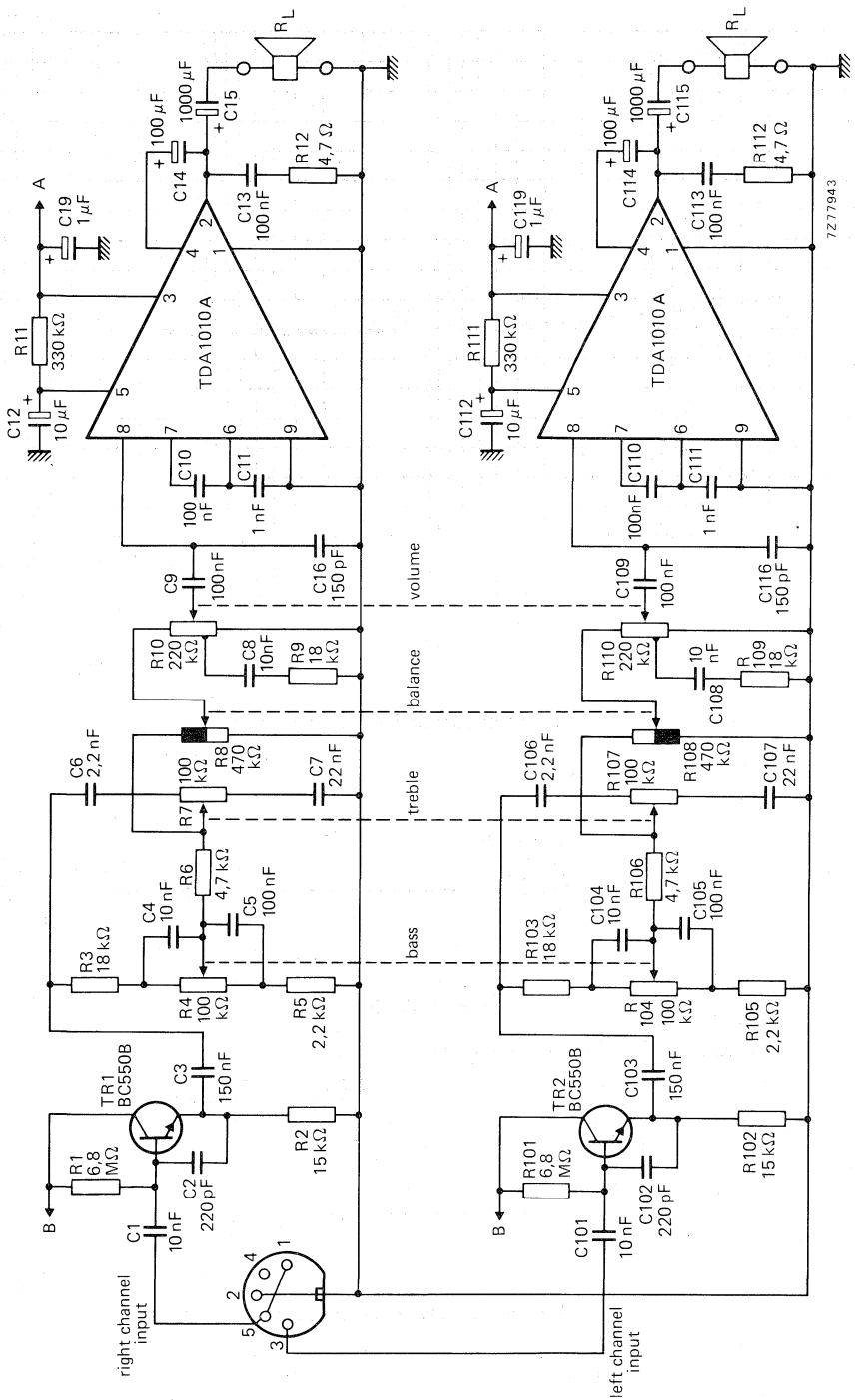


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

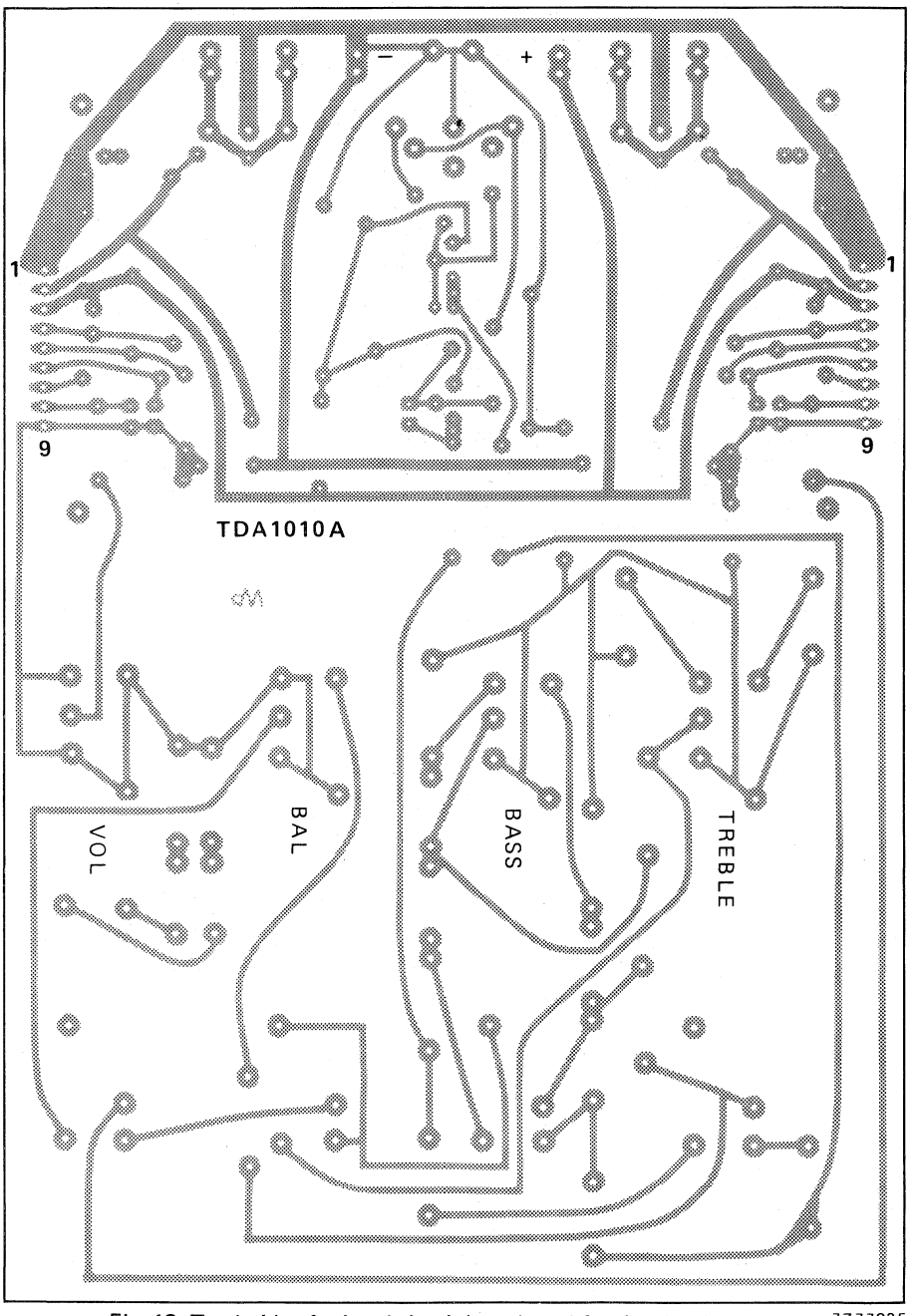


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

7Z77935

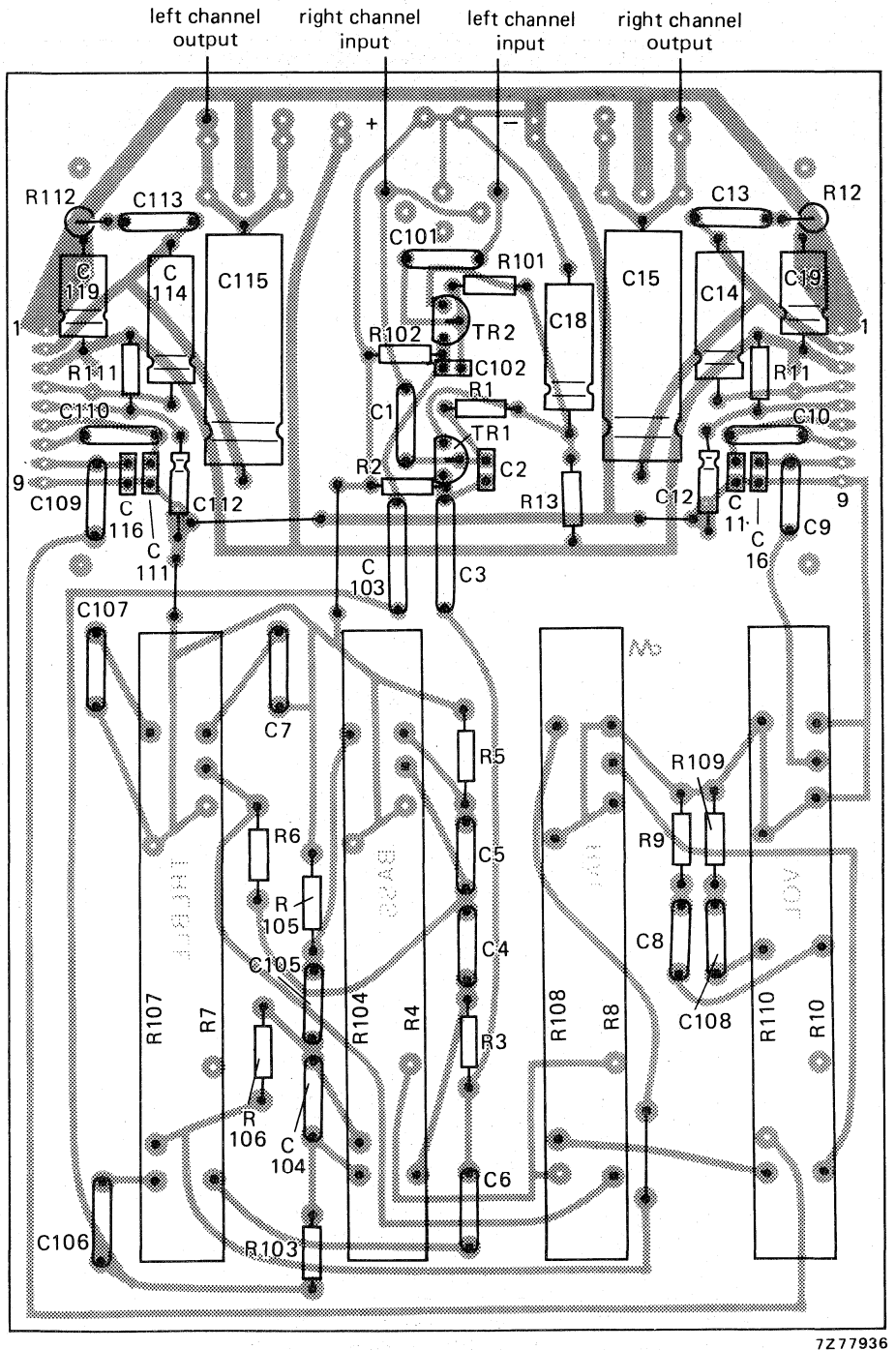


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

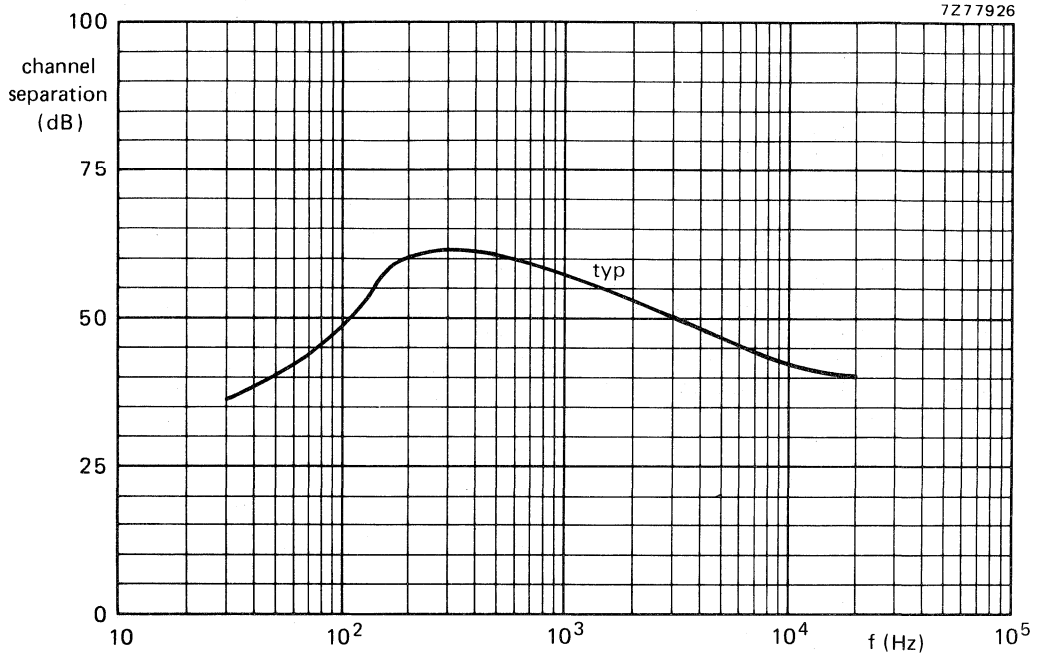


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 20	V
Peak output current	I_{OM}	max. 3	A
Output power at d_{tot} = 10%			
V_P = 16 V; R_L = 4 Ω	P_o	typ. 6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,2	%
Input impedance			
preamplifier (pin 8)	$\lvert Z_i \rvert$	> 100	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

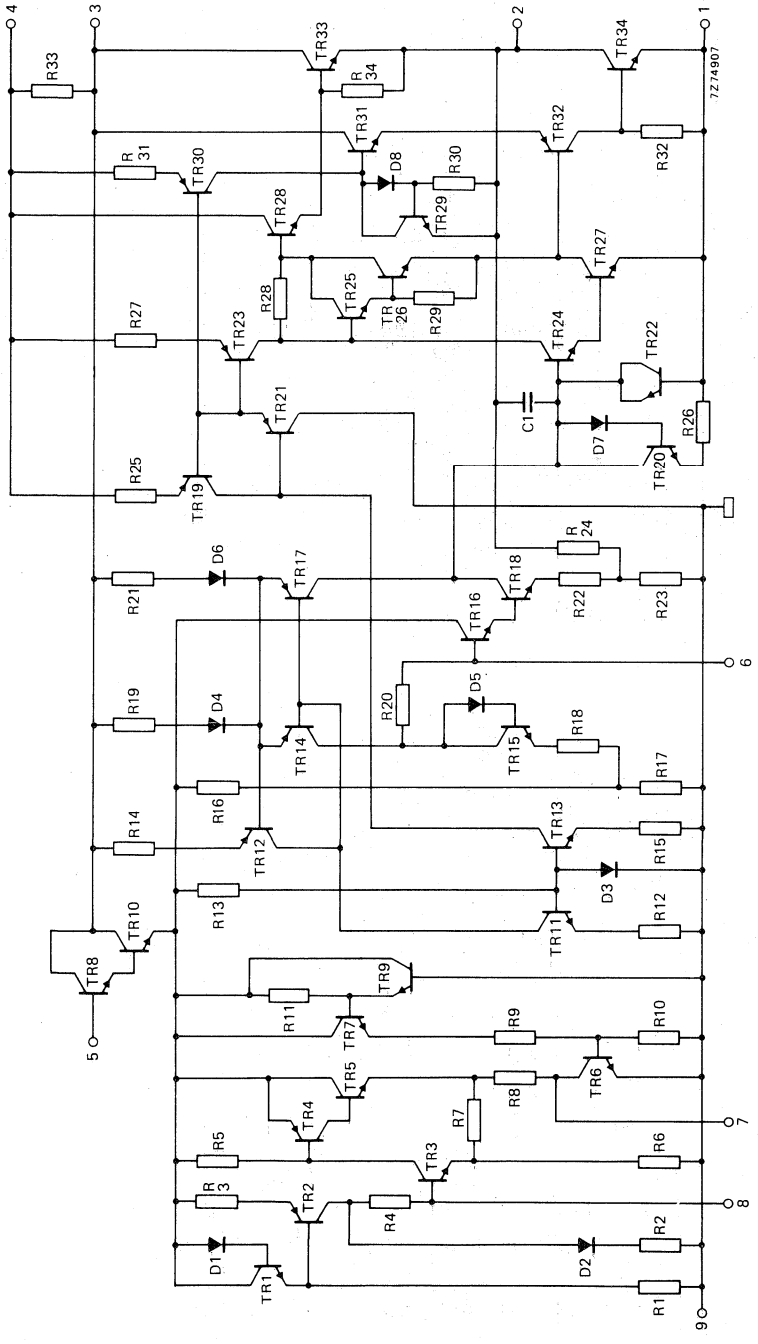


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

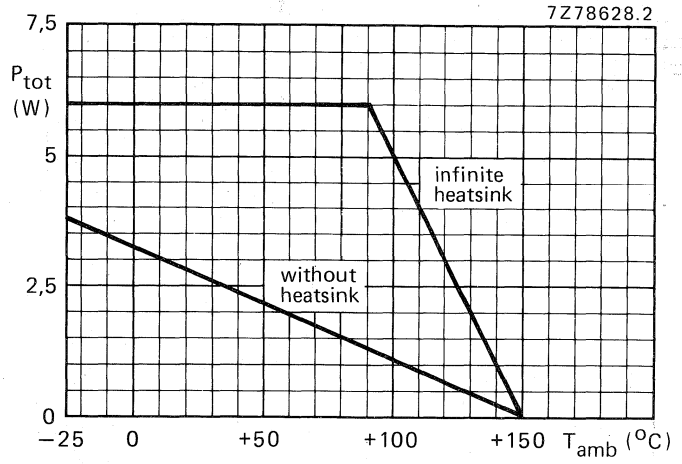


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{1,8} = 50\ K/W.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 50 − (10 + 1) = 39 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 20	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	>	3,6	W
		typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier	G_{v2}	typ.	29	dB
			27 to 31	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			50 to 54	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; −3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ.	20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,6	mV
		<	1,4	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

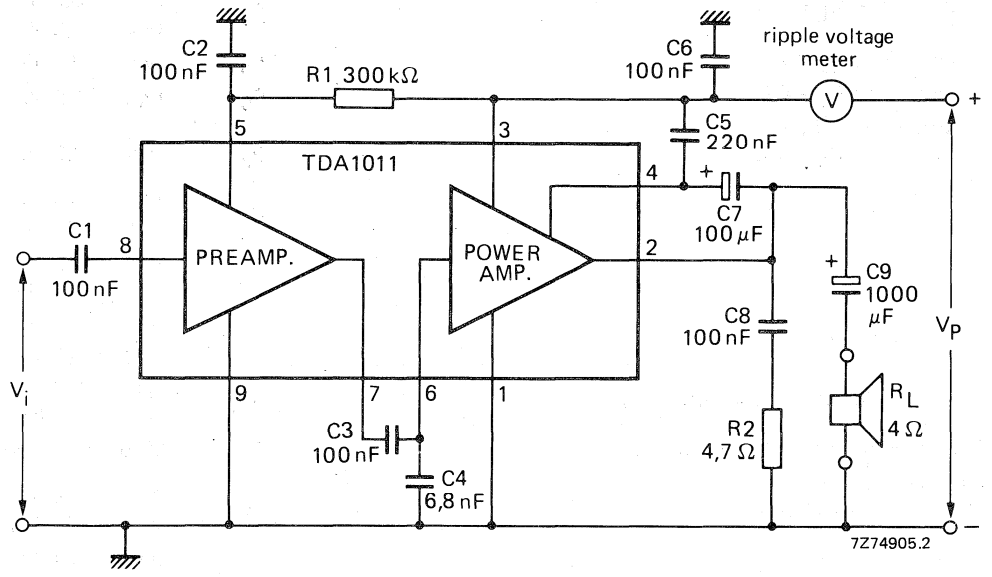


Fig. 3 Test circuit.

APPLICATION INFORMATION

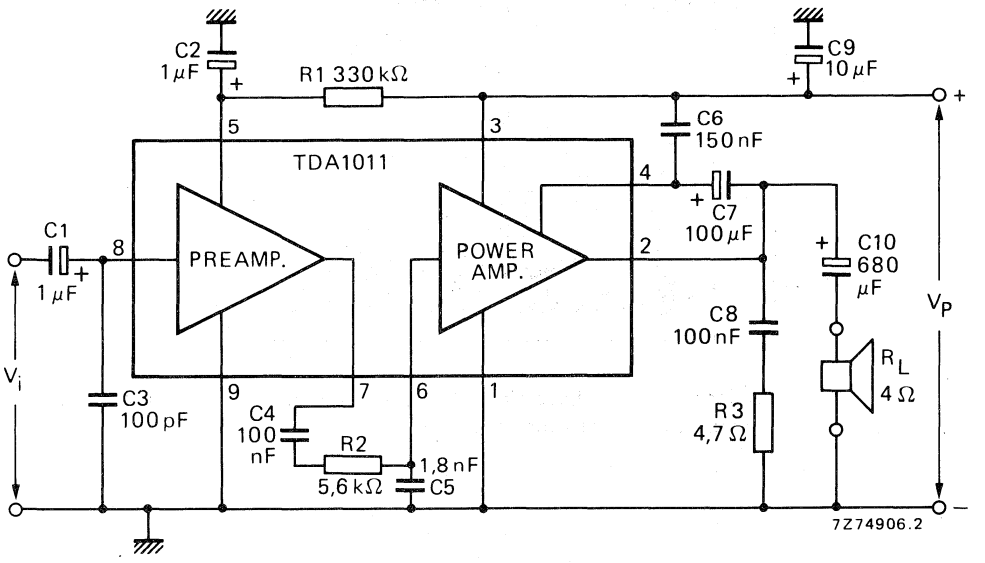


Fig. 4 Circuit diagram of a 4 W amplifier.

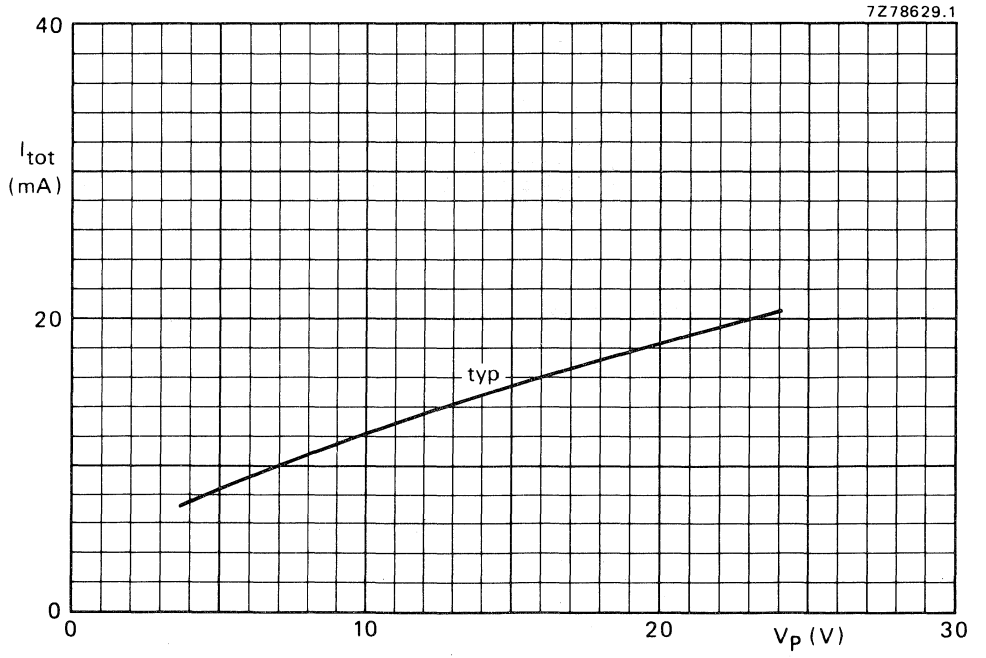


Fig. 5 Total quiescent current as a function of supply voltage.

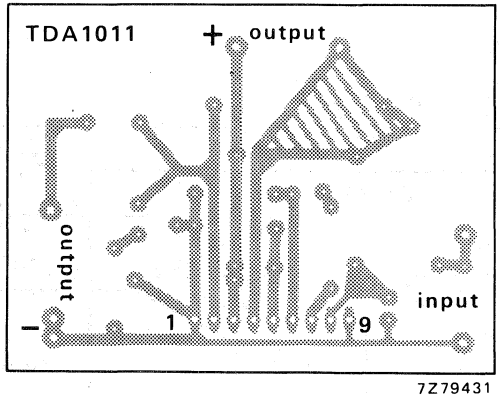


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.

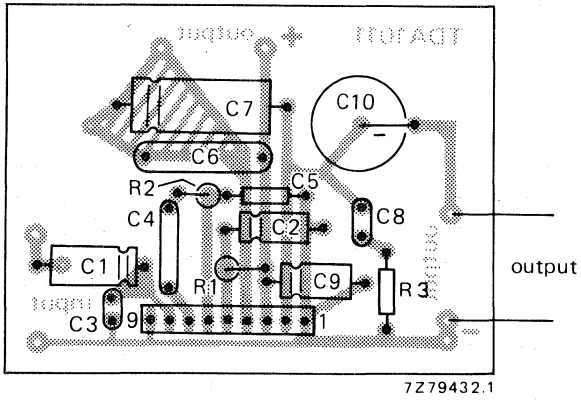


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

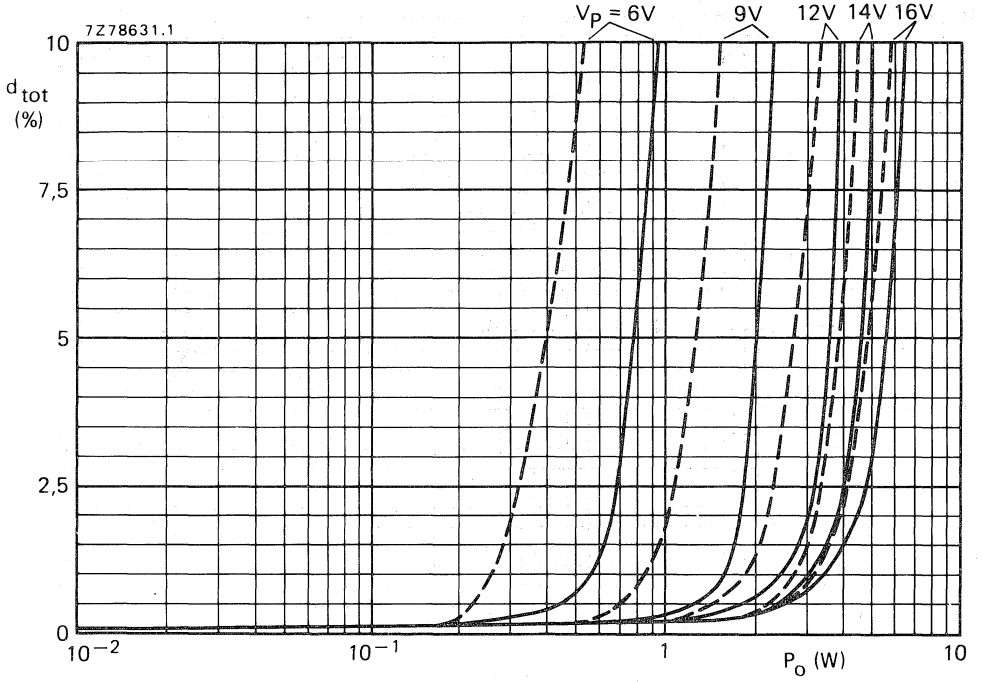


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

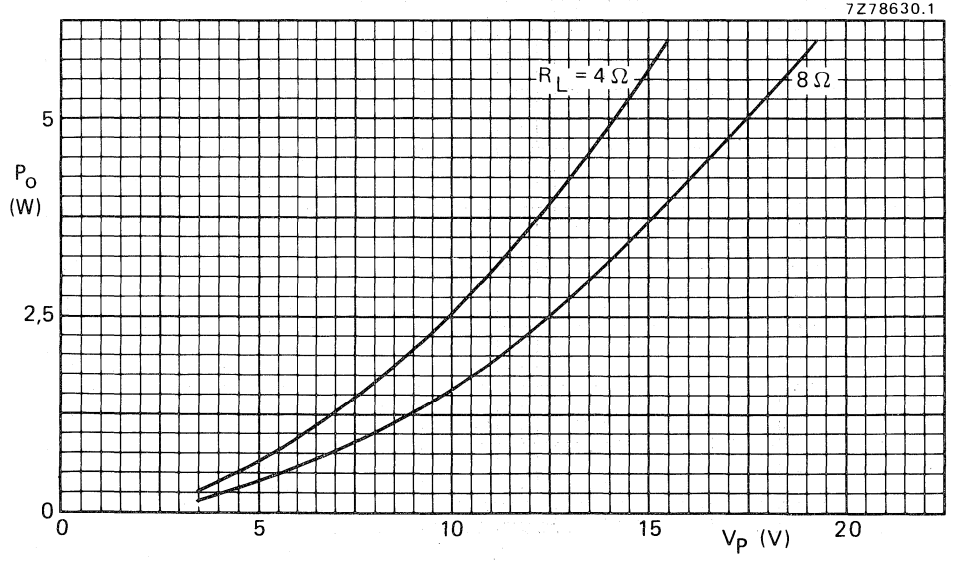


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

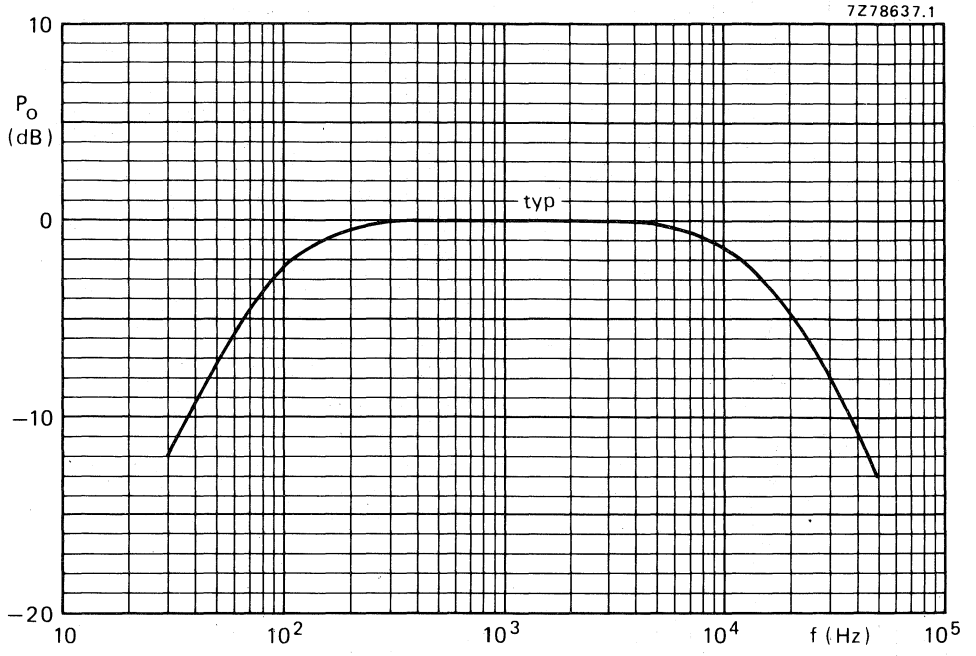


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

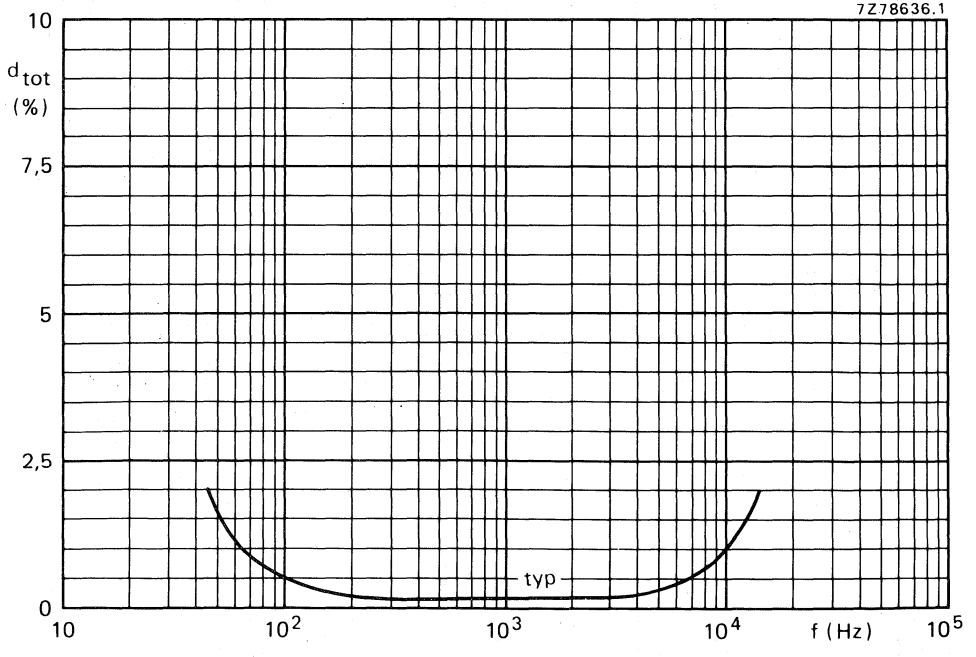


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

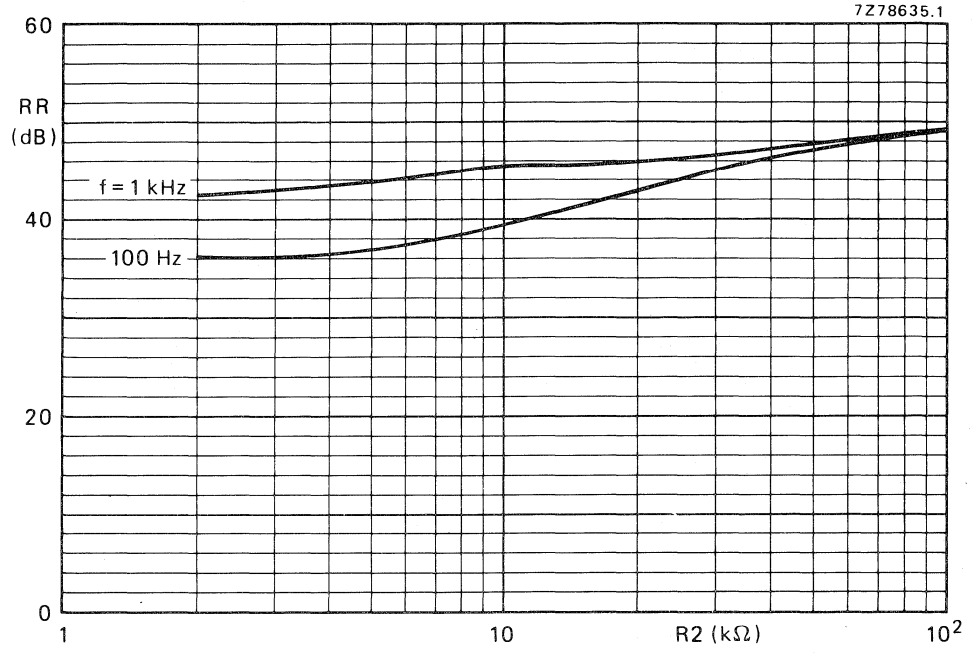


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

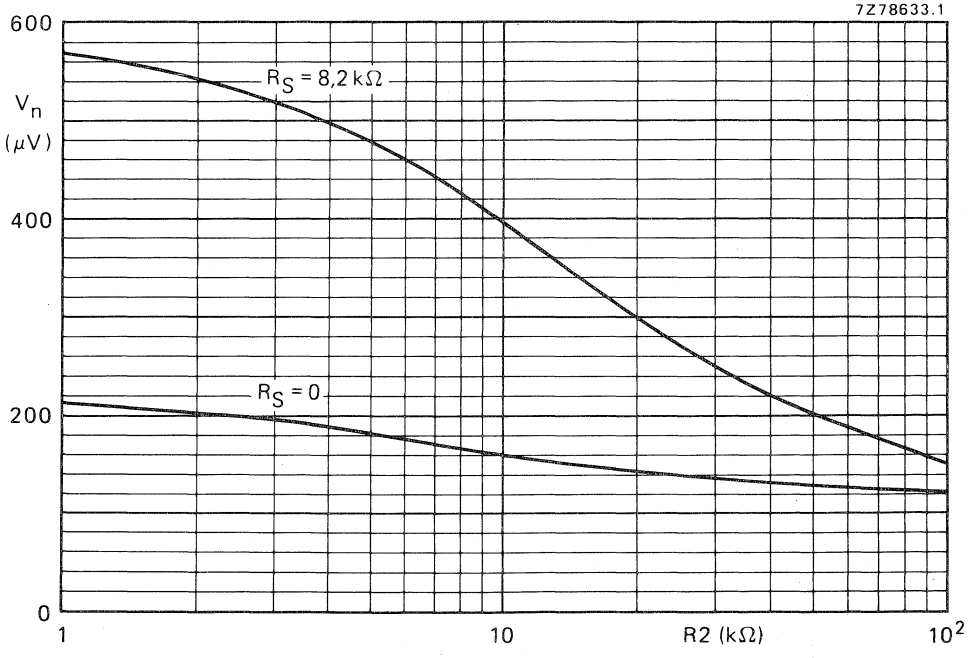


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

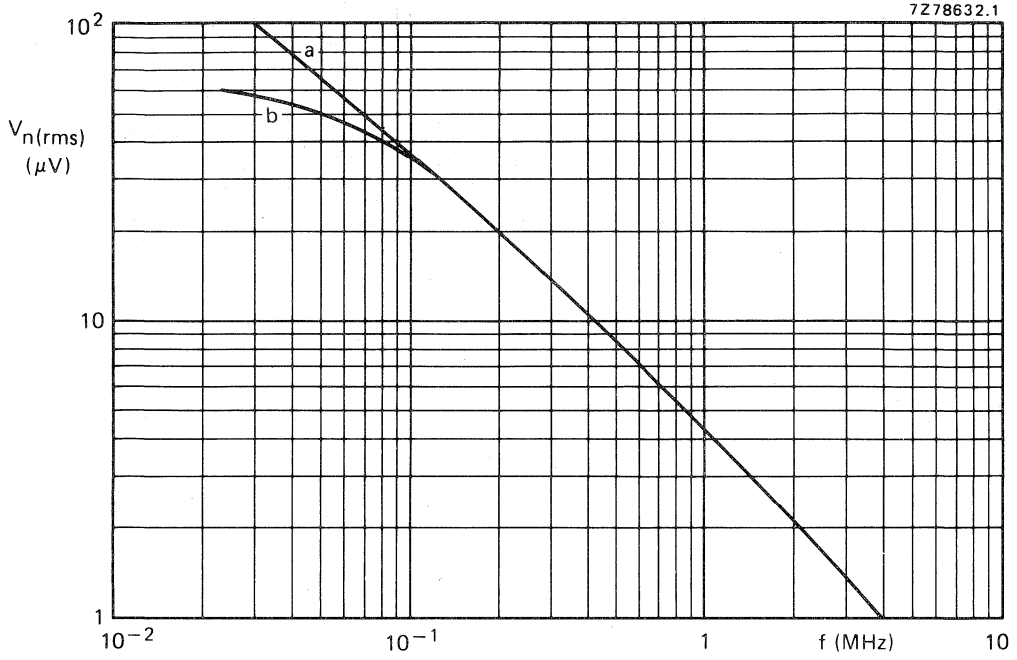


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

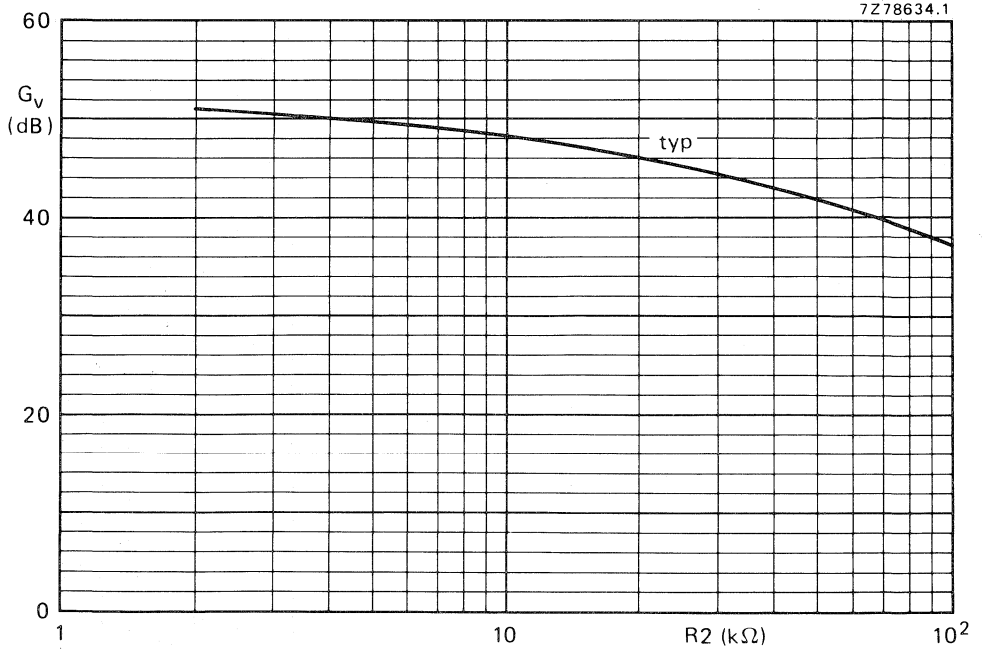


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

4 W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

GENERAL DESCRIPTION

The TDA1013B is an integrated audio amplifier circuit with DC volume control, encapsulated in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit ideal for applications in mains and battery-fed apparatus such as television receivers and record players.

The DC volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control is by means of a DC voltage variable between 2 and 6.5 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop. This device requires only a few external components and offers stability and performance.

Features

- Few external components
- Wide supply voltage range
- Wide control range
- Pin compatible with TDA1013A
- Fixed gain
- High signal-to-noise ratio
- Thermal protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_P	10	18	40	V
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	0.1	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
DC volume control unit						
Gain control range		$\lvert\Delta G_v\rvert$	80	–	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	45	55	mV
Input impedance (pin 8)		$\lvert Z_i\rvert$	23	29	35	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

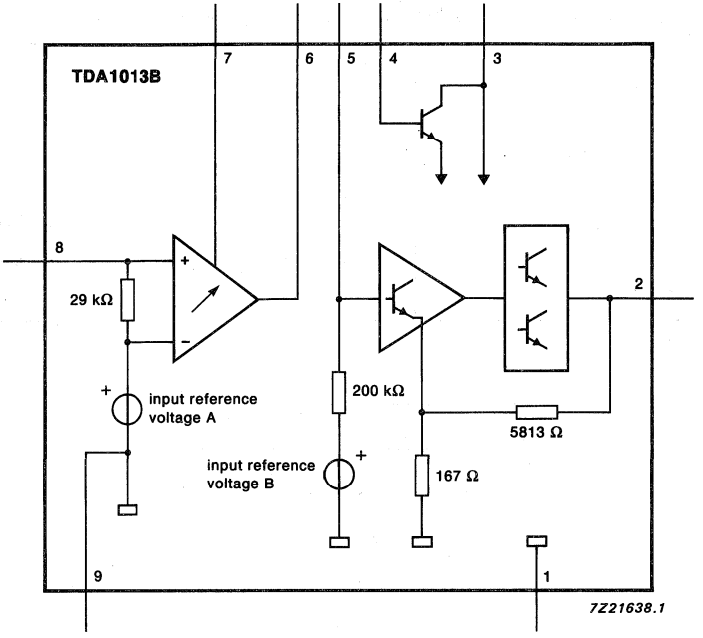


Fig.1 Block diagram.

PINNING

1 power ground
2 amplifier output
3 supply voltage
4 electronic filter
5 amplifier input
6 control unit output
7 control voltage
8 control unit input
9 signal ground

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	40	V
Non-repetitive peak output current	I_{OSM}	–	3	A
Repetitive peak output current	I_{ORM}	–	1.5	A
Storage temperature range	T_{stg}	–55	+ 150	°C
Crystal temperature	T_c	–	+ 150	°C
Total power dissipation	P_{tot}	see Fig. 2		

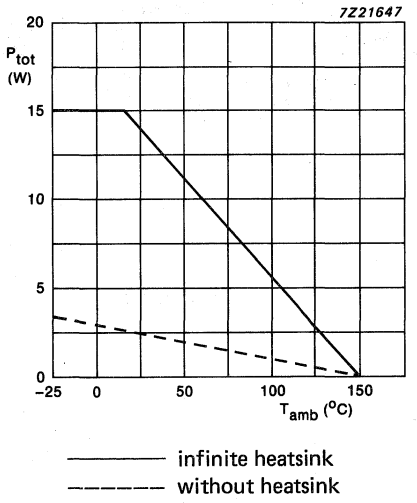


Fig.2 Power derating curve.

HEATSINK DESIGN EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C; T_c = 150 °C (max.); for a 4 W application, the maximum dissipation is approximately 2.5 W. The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} =$$

$$\frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2.5} = 36\ K/W$$

Since $R_{th\ j\text{-}tab}$ = 9 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (9 + 1) = 26 K/W.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; see Fig.10; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	10	18	40	V
Total quiescent current		I_{tot}	–	25	60	mA
Noise output voltage	note 1					
at maximum gain	R_S = 0 Ω	V_n	–	0.5	–	mV
at maximum gain	R_S = 5 kΩ	V_n	–	0.6	1.4	mV
at minimum gain	R_S = 0 Ω	V_n	–	0.25	–	mV
Total sensitivity	P_o = 2.5 W; DC control at max. gain	V_i	44	55	69	mV
Audio amplifier						
Repetitive peak output current		I_{ORM}	–	–	1.5	A
Output power	THD = 10%; R_L = 8 Ω	P_o	4.0	4.2	–	W
Total harmonic distortion	P_o = 2.5 W; R_L = 8 Ω	THD	–	0.15	1.0	%
Sensitivity	P_o = 2.5 W	V_i	100	125	160	mV
Input impedance (pin 5)		$\|Z_i\|$	100	200	500	kΩ
Power bandwidth		B_P	–	30 to 40 000	–	Hz
DC volume control unit						
Gain control range		$\|\Delta G_v\|$	80	90	–	dB
Signal handling	THD < 1%; DC control = 0 dB	V_i	1.2	1.7	–	V
Sensitivity (pin 6)	V_o = 125 mV; max. voltage gain	V_i	39	44	55	mV
Input impedance (pin 8)		$\|Z_i\|$	23	29	35	kΩ
Output impedance (pin 6)		$\|Z_o\|$	45	60	75	Ω

Note to the characteristics

1. Measured in a bandwidth in accordance with IEC 179, curve 'A'.

APPLICATION INFORMATION

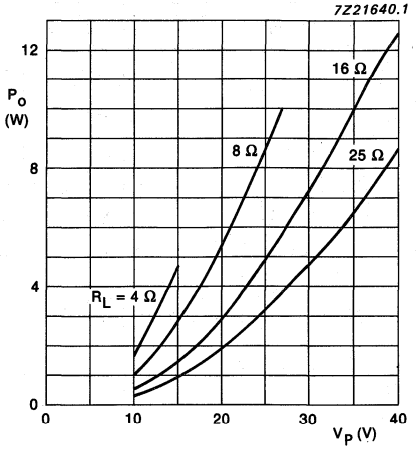


Fig.3 Output power as a function of supply voltage; f = 1 kHz; THD = 10% and control voltage (V_7) = 6.5 V.

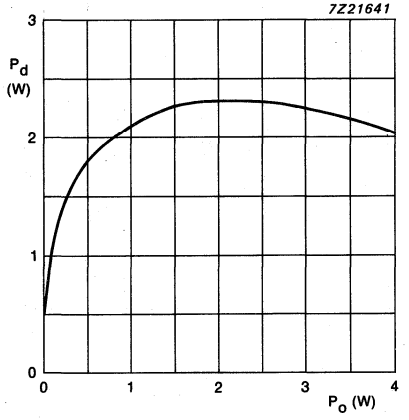


Fig.4 Power dissipation as a function of output power; V_P = 18 V; f = 1 kHz; R_L = 8 Ω and control voltage (V_7) = 6.5 V.

APPLICATION INFORMATION (continued)

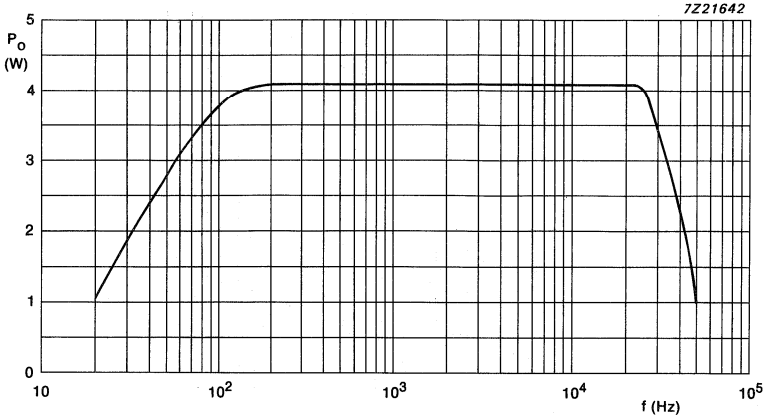


Fig.5 Power bandwidth; V_P = 18 V; R_L = 8 Ω; THD = 10% and control voltage (V_7) = 6.5 V.

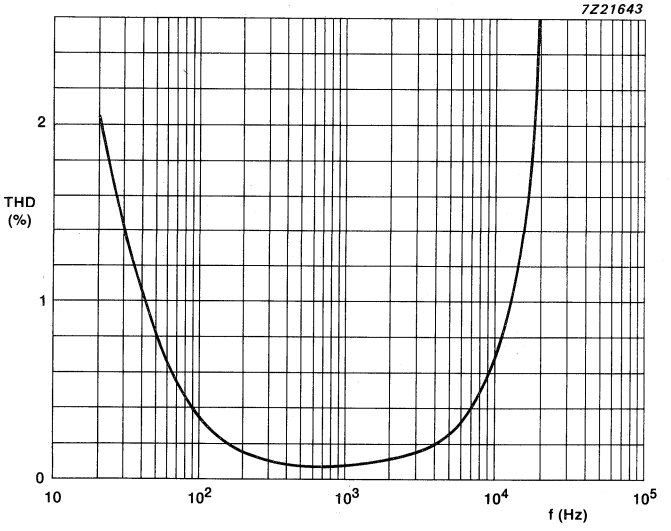


Fig.6 Total harmonic distortion as a function of frequency; V_P = 18 V; R_L = 8 Ω; P_o = 2.5 W and control voltage = 6.5 V.

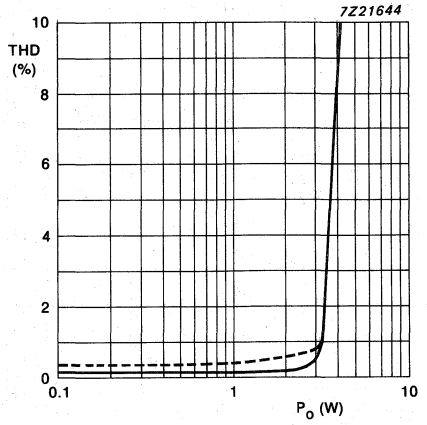


Fig.7 Total harmonic distortion as a function of output power; V_P = 18 V; R_L = 8 Ω and control voltage = 6.5 V.

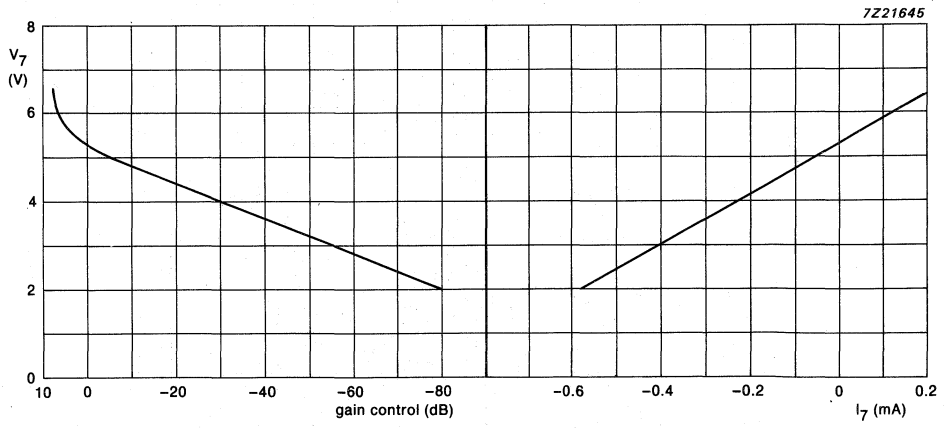


Fig.8 Typical control curve.

APPLICATION INFORMATION (continued)

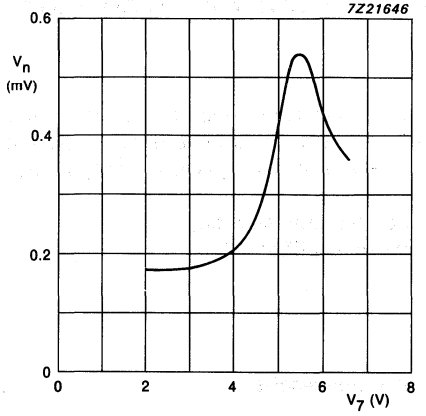
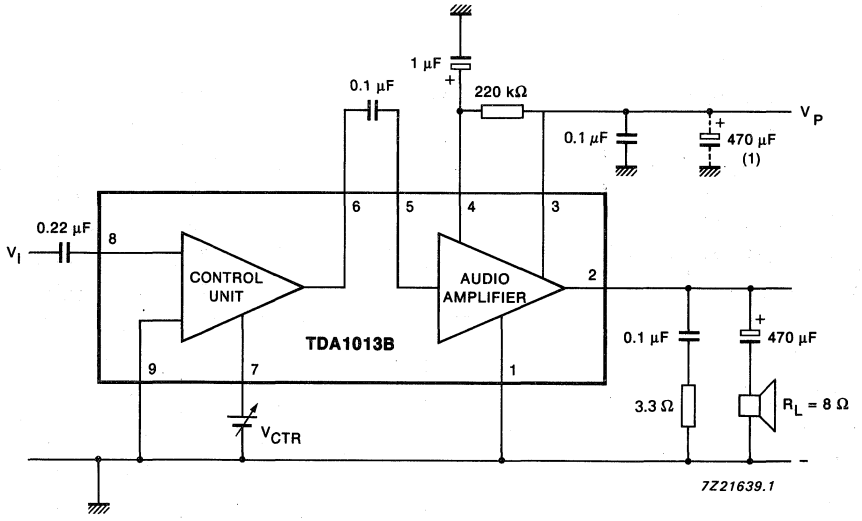


Fig.9 Noise output voltage as a function of the control voltage; V_P = 18 V; R_L = 8 Ω (in accordance with IEC 179, curve 'A').



(1) Belongs to power supply circuitry.

Fig.10 Application diagram.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 18	V
Peak output current	I_{OM}	max. 2,5	A
Output power at d_{tot} = 10%			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ. 0,3	%
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	> 100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ. 20	kΩ
Total quiescent current	I_{tot}	typ. 14	mA
Operating ambient temperature	T_{amb}	−25 to + 150	°C
Storage temperature	T_{stg}	−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT 110B).

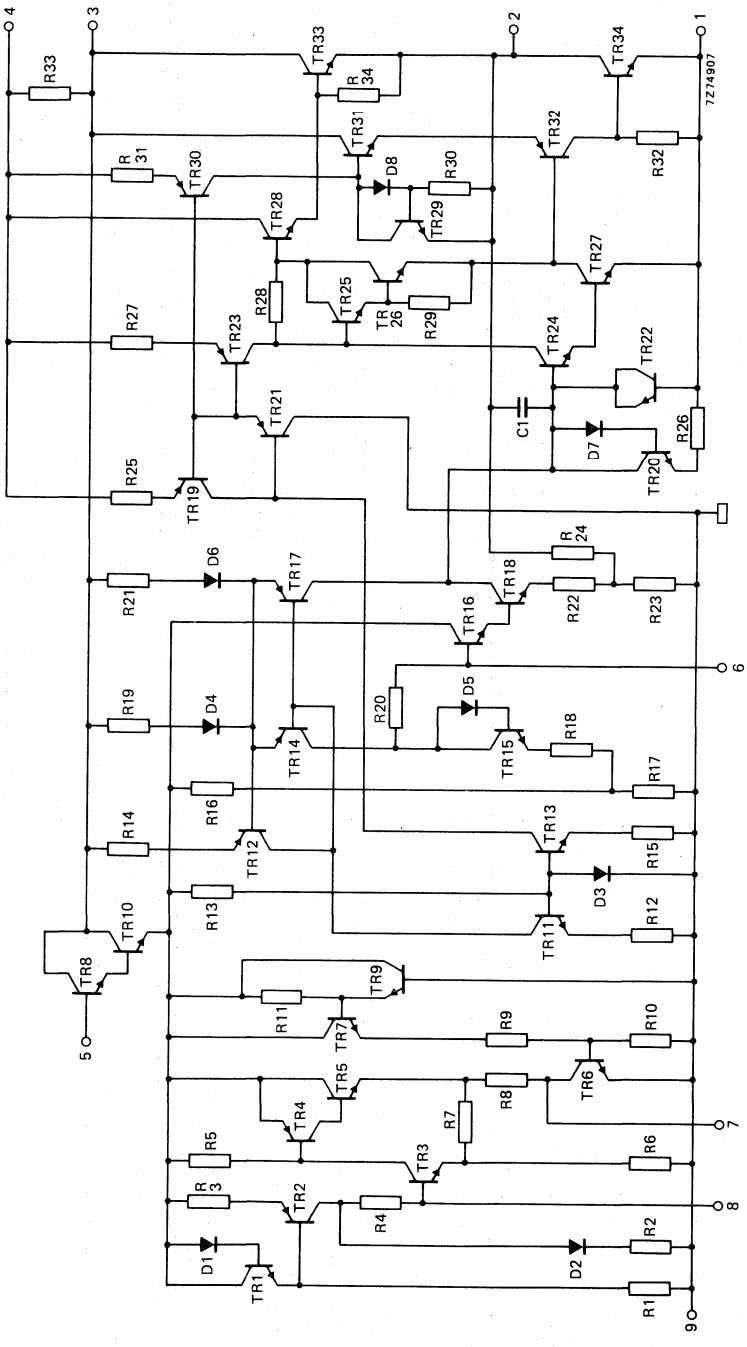


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

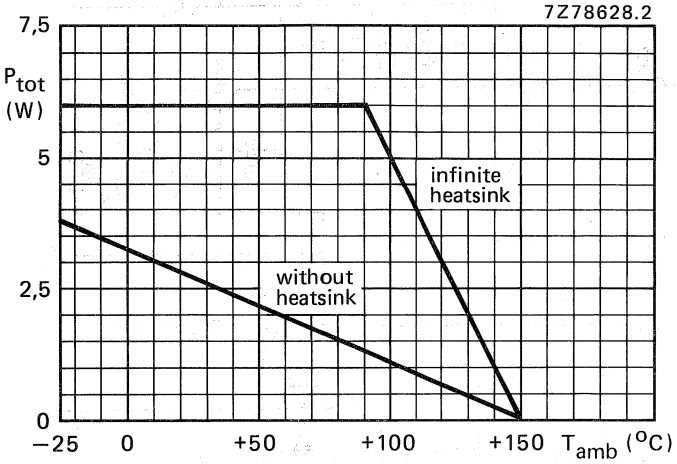


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 45}{1,8} = 58 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P	3,6 to 18	V
Repetitive peak output current	I_{ORM}	< 2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. 14 < 25	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1,0	W
without bootstrap:			
V_P = 12 V; R_L = 4 Ω	P_o	typ. 3,0	W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ. 23	dB
power amplifier	G_{v2}	typ. 29	dB
total amplifier	$G_{v\,tot}$	typ. 52 49 to 55	dB dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. 0,3 < 1,0	% %
Frequency response; −3 dB (note 3)	B	60 Hz to 15	kHz
Input impedance:			
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> 100 typ. 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ. 20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ. 1	kΩ
Output voltage preamplifier (r.m.s. value)			
d_{tot} < 1% (note 2)	$V_{o(rms)}$	typ. 0,8	V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ. 0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. 0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)			
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ. 8	μV
Ripple rejection (note 6)			
f = 100 Hz	RR	typ. 38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_O = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

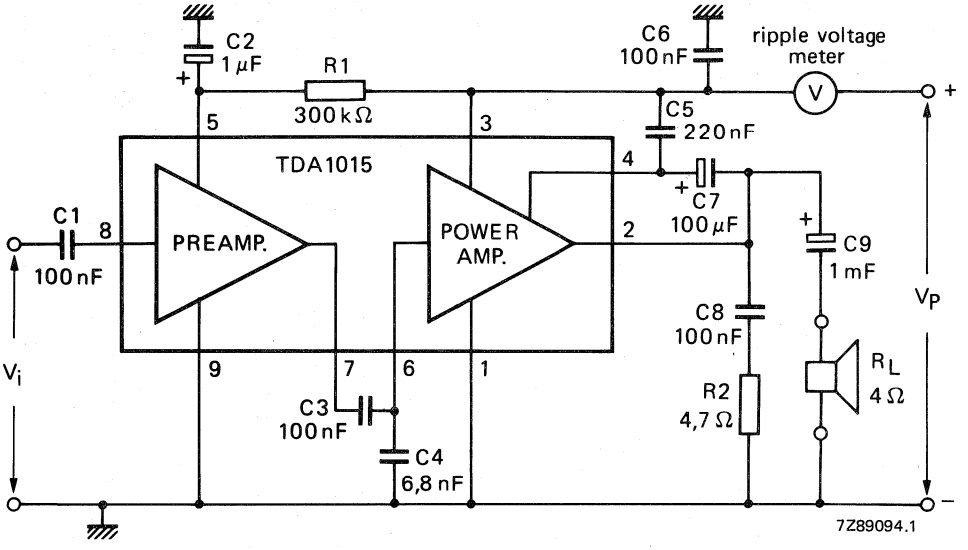


Fig. 3 Test circuit.

APPLICATION INFORMATION

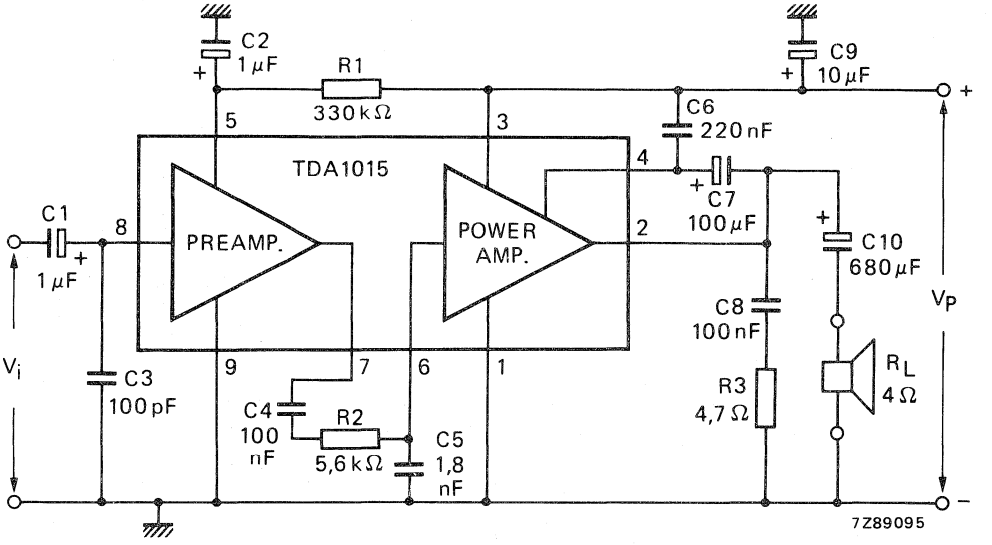


Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

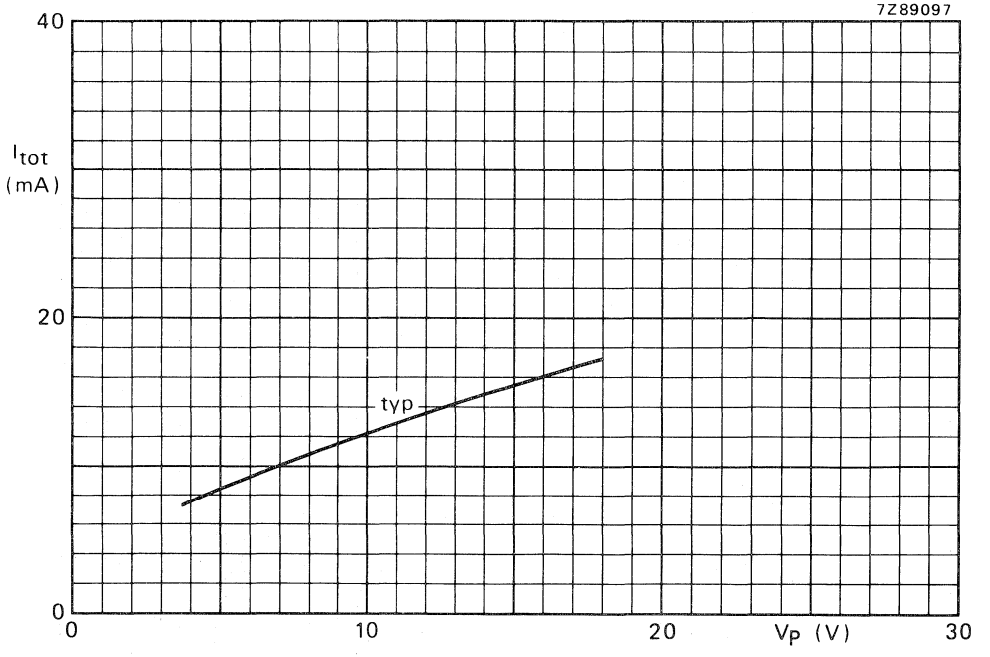


Fig. 5 Total quiescent current as a function of supply voltage.

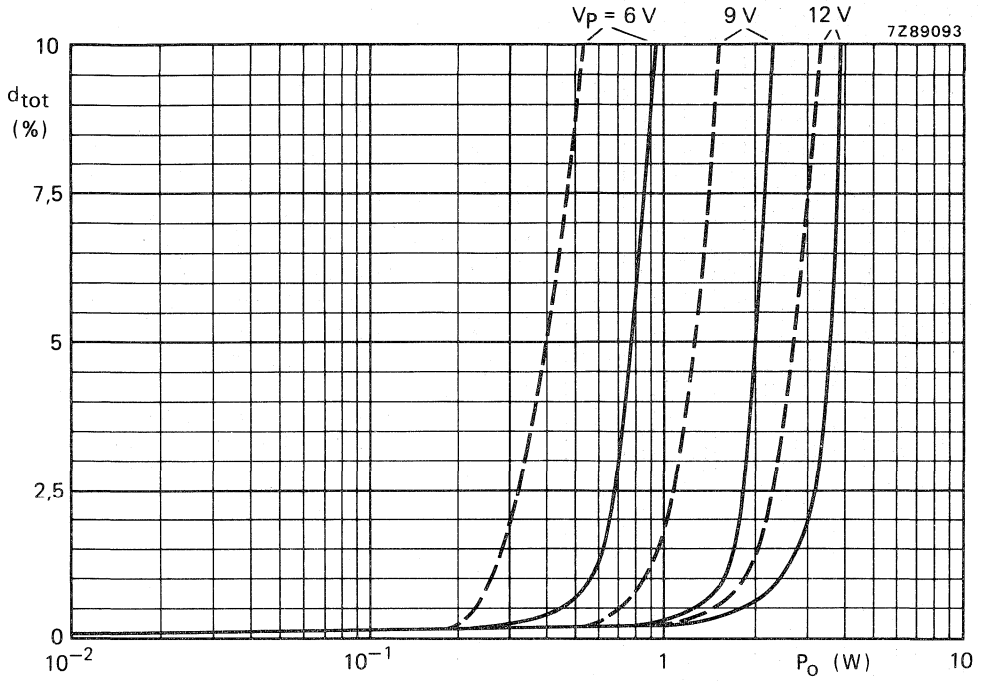


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

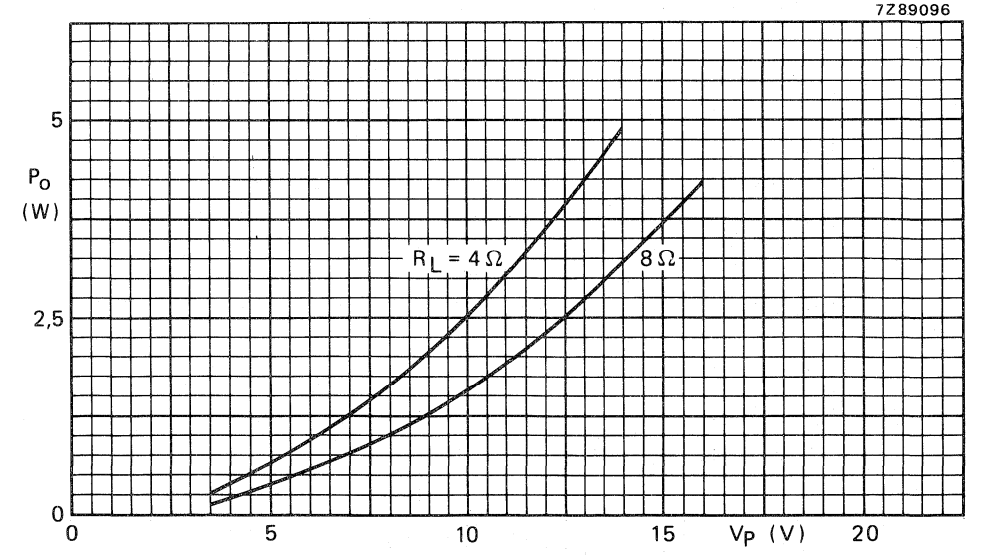


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

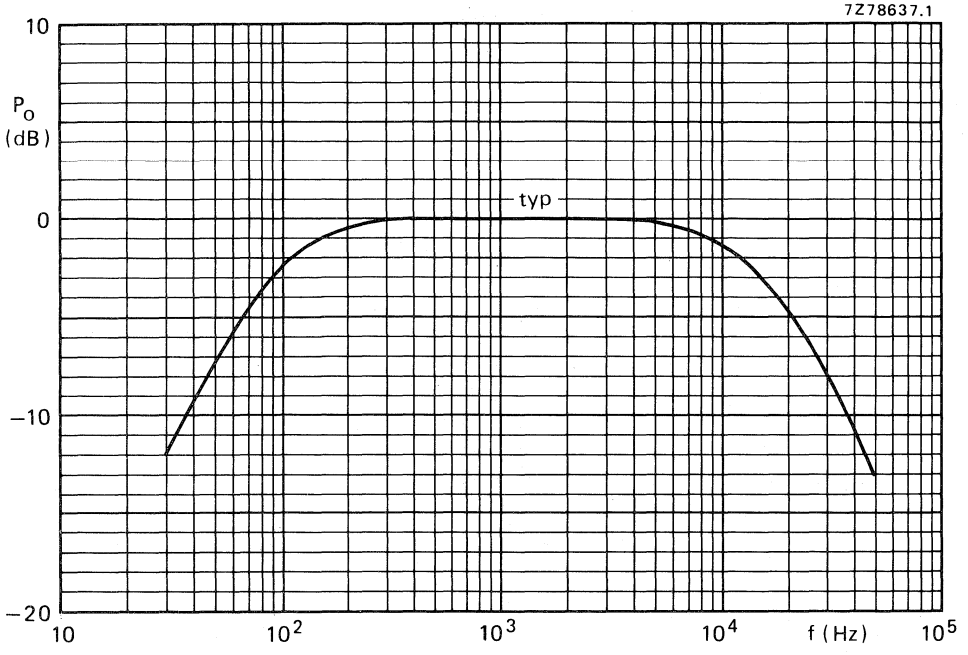


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

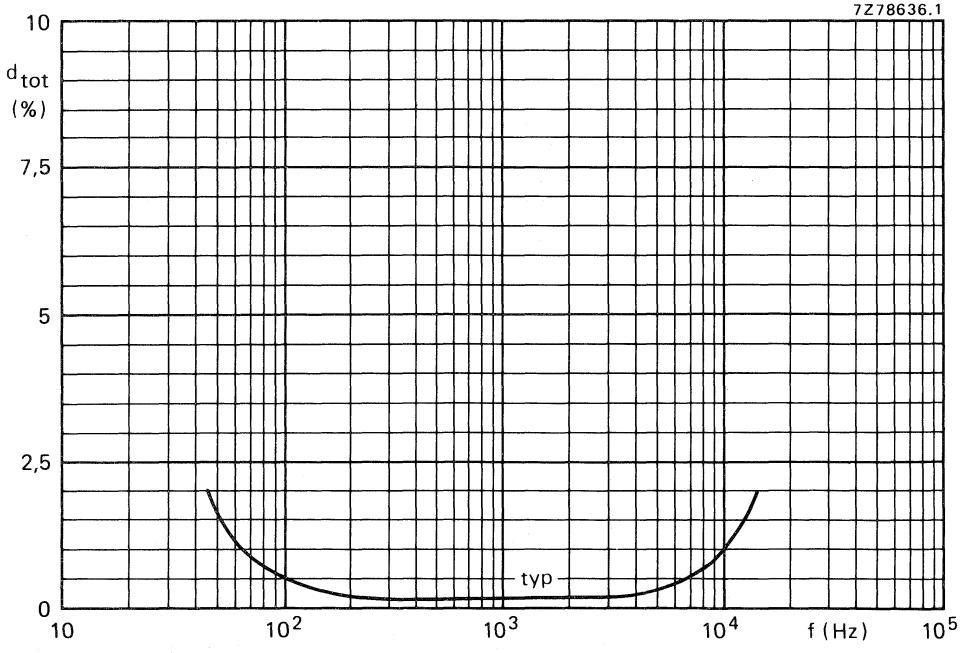


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

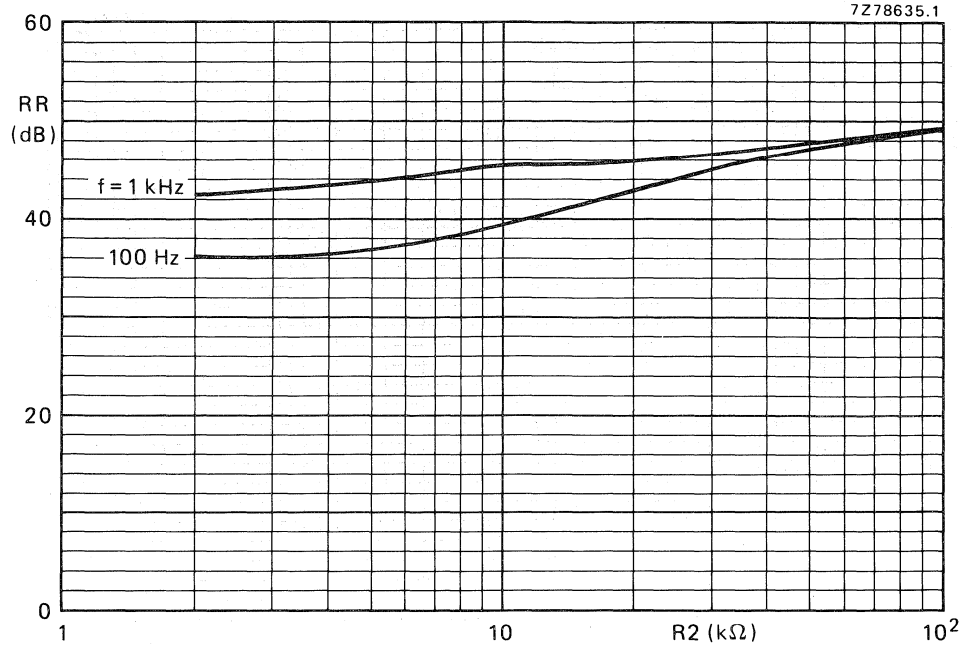


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

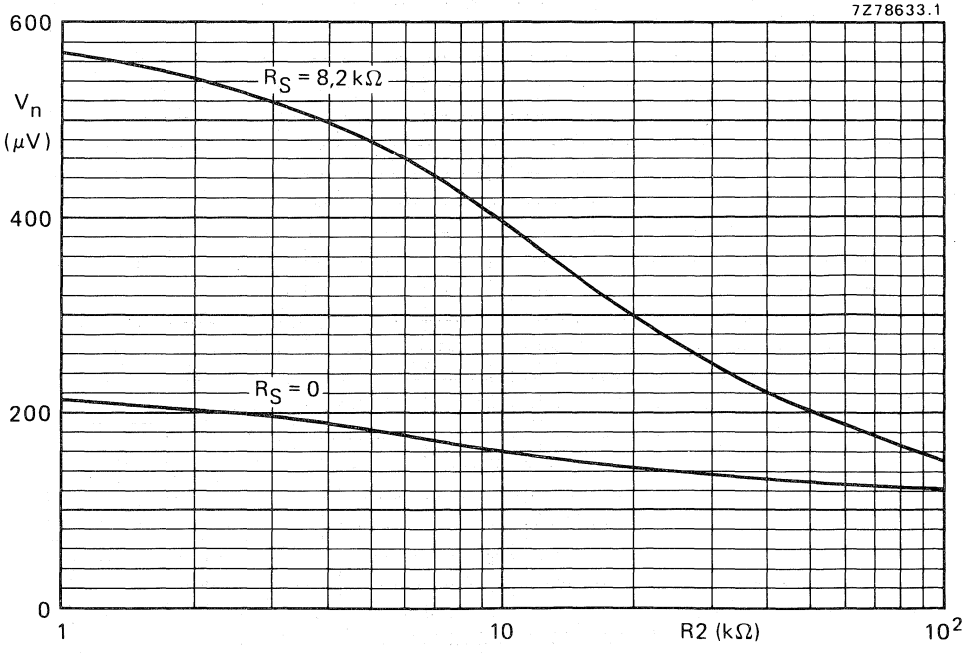


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

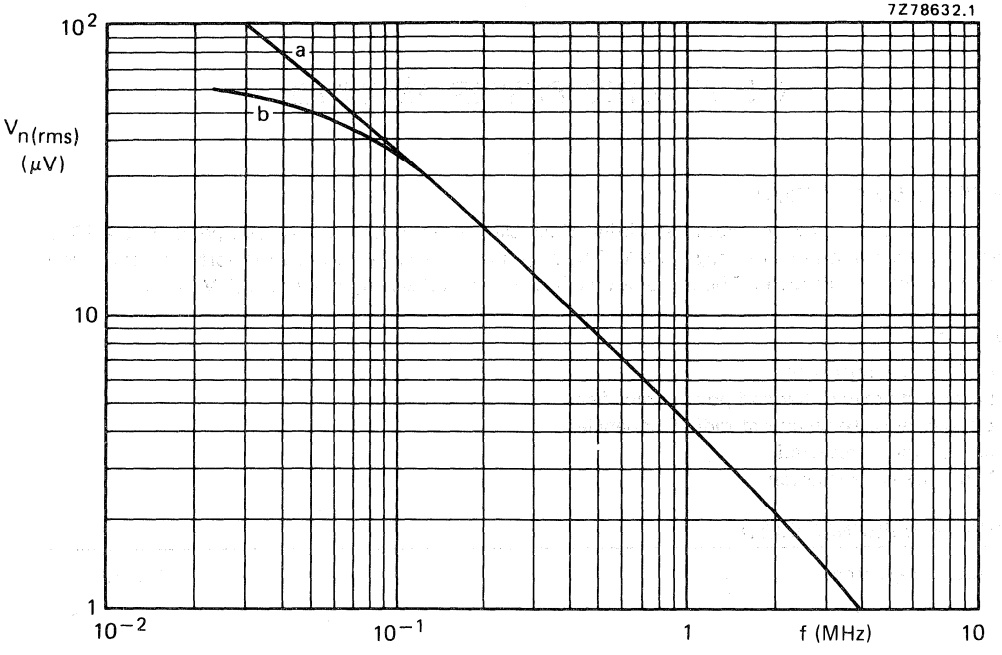


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

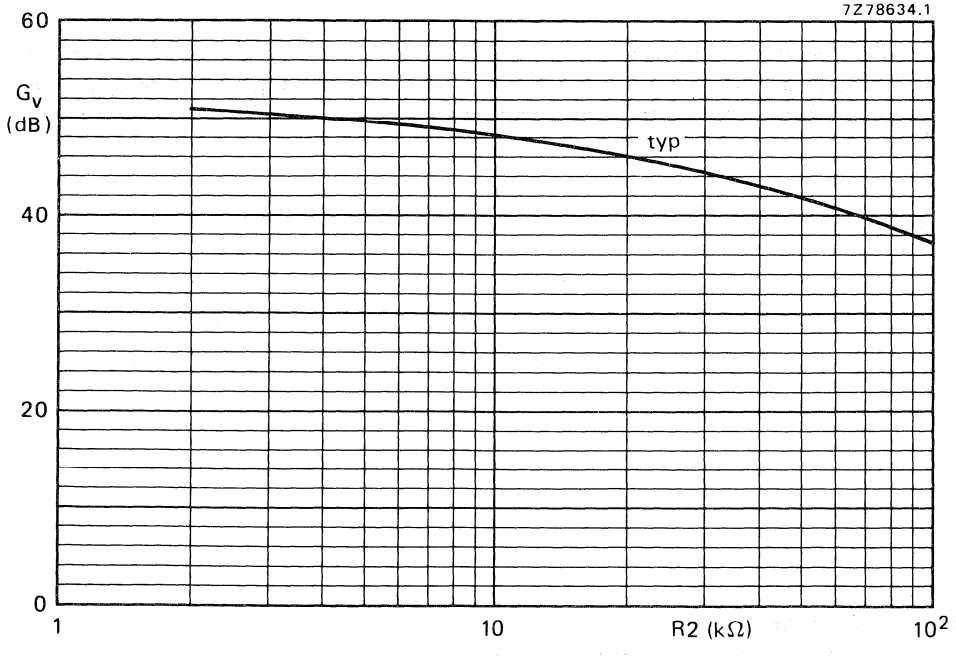


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

0,5 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1015T is a low-cost audio amplifier which can deliver up to 0,5 W output power into a 16 Ω load impedance at a supply voltage of 9 V. The amplifier is specially designed for portable applications such as radios and recorders. The IC has a very low supply voltage requirement (3,6 V min.).

Features

- High input impedance
- Separated preamplifier and power amplifier
- Limited noise behaviour at radio frequencies
- Short-circuit protected
- Miniature encapsulation

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 12	V
Peak output current	I_{OM}	max.	1	A
Output power	P_o	typ.	0,5	W
Voltage gain power amplifier	G_{v1}	typ.	29	dB
Voltage gain preamplifier	G_{v2}	typ.	23	dB
Total quiescent current	I_{tot}	max.	22	mA
Operating ambient temperature range	T_{amb}		−25 to +150	°C
Storage temperature range	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

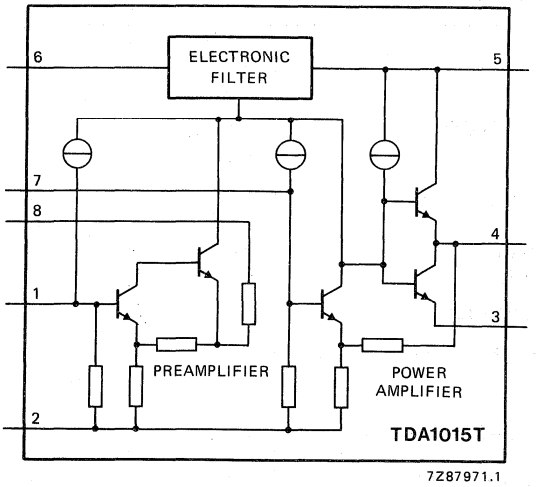


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	12 V
Peak output current	I_{OM}	max.	1 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range			−55 to +150 °C
A.C. short-circuit duration of load during sine-wave drive at V_P = 9 V	t_{sc}	max.	1 hour

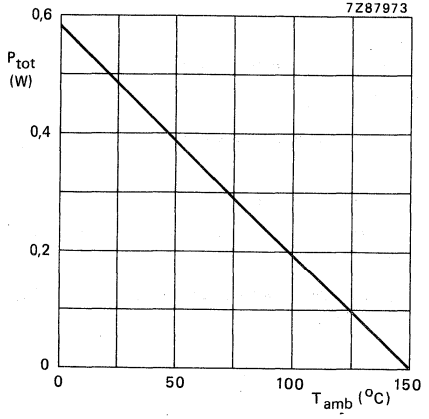


Fig. 2 Power derating curve.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V; R_L = 16 Ω; f = 1 kHz; see Fig. 3; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_P	3,6	9	12	V
Repetitive peak output current	I_{ORM}	–	–	1	A
Total quiescent current	I_{tot}	–	12	22	mA
A.F. output power at d_{tot} = 10% (note 1)					
V_P = 9 V; R_L = 16 Ω	P_o	–	0,5	–	W
V_P = 6 V; R_L = 8 Ω	P_o	–	0,3	–	W
Voltage gain power amplifier	G_{v1}	–	29	–	dB
Voltage gain preamplifier (note 2)	G_{v2}	–	23	–	dB
Total voltage gain	G_{tot}	49	52	55	dB
Frequency response at −3 dB (note 3)	B	–	60 to 15 000	–	Hz
Input impedance power amplifier	$\|Z_{i1}\|$	–	20	–	kΩ
Input impedance preamplifier (note 4)	$\|Z_{i2}\|$	100	200	–	kΩ
Output impedance preamplifier	$\|Z_{o2}\|$	0,5	1	1,5	kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (note 2)	$V_{o2(rms)}$	–	0,7	–	V
Noise output voltage (r.m.s. value) (note 5)					
R_S = 0 Ω	$V_{n(rms)}$	–	0,2	–	mV
R_S = 10 kΩ	$V_{n(rms)}$	–	0,5	–	mV
Noise output voltage (r.m.s. value) f = 500 kHz; B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	–	8	–	μV
Ripple rejection at f = 100 Hz; C2 = 1 μF (note 6)	RR	–	38	–	dB

Notes to the characteristics

1. Output power is measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistance of 20 kΩ.
3. The frequency response is mainly determined by the capacitors, C1, C3 (low frequency) and C4 (high frequency).
4. Independent of load impedance of preamplifier.
5. Effective unweighted r.m.s. noise voltage measured in a bandwidth from 60 Hz to 15 kHz (slopes 12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude of 2 V).

APPLICATION INFORMATION

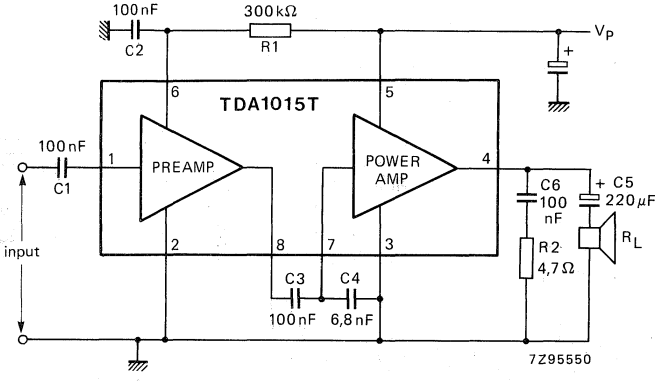


Fig. 3 Test circuit.

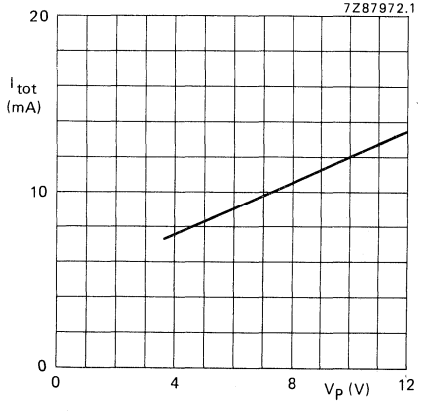


Fig. 4 Total quiescent current as a function of supply voltage.

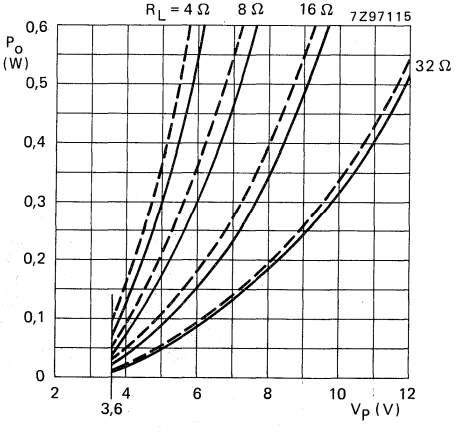


Fig. 5 Output power as a function of supply voltage; d_{tot} = 10%; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

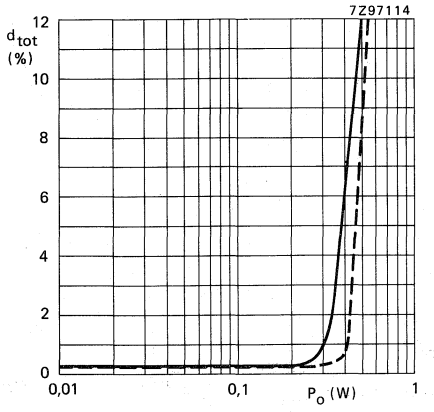


Fig. 6 Total distortion as a function of output power; V_P = 9 V; R_L = 16 Ω; f = 1 kHz.
——— measured in Fig. 3
– – – – – measured with a 1,5 MΩ resistor connected between pins 7 and 2.

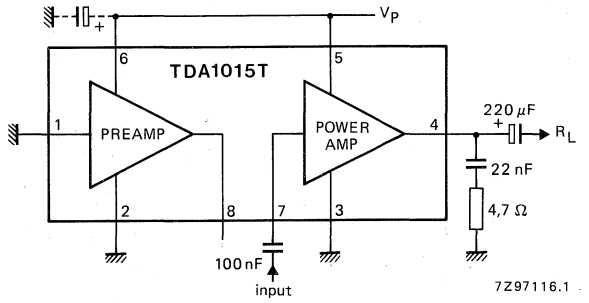


Fig. 7 Application circuit for power stage only and battery power supply; G_{v1} = 29 dB; $|Z_{i1}|$ = 20 kΩ.

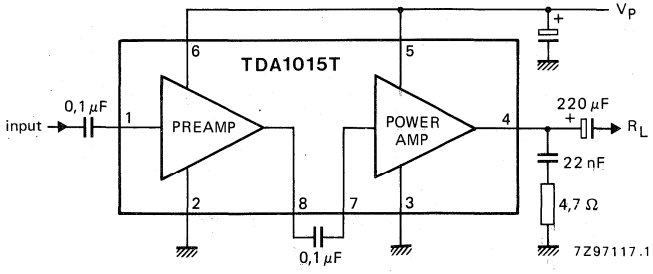


Fig. 8 Application circuit for preamplifier and power amplifier stages and battery power supply; $G_{v\,tot}$ = 52 dB; $|Z_{i2}|$ = 200 kΩ.

RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

Features

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

QUICK REFERENCE DATA

Supply voltage range	V_P	3,6 to 15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	typ. 10	mA
Operating ambient temperature range	T_{amb}	−25 to 150	°C
Power amplifier			
Output power at d_{tot} = 10%			
V_P = 6 V; R_L = 4 Ω	P_o	typ. 1	W
V_P = 9 V; R_L = 4 Ω	P_o	typ. 2	W
Closed loop gain	G_c	typ. 36	dB
Preamplifier			
Open loop gain	G_o	min. 70	dB
Minimum closed loop voltage gain	$G_{c\,min}$	min. 35	dB
Output voltage at d_{tot} = 1%	V_o	min. 1	V
Automatic Level Control (A.L.C.)			
Gain variation for ΔV_i = 40 dB	ΔG_v	typ. 2	dB
Stabilized supply voltage			
Output voltage	$V_{5\text{-}16}$	typ. 2,6	V

PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT38).

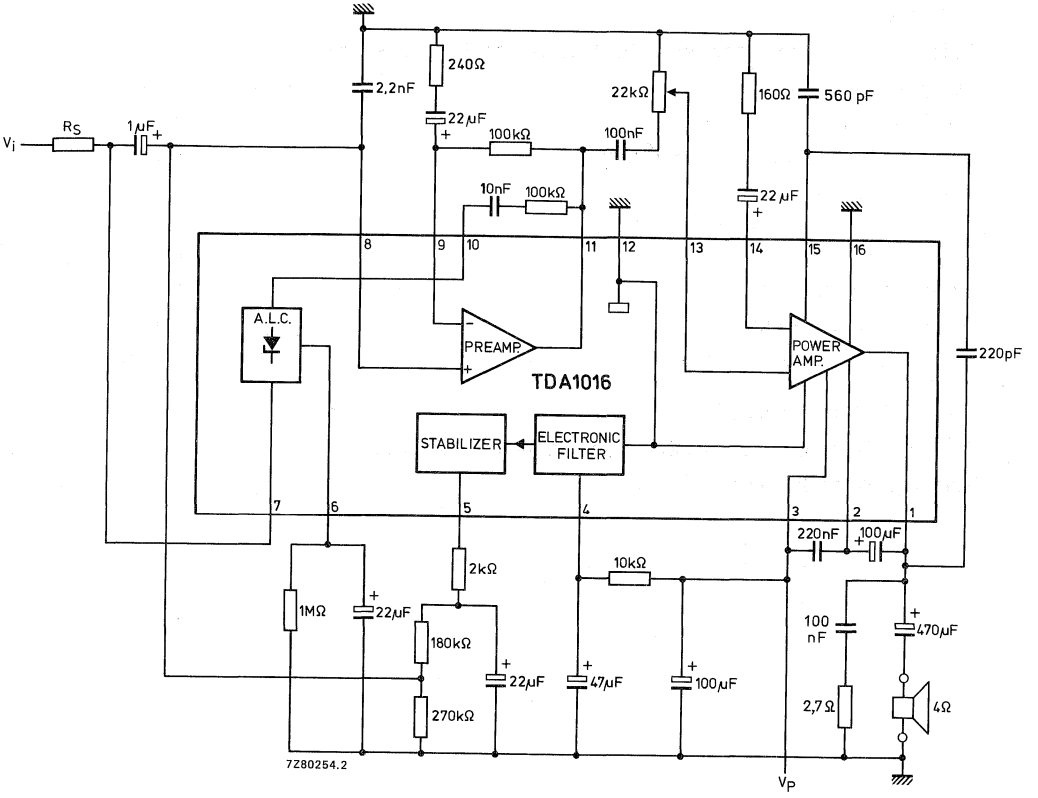


Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	V_P	max.	18	V
Repetitive peak output current	I_{ORM}	max.	1	A
Non-repetitive peak output current (pin 1)	I_{OSM}	max.	2	A
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sinewave drive; V_P = 12 V	t_{sc}	max.	100	hours
Crystal temperature	T_c	max.	150	°C
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−25 to + 150	°C

THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient	$R_{th\ j\text{-}a}$	=	55	K/W

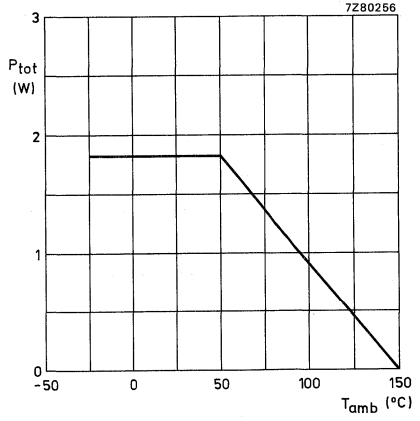


Fig. 2 Power derating curve.

CHARACTERISTICS

V_P = 6 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	V_P	3,6	6	15	V
Supply current; total quiescent at V_P = 6 V	I_{tot}	–	10	–	mA
Power amplifier					
Output power at d_{tot} = 10%*					
V_P = 6 V	P_o	–	1	–	W
V_P = 9 V	P_o	–	2	–	W
Closed loop voltage gain	G_c	–	36	–	dB
Total harmonic distortion at P_o = 0,5 W	d_{tot}	–	–	1	%
Input impedance	$\|Z_i\|$	0,5	–	–	MΩ
Ripple rejection at f = 100 Hz (R_S = 0 Ω)	RR	40	50	–	dB
Noise output voltage (r.m.s. value) R_S = 0 Ω; B = 60 Hz to 15 kHz	$V_{n(rms)}$	–	90	200	μV
Noise output voltage at 500 kHz R_S = 0 Ω; B = 5 kHz	V_n	–	8	–	μV
Preamplifier					
Open loop voltage gain at f = 10 kHz	G_o	70	78	–	dB
Closed loop voltage gain	G_c	–	52	–	dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\,min}$	35	–	–	dB
Output voltage at d_{tot} = 1%	V_o	1	–	–	V
Output voltage with A.L.C. V_i = 2 mV	V_o	0,45	0,5	0,55	V
Total harmonic distortion with A.L.C.					
V_i = 2 mV	d_{tot}	–	–	1	%
V_i = 360 mV	d_{tot}	–	–	3	%
Signal-to-noise ratio related to V_i = 1,2 mV; R_S = 1 kΩ; B = 60 Hz to 15 kHz	S/N	–	60	–	dB
Input impedance	$\|Z_i\|$	100	–	–	kΩ
Ripple rejection at f = 100 Hz; R_S = 0 Ω	RR	50	54	–	dB
Output impedance **	$\|Z_o\|$	–	–	50	Ω

* Measured with an ideal coupling capacitor connected to the speaker load.

** I_P (effective value) must not exceed 1 mA.

parameter	symbol	min.	typ.	max.	unit
Automatic Level Control (A.L.C.) (see Fig. 3) **					
Gain variation for ΔV_i = 45 dB	ΔG_v	–	2	3	dB
Limiting time*	t_l	–	–	50	ms
Level setting time*	t_s	–	–	50	ms
Recovery time* ▲	t_r	–	100	–	s
Voltage stabilizer					
Output voltage	$V_{11\text{-}15}$	–	2,6	–	V
Load current	I_{11}	–	–	1,5	mA
Ripple rejection at f = 100 Hz	RR	40	–	–	dB

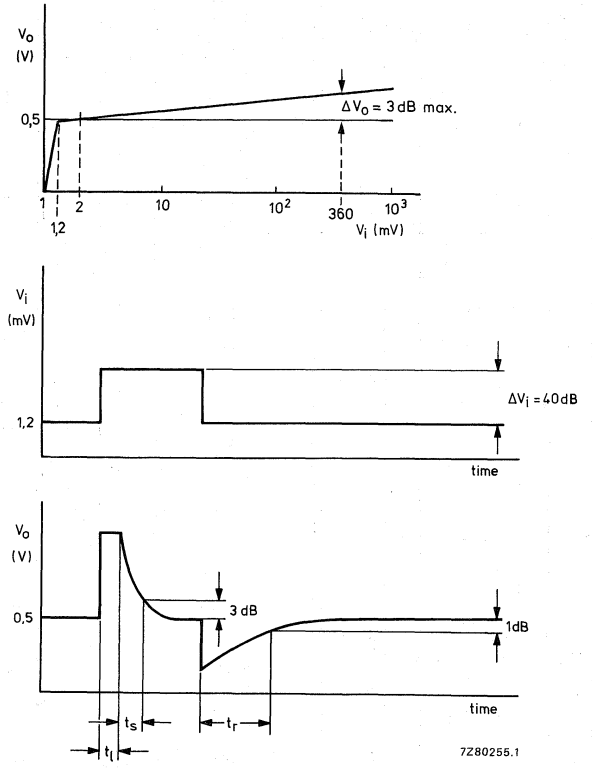


Fig. 3 Typical A.L.C. curve with R_S = 10 kΩ.

* At ΔV_i = 40 dB with respect to V_i = 1,2 mV.

** The A.L.C. tracking in stereo has a typical spread of 1 dB if pins 6 of both ICs are connected to the same RC network.

▲ Without a shunt resistor across A.L.C.
With 1 MΩ or 2,2 MΩ across A.L.C. recovery time becomes 22 or 50 seconds.

12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V (< 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P	6 to 18	V
Repetitive peak output current	I_{ORM}	< 4	A
Output power at d_{tot} = 10% (with bootstrap)			
V_P = 14,4 V; R_L = 2 Ω	P_o	> 10	W
		typ. 12	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ. 7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ. 3,5	W
Output power at d_{tot} = 10% (without bootstrap)			
V_P = 14,4 V; R_L = 4 Ω	P_o	> 4,5	W
Input impedance			
preamplifier (pin 8)	$\|Z_i\|$	typ. 40	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ. 40	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ. 30	mA
Stand-by current	I_{sb}	< 1	mA
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max. 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).

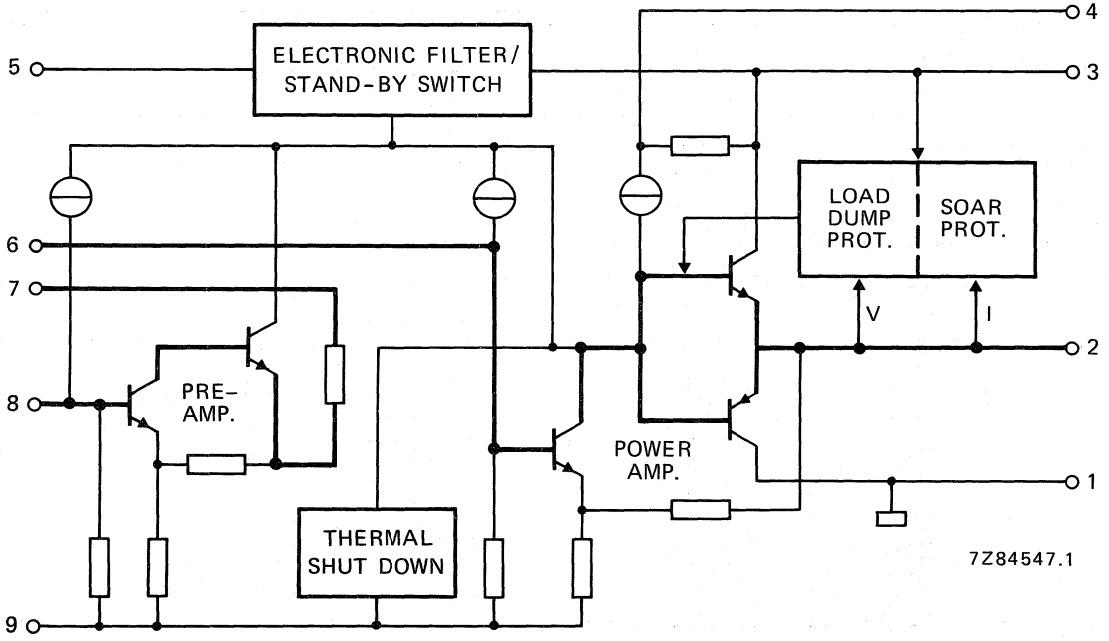


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; load dump	V_P	max.	45 V
Non-repetitive peak output current	I_{OSM}	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100 hours

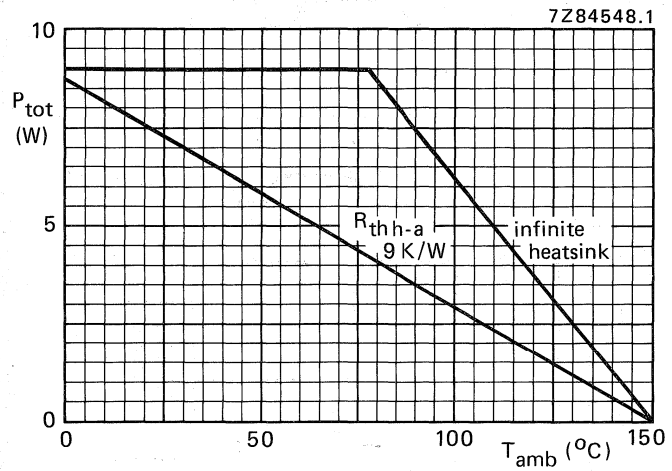


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{5{,}2} = 17{,}3\ \text{K/W}$$

Since $R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} = 8$ K/W, $R_{th\ h\text{-}a} = 17{,}3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current			
at V_P = 14,4 V	I_{tot}	typ.	30 mA
at V_P = 18 V	I_{tot}	typ.	40 mA

A.C. CHARACTERISTICS

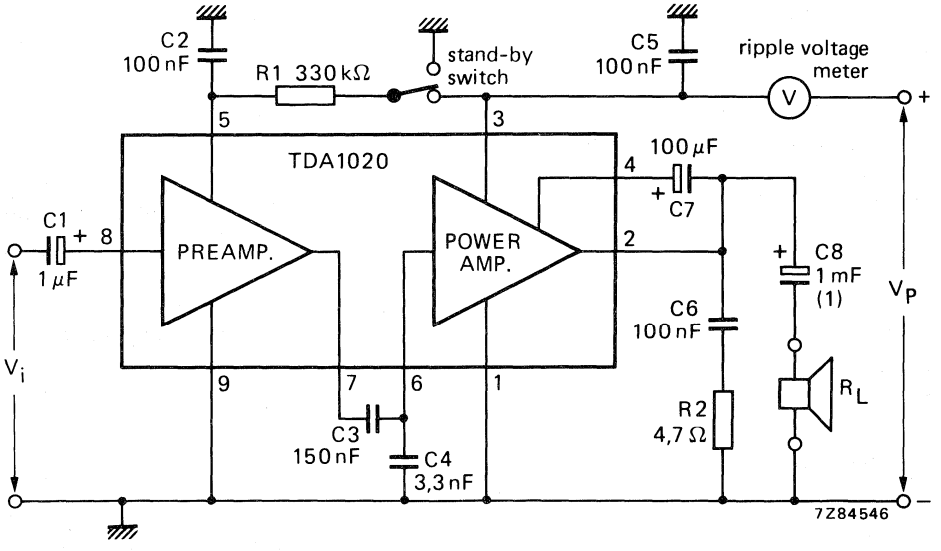
T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; unless otherwise specified; see also Fig. 3

Output power at d_{tot} = 10%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5 W
Output power at d_{tot} = 1%; with bootstrap (note 1)			
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,5 W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3 W
Output voltage (r.m.s. value)			
R_L = 1 kΩ; d_{tot} = 0,5%	$V_{o(rms)}$	typ.	5 V
Output power at d_{tot} = 10%; without bootstrap	P_o	>	4,5 W
Voltage gain			
preamplifier (note 2)	G_{v1}	typ.	17,7 dB
			16,7 to 18,7 dB
power amplifier	G_{v2}	typ.	29,5 dB
			28,5 to 30,5 dB
total amplifier	$G_{v\,tot}$	typ.	47 dB
			46,2 to 48,2 dB
Input impedance			
preamplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
power amplifier	$\|Z_i\|$	typ.	40 kΩ
			28 to 52 kΩ
Output impedance			
preamplifier	$\|Z_o\|$	typ.	2,0 kΩ
			1,4 to 2,6 kΩ
power amplifier	$\|Z_o\|$	typ.	50 mΩ
Output voltage (r.m.s. value) at d_{tot} = 1%			
preamplifier (note 2)	$V_{o(rms)}$	>	1 V
		typ.	1,5 V
Frequency response	B		50 Hz to 25 kHz
Noise output voltage (r.m.s. value; note 3)			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3 mV
		<	0,5 mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,5 mV
		<	1,0 mV

Ripple rejection (note 4)			
at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	>	48 dB
		typ.	54 dB
Bootstrap current at onset of clipping (pin 4)			
R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).



(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

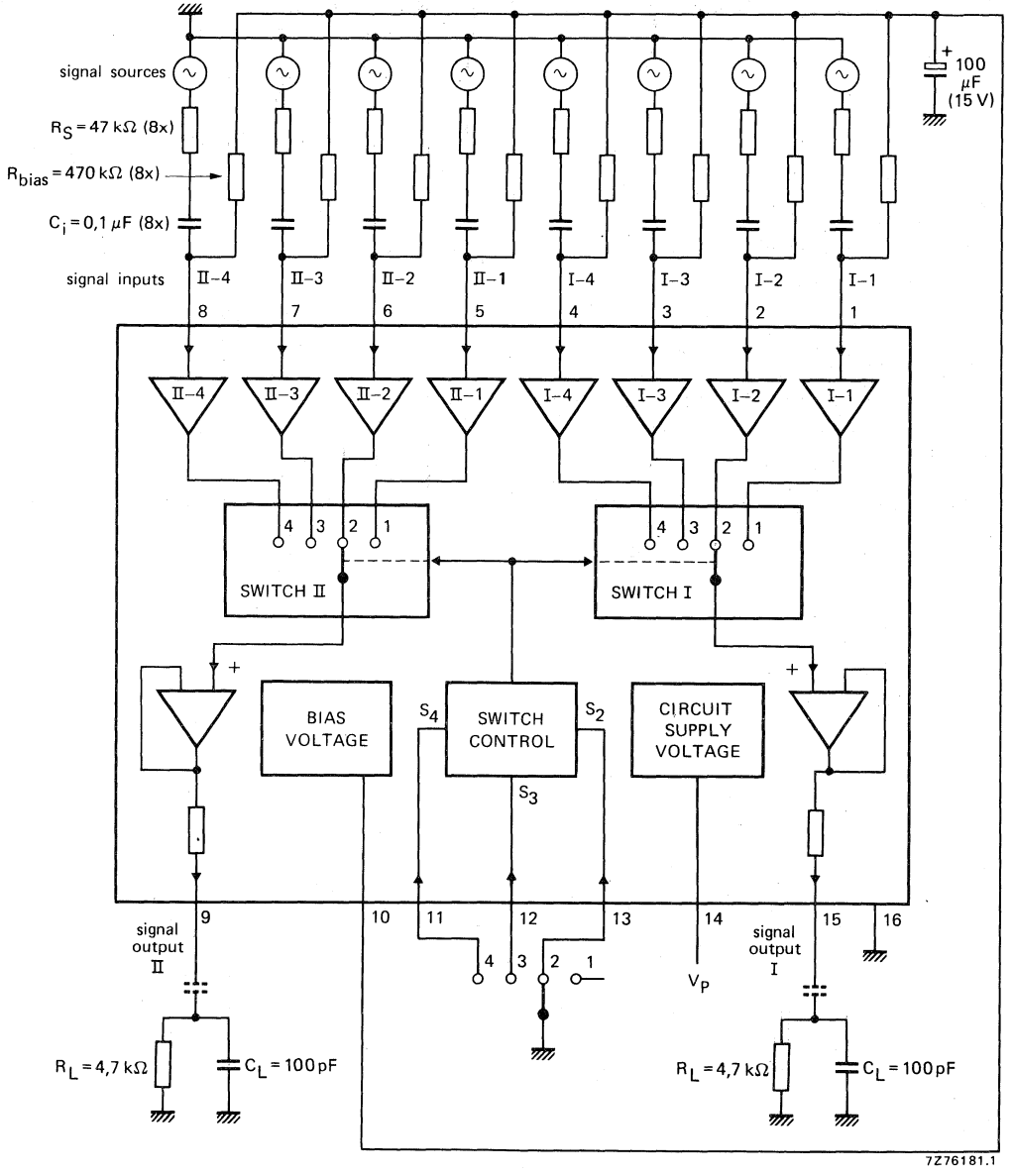


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 20 V; T_{amb} = 25 °C; unless otherwise specified

Current consumption				
without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5	mA
			2 to 5	mA
Supply voltage range (pin 14)	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at R_S = 1 kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to 11,8	11 V * V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1{,}5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* $V_{10\text{-}16}$ is typically $0{,}5 \cdot V_{14\text{-}16} + 1{,}5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5 dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 mV 100 mV
Total harmonic distortion			
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01 %
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02 %
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03 %
Output signal handling			
d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 V 5,3 V
Noise output voltage (unweighted)			
f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5 μV
Noise output voltage (weighted)			
f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12 μV
Amplitude response			
V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1 dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75 dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90 dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

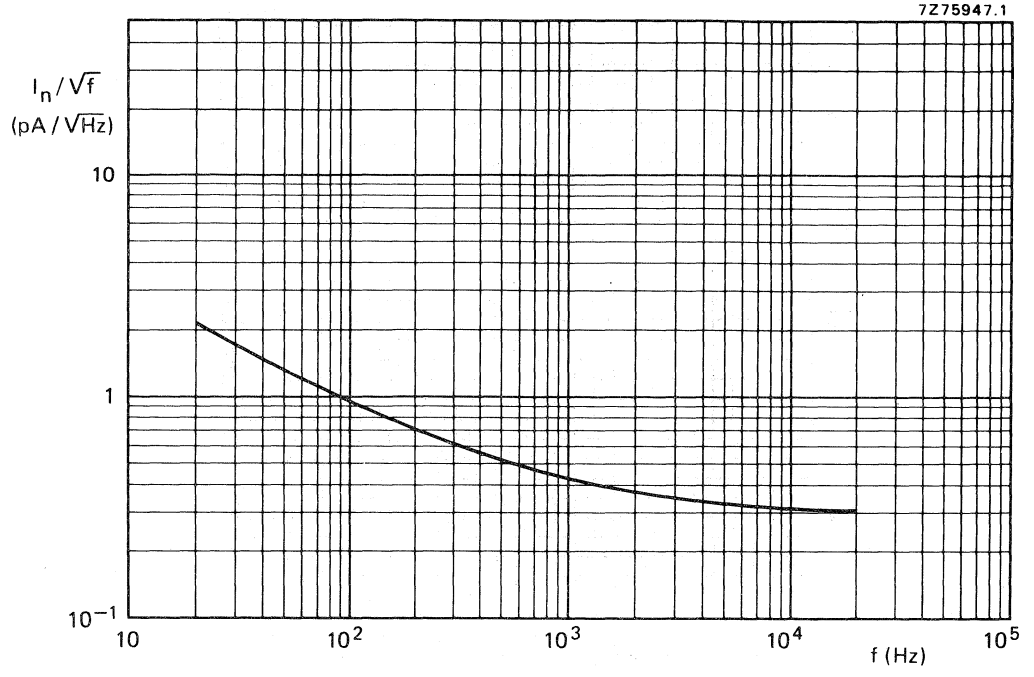


Fig. 2 Equivalent input noise current.

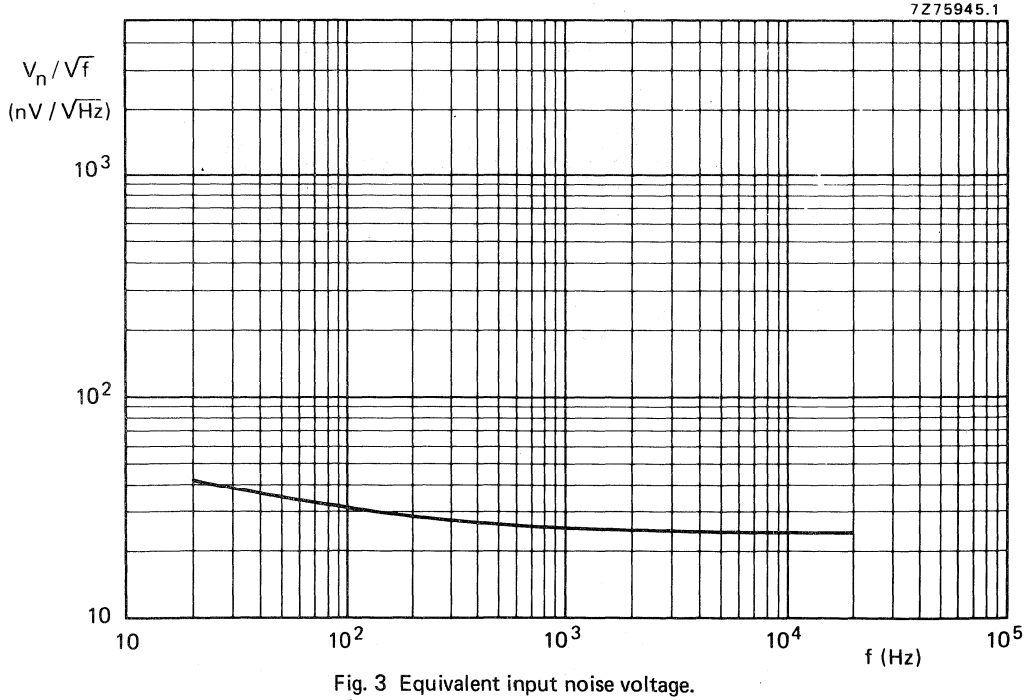


Fig. 3 Equivalent input noise voltage.

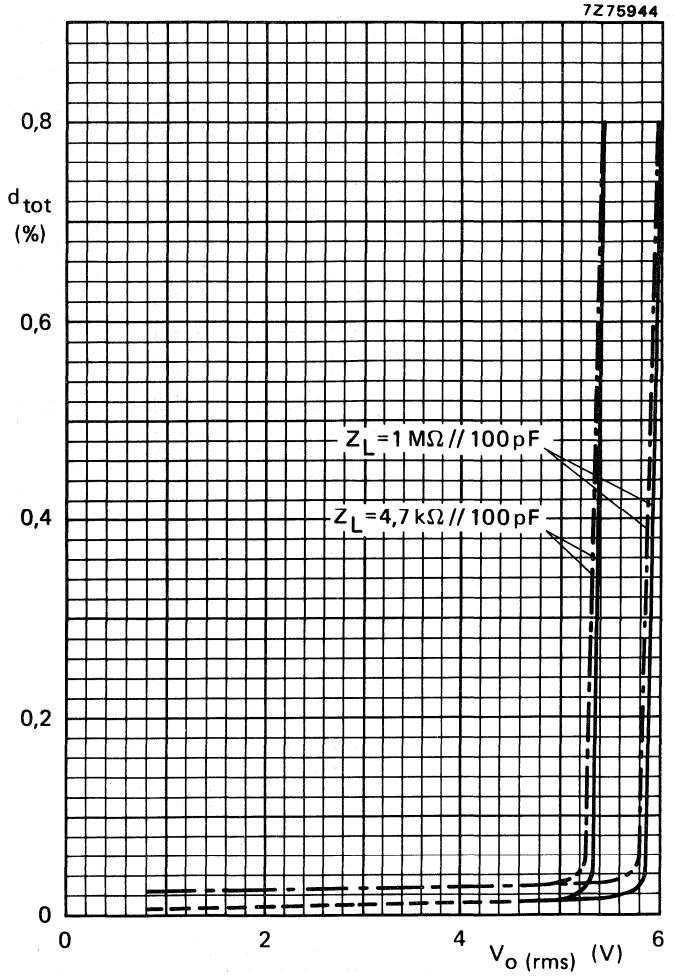


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; —— - —— - f = 20 kHz.

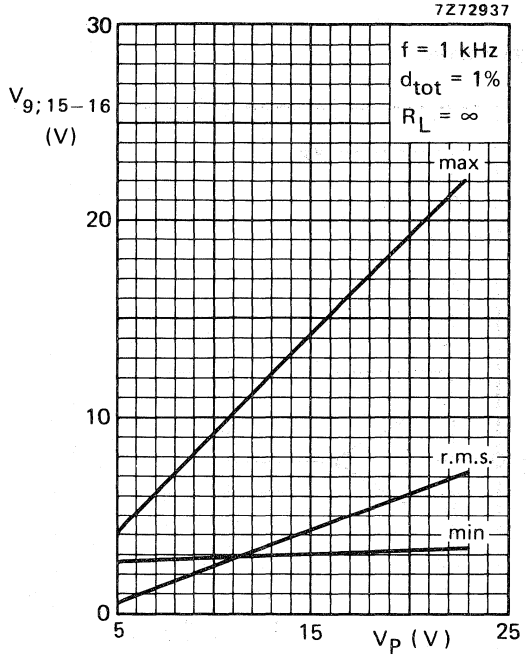


Fig. 5 Output voltage as a function of supply voltage.

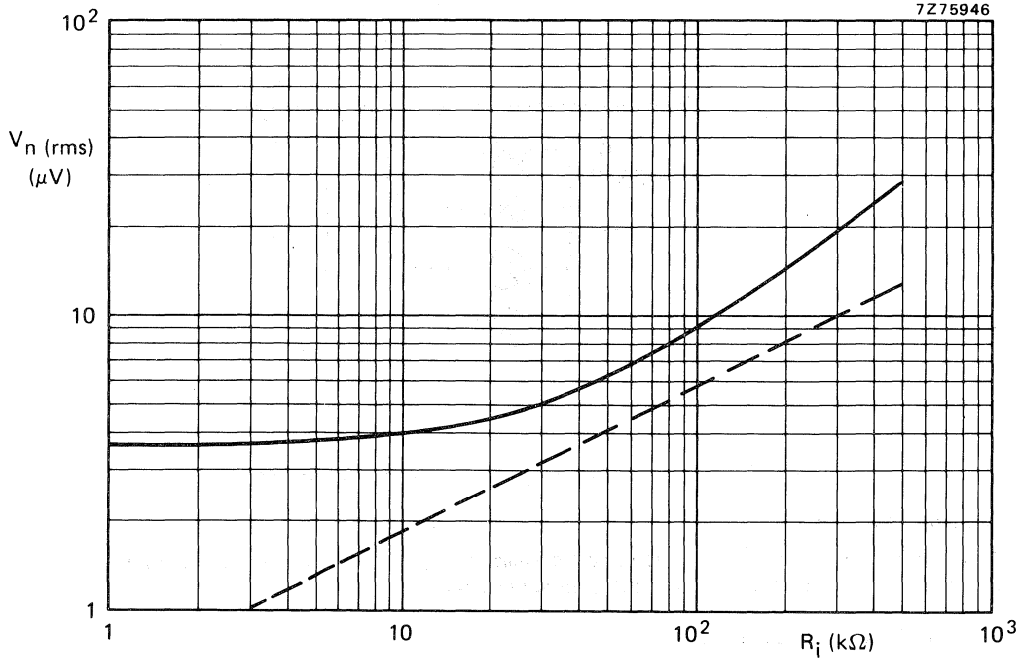


Fig. 6 Noise output voltage as a function of input resistance; G_V = 1; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

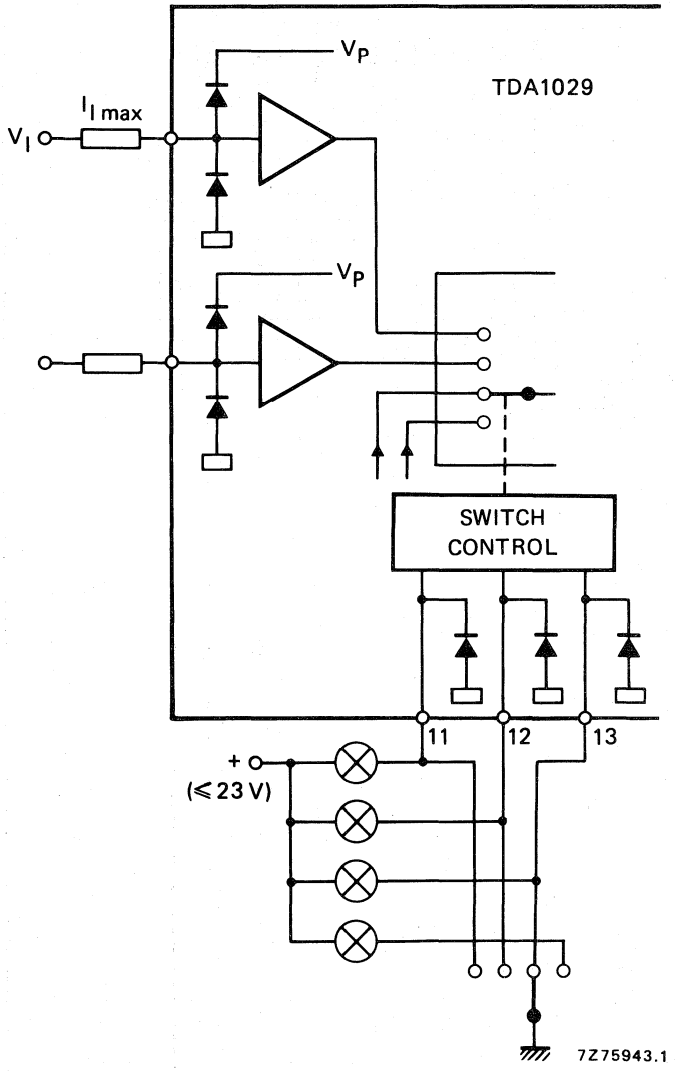


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

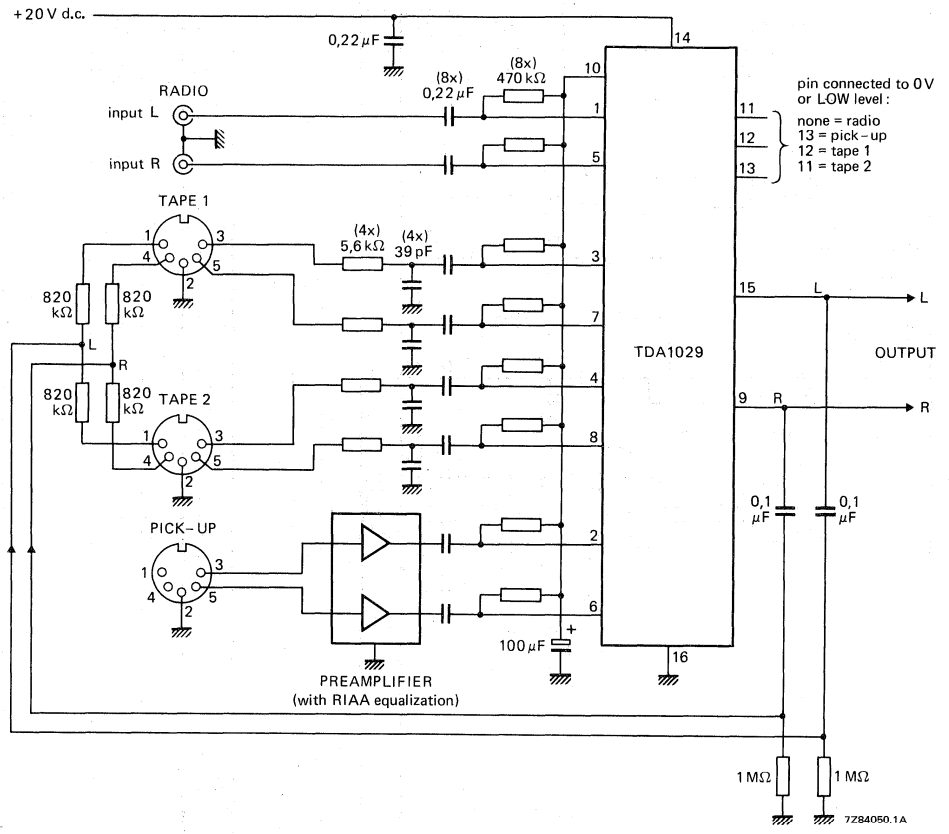


Fig. 8 TDA1029 connected as a four input stereo source selector.

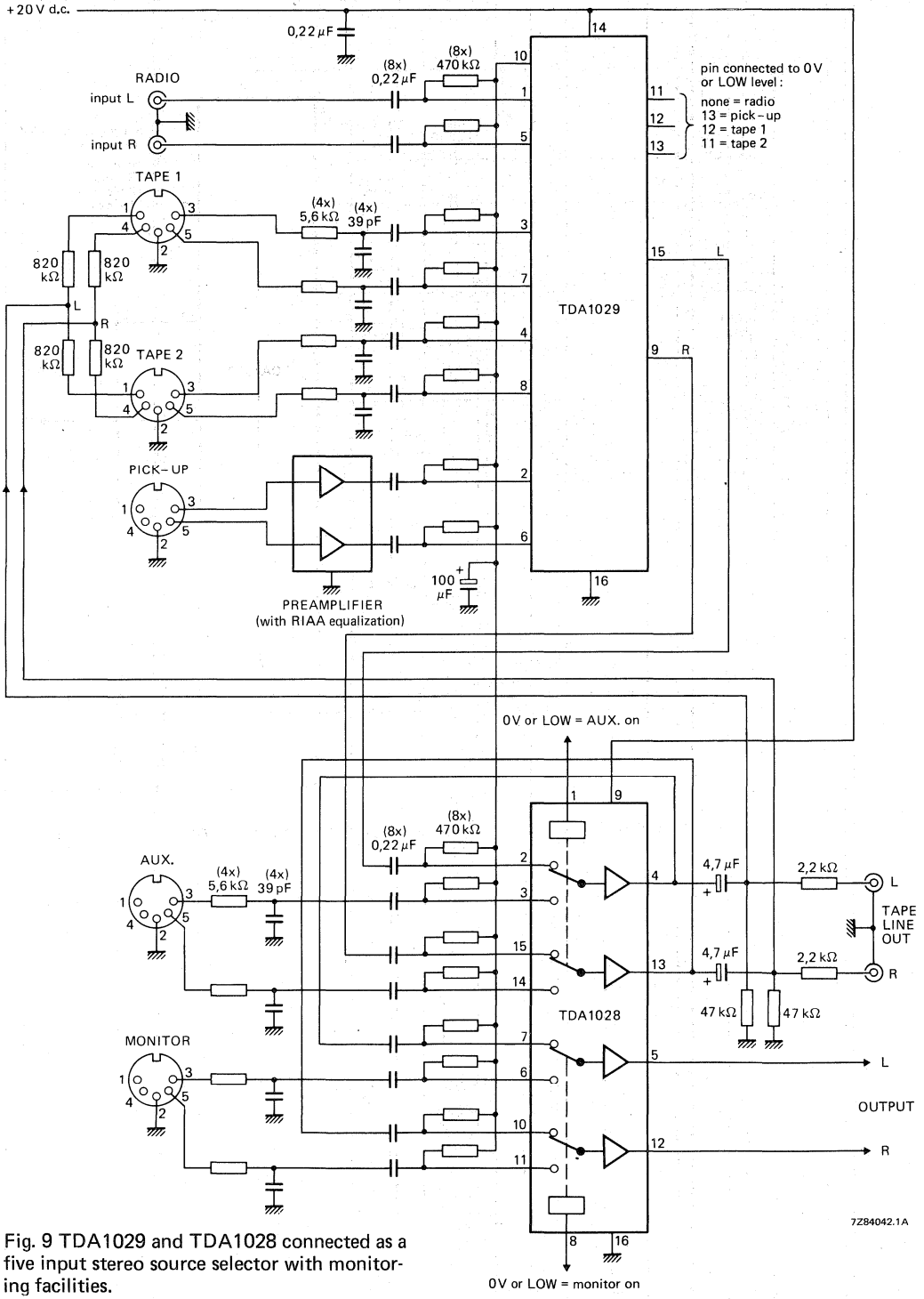


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

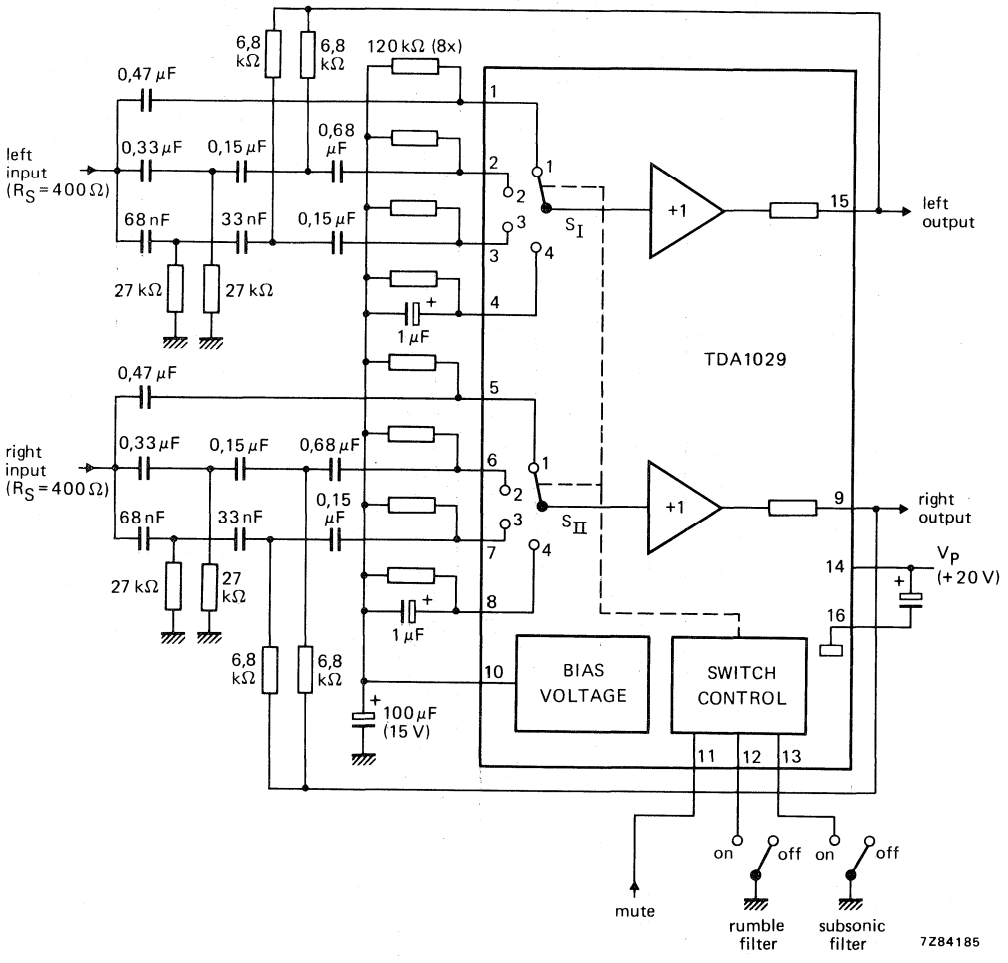


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

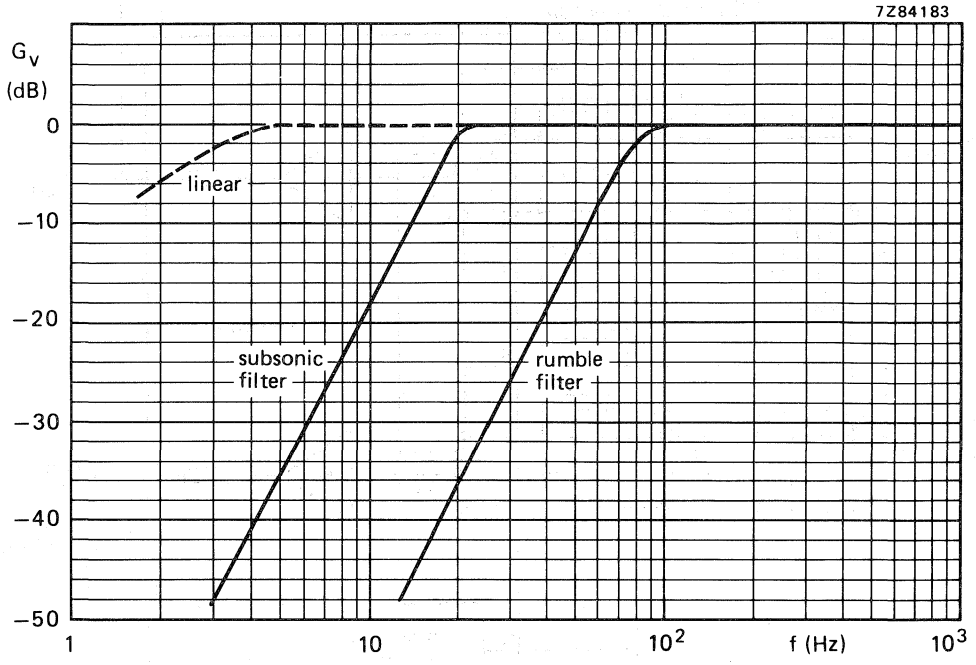


Fig. 11 Frequency response curves for the circuit of Fig. 10.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072A integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle r.f. signals up to 500 mV. R.F. radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the i.f. amplifier.

Features

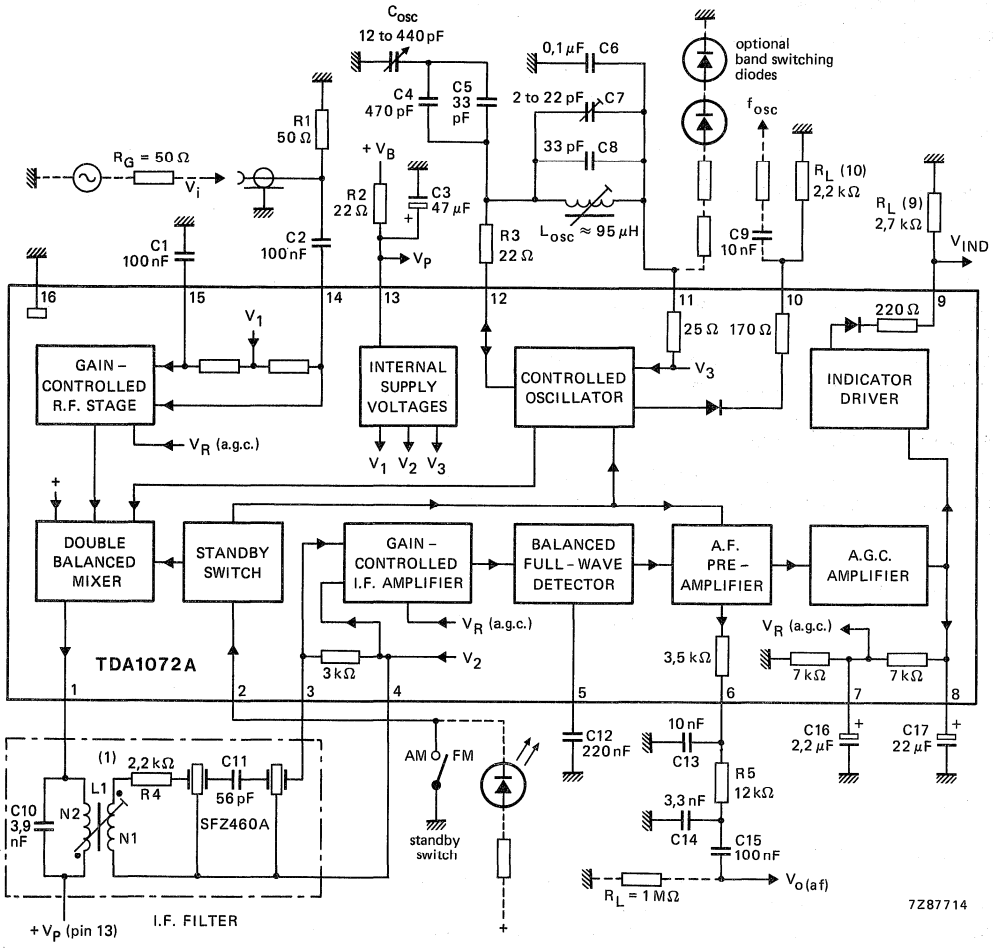
- Inputs protected against damage by static discharge
- Gain-controlled r.f. stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled i.f. stage with wide a.g.c. range
- Full-wave, balanced envelope detector
- Internal generation of a.g.c. voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- A.F. preamplifier with possibilities for simple a.f. filtering
- Electronic standby switch

QUICK REFERENCE DATA

Supply voltage range	V_P	7,5 to 18	V
Supply current range	I_P	15 to 30	mA
R.F. input voltage for S + N/N = 6 dB at m = 30%	V_i	typ. 1,5	μV
R.F. input voltage for 3% total harmonic distortion (THD) at m = 80%	V_i	typ. 500	mV
A.F. output voltage with V_i = 2 mV; f_i = 1 MHz; m = 30% and f_m = 400 Hz	$V_{o(af)}$	typ. 310	mV
A.G.C. range: change of V_i for 1 dB change of $V_{o(af)}$		typ. 86	dB
Field strength indicator voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	V_{IND}	typ. 2,8	V

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1 : N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_I = 4,8 kΩ.

Fig. 1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled r.f. stage and mixer

The differential amplifier in the r.f. stage employs an a.g.c. negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by a.g.c. delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is improved. Low noise working is achieved in the differential amplifier by using transistors with low base resistance.

A double balanced mixer provides the i.f. output signal to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output (pin 10) is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled i.f. amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the a.g.c. negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. Residual i.f. carrier is blocked from the signal path by an internal low-pass filter.

A.F. preamplifier

This stage preamplifies the audio frequency output signal. The amplifier output has an emitter follower with a series resistor which, together with an external capacitor, yields the required low-pass for a.f. filtering.

A.G.C. amplifier

The a.g.c. amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the a.g.c. voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives fast a.g.c. settling time which is advantageous for electronic search tuning. The a.g.c. settling time can be further reduced by using capacitors of smaller value in the external filter (C16 and C17). The a.g.c. voltage is fed to the r.f. and i.f. stages via suitable a.g.c. delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If the field strength information is not needed, $R_{L(9)}$ can be omitted.

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and a.f. preamplifier are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Supply voltage	$V_P = V_{13-16}$	max.	20	V
Total power dissipation	P_{tot}	max.	875	mW
Input voltage	$\|V_{14-15}\|$	max.	12	V
	$-V_{14-16}$, $-V_{15-16}$	max.	0,6	V
	V_{14-16}, V_{15-16}	max.	V_P	V
Input current	$\|I_{14}\|$, $\|I_{15}\|$	max.	200	mA
Operating ambient temperature range	T_{amb}	−40 to	+80	°C
Storage temperature range	T_{stg}	−55 to	+150	°C
Junction temperature	T_j	max.	+125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j-a}$	=	80	K/W

DEVICE CHARACTERISTICS

$V_P = V_{13-16} = 8{,}5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{if} = 460$ kHz; measured in test circuit of Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	$V_P = V_{13-16}$	7,5	8,5	18	V
Supply current	$I_P = I_{13}$	15	23	30	mA
R.F. stage and mixer					
Input voltage (d.c. value)	V_{14-16}, V_{15-16}	–	$V_P/2$	–	V
R.F. input impedance at $V_i < 300\ \mu V$	R_{14-16}, R_{15-16}	–	5,5	–	kΩ
	C_{14-16}, C_{15-16}	–	25	–	pF
R.F. input impedance at $V_i > 10$ mV	R_{14-16}, R_{15-16}	–	8	–	kΩ
	C_{14-16}, C_{15-16}	–	22	–	pF
I.F. output impedance	R_{1-16}	500	–	–	kΩ
	C_{1-16}	–	6	–	pF
Conversion transconductance before start of a.g.c.	I_1/V_i	–	6,5	–	mA/V
Maximum i.f. output voltage, inductive coupling to pin 1	$V_{1-13(p-p)}$	–	5	–	V
D.C. value of output current (pin 1) at $V_i = 0$ V	I_1	–	1,2	–	mA
A.G.C. range of input stage		–	30	–	dB
R.F. signal handling capability: input voltage for THD = 3% at m = 80%	$V_{i(rms)}$	–	500	–	mV

parameter	symbol	min.	typ.	max.	unit
Oscillator					
Frequency range	f_{osc}	0,6	–	60	MHz
Oscillator amplitude (pins 11 to 12)	$V_{11\text{-}12}$	–	130	150	mV
External load impedance	$R_{12\text{-}11(ext)}$	0,5	–	200	kΩ
External load impedance for no oscillation	$R_{12\text{-}11(ext)}$	–	–	60	Ω
Ripple rejection at $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_{13\text{-}16}/V_{11\text{-}16}]$)	RR	–	55	–	dB
Source voltage for switching diodes (6 x V_{BE})	$V_{11\text{-}16}$	–	4,2	–	V
D.C. output current (for switching diodes)	$-I_{11}$	0	–	20	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)	$\Delta V_{11\text{-}16}$	–	0,5	–	V
Buffered oscillator output					
D.C. output voltage	$V_{10\text{-}16}$	–	0,7	–	V
Output signal amplitude	$V_{10\text{-}16(p\text{-}p)}$	–	320	–	mV
Output impedance	R_{10}	–	170	–	Ω
Output current	$-I_{10(peak)}$	–	–	3	mA
I.F., a.g.c. and a.f. stages					
D.C. input voltage	$V_{3\text{-}16}$, $V_{4\text{-}16}$	–	2,0	–	V
I.F. input impedance	$R_{3\text{-}4}$	2,4	3	3,9	kΩ
	$C_{3\text{-}4}$	–	7	–	pF
I.F. input voltage for THD = 3% at m = 80%	$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of a.g.c.	$V_{3\text{-}4}/V_{6\text{-}16}$	–	68	–	dB
A.G.C. range of i.f. stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{o(af)}$; $V_{3\text{-}4(ref)}$ = 75 mV	$\Delta V_{3\text{-}4}$	–	55	–	dB
A.F. output voltage at $V_{3\text{-}4(if)}$ = 50 μV	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at $V_{3\text{-}4(if)}$ = 1 mV	$V_{o(af)}$	–	310	–	mV
A.F. output impedance (pin 6)	$\lvert Z_o \rvert$	–	3,5	–	kΩ
Indicator driver					
Output voltage at V_i = 0 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	–	20	150	mV
Output voltage at V_i = 500 mV; $R_{L(9)}$ = 2,7 kΩ	$V_{9\text{-}16}$	2,5	2,8	3,1	V
Load resistance	$R_{L(9)}$	1,5	–	–	kΩ

DEVICE CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Standby switch					
Switching threshold at V_P = 7,5 to 18 V; T_{amb} = −40 to + 80 °C					
on-voltage	V_{2-16}	0	–	2,0	V
off-voltage	V_{2-16}	3,5	–	20	V
on-current at V_{2-16} = 0 V	$-I_2$	–	–	200	μA
off-current at V_{2-16} = 20 V	$\|I_2\|$	–	–	10	μA

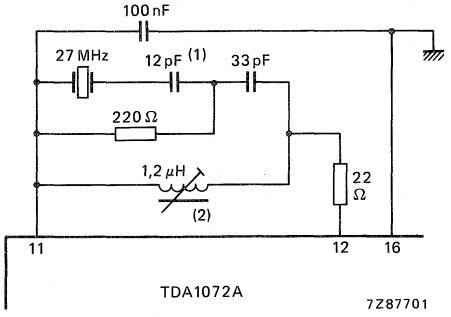
OPERATING CHARACTERISTICS

V_P = 8,5 V; f_i = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity					
R.F. input required for S + N/N = 6 dB	V_i	–	1,5	–	μV
R.F. input required for S + N/N = 26 dB	V_i	–	15	–	μV
R.F. input required for S + N/N = 46 dB	V_i	–	150	–	μV
R.F. input at start of a.g.c.	V_i	–	30	–	μV
R.F. large signal handling					
R.F. input at THD = 3%; m = 80%	V_i	–	500	–	mV
R.F. input at THD = 3%; m = 30%	V_i	–	700	–	mV
R.F. input at THD = 10%; m = 30%	V_i	–	900	–	mV
A.G.C. range					
Change of V_i for 1 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	86	–	dB
Change of V_i for 6 dB change of $V_{o(af)}$; $V_{i(ref)}$ = 500 mV	ΔV_i	–	91	–	dB
Output signal					
A.F. output voltage at V_i = 4 μV; m = 80%	$V_{o(af)}$	–	130	–	mV
A.F. output voltage at V_i = 1 mV	$V_{o(af)}$	240	310	390	mV
THD at V_i = 1 mV; m = 80%	d_{tot}	–	0,5	–	%
THD at V_i = 500 mV; m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio at V_i = 100 mV	(S + N)/N	–	58	–	dB
Ripple rejection at V_i = 2 mV; $V_{P(rms)}$ = 100 mV; f_P = 100 Hz ($RR = 20 \log [V_P/V_{o(af)}]$)	RR	–	38	–	dB

parameter	symbol	min.	typ.	max.	unit
Unwanted signals					
Suppression of i.f. whistles at V_i = 15 μV; m = 0% related to a.f. signal of m = 30%					
at $f_i \approx 2 \times f_{if}$	α_{2if}	–	37	–	dB
at $f_i \approx 3 \times f_{if}$	α_{3if}	–	44	–	dB
I.F. suppression at r.f. input					
for symmetrical input	α_{if}	–	40	–	dB
for asymmetrical input	α_{if}	–	40	–	dB
Residual oscillator signal at mixer output					
at f_{osc}	$I_{1(osc)}$	–	1	–	μA
at 2 x f_{osc}	$I_{1(2osc)}$	–	1,1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0,1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig. 2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

APPLICATION INFORMATION (continued)

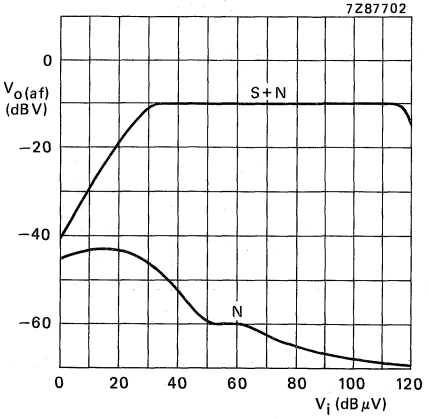


Fig. 3 A.F. output as a function of r.f. input in the circuit of Fig. 1; f_i = 1 MHz; f_m = 400 Hz; m = 30%.

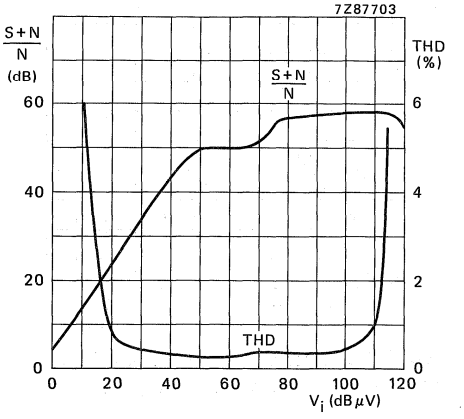


Fig. 4 Total harmonic distortion and (S + N)/N as functions of r.f. input in the circuit of Fig. 1; m = 30% for (S + N)/N curve and m = 80% for THD curve.

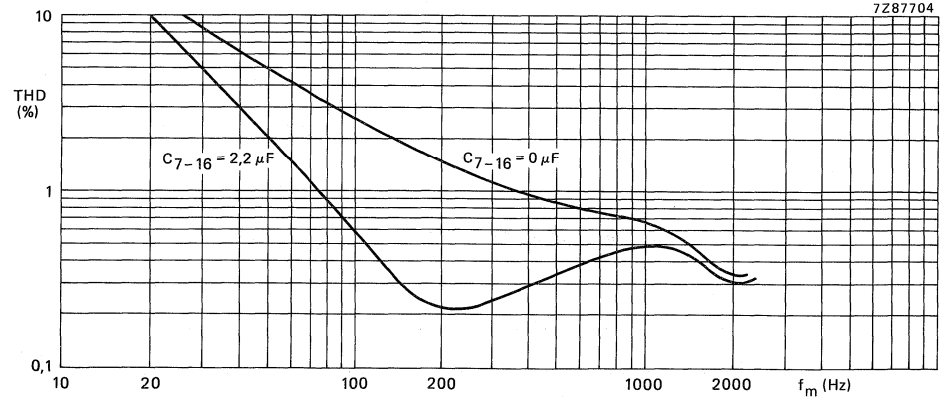


Fig. 5 Total harmonic distortion as a function of modulation frequency at V_i = 5 mV; m = 80%; measured in the circuit of Fig. 1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2,2 μF.

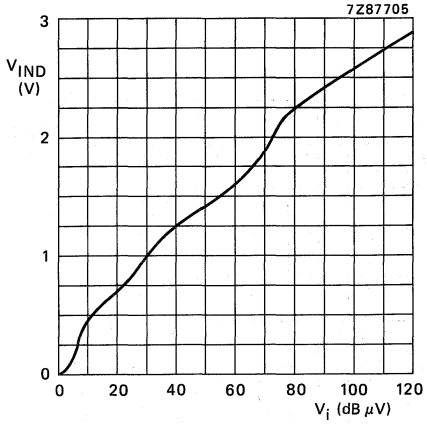


Fig. 6 Indicator driver voltage as a function of r.f. input in the circuit of Fig. 1.

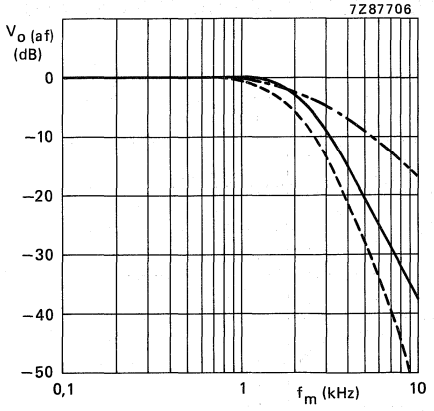


Fig. 7 Typical frequency response curves from Fig. 1 showing the effect of filtering as follows:
——— with i.f. filter;
—·—·—·— with a.f. filter;
– – – – – with i.f. and a.f. filters.

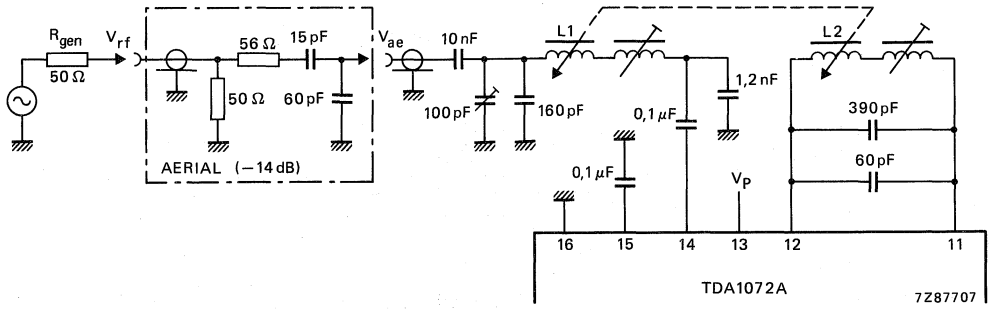


Fig. 8 Car radio application with inductive tuning.

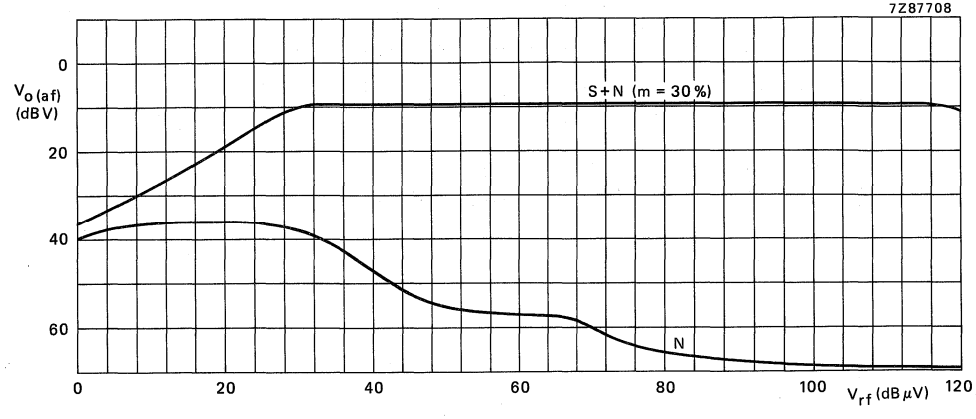


Fig. 9 A.F. output as a function of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

APPLICATION INFORMATION (continued)

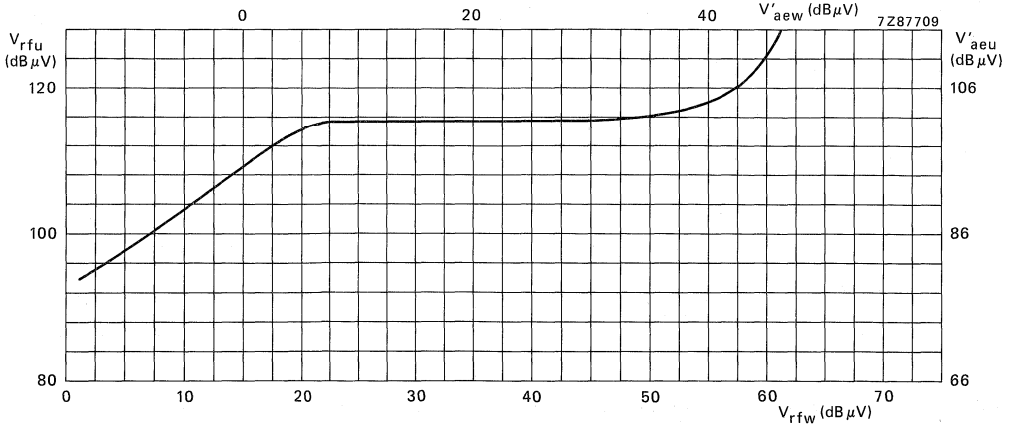


Fig. 10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig. 8 with the input circuit as shown in Fig. 11. Curve is for Wanted $V_{o(af)}$/Unwanted $V_{o(af)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

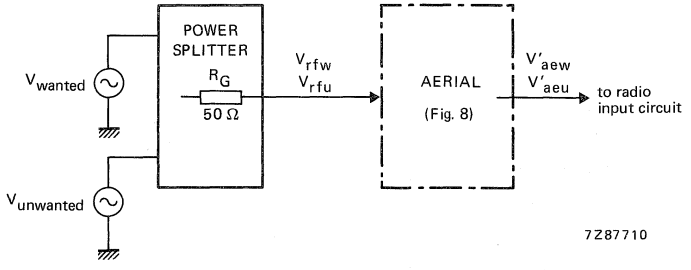


Fig. 11 Input circuit to show cross-modulation suppression (see Fig. 10).

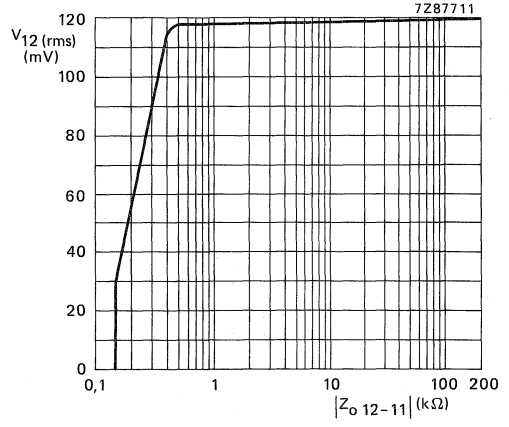


Fig. 12 Oscillator amplitude as a function of pin 11, 12 impedance in the circuit of Fig. 8.

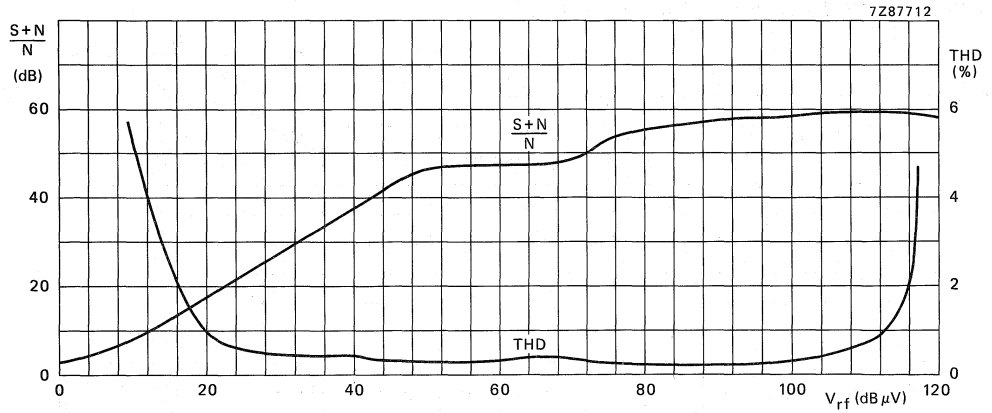


Fig. 13 Total harmonic distortion and (S + N)/N as functions of r.f. input using the circuit of Fig. 8 with that of Fig. 1.

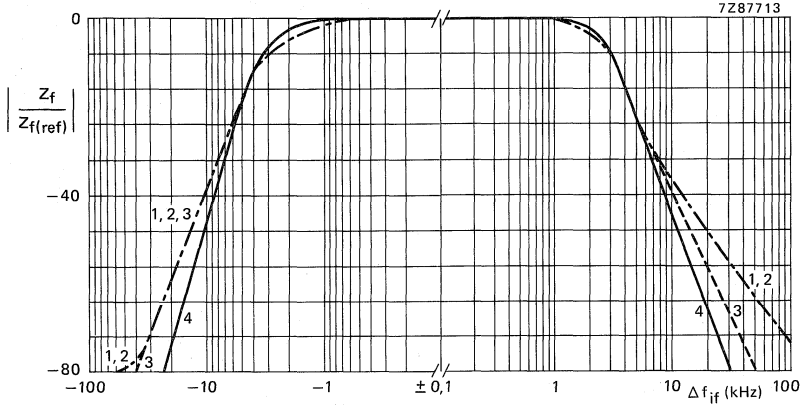


Fig. 14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig. 15; centre frequency = 455 kHz.

APPLICATION INFORMATION (continued)

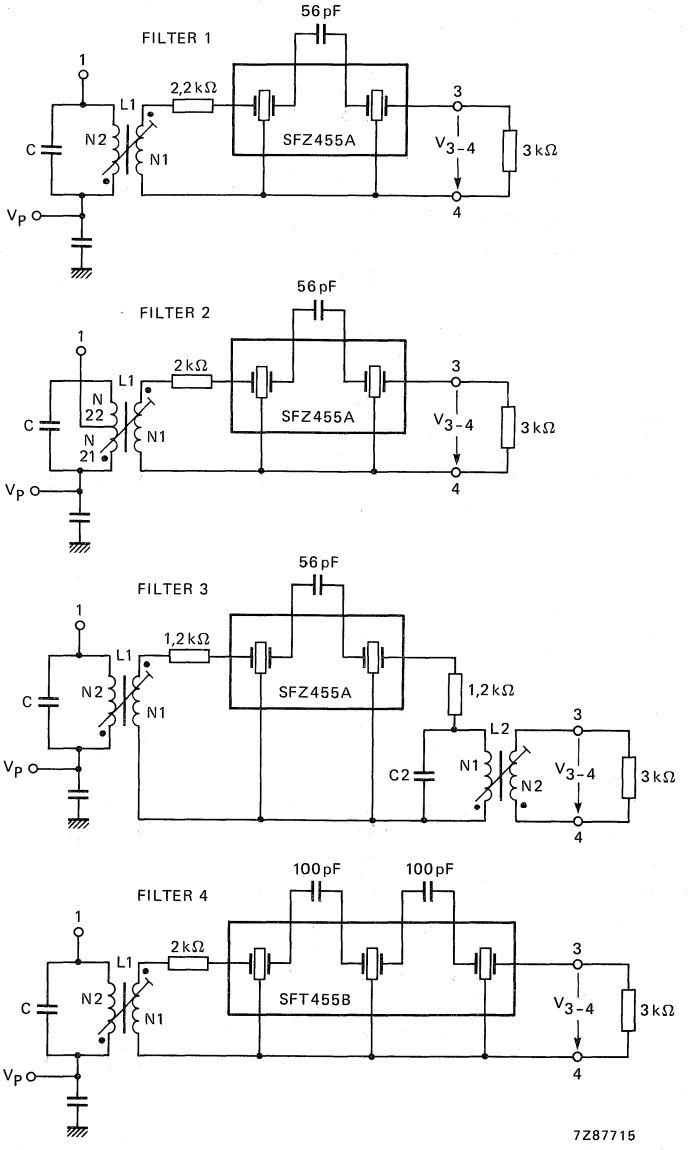
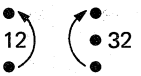
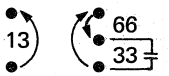
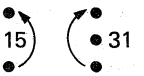
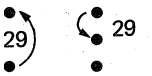
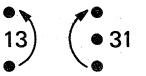


Fig. 15 I.F. filter variants applied to the circuit of Fig. 1. For filter data, refer to Table 1.

Table 1 Data for I.F. filters shown in Fig. 15. Criterium for adjustment is Z_F = maximum (optimum selectivity curve at centre frequency f_0 = 455 kHz). See also Fig. 14.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0,09	0,08	0,09	0,08	0,09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings						
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (–3 dB)	4,2	4,2	4,2		4,5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4,8	3,8	4,2		4,8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0,70	0,67	0,68		0,68	kΩ
Bandwidth (–3 dB)	3,6	3,8	3,6		4,0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding, N2 the outer winding.

APPLICATION INFORMATION (continued)

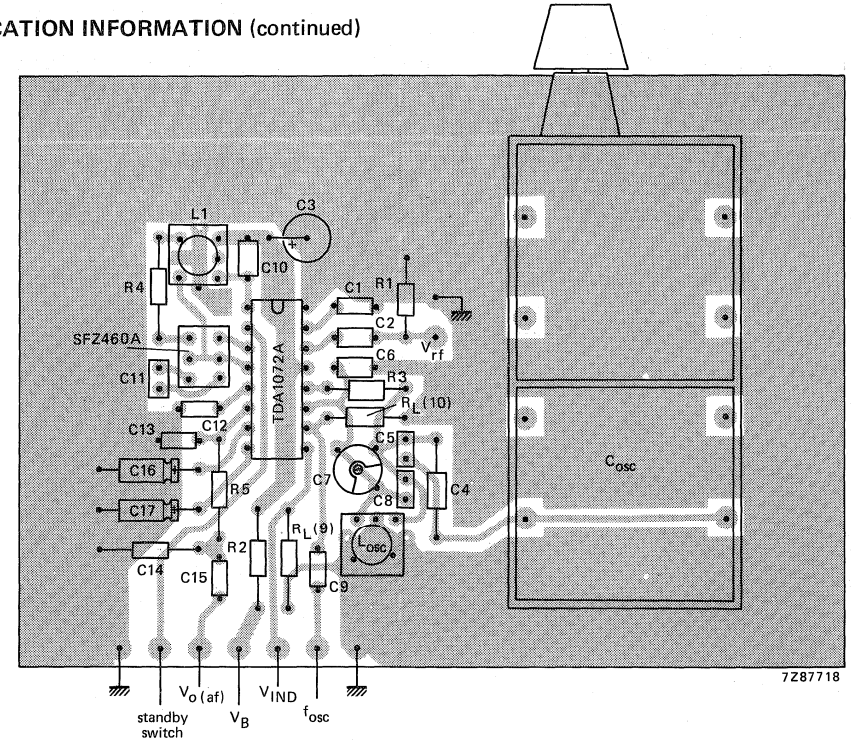


Fig. 16 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 1.

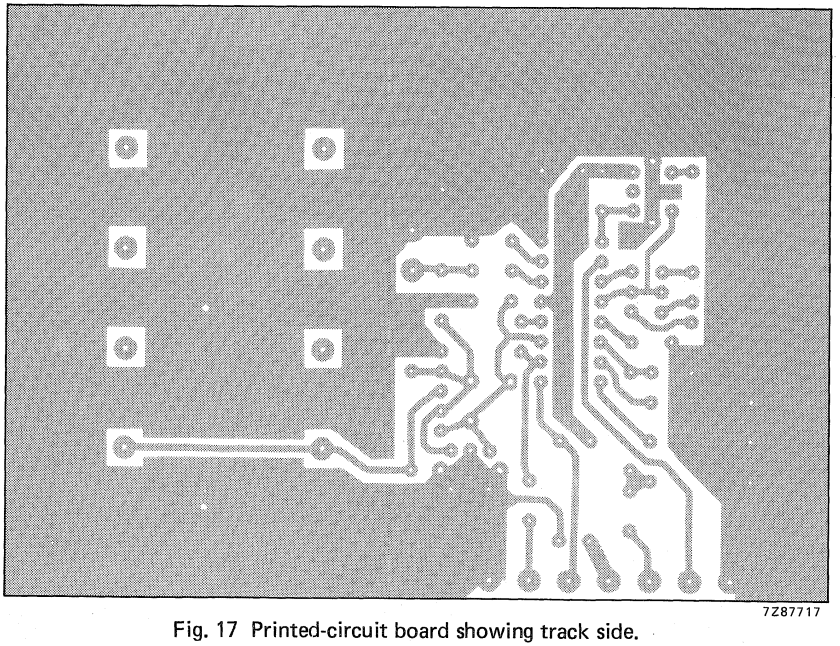
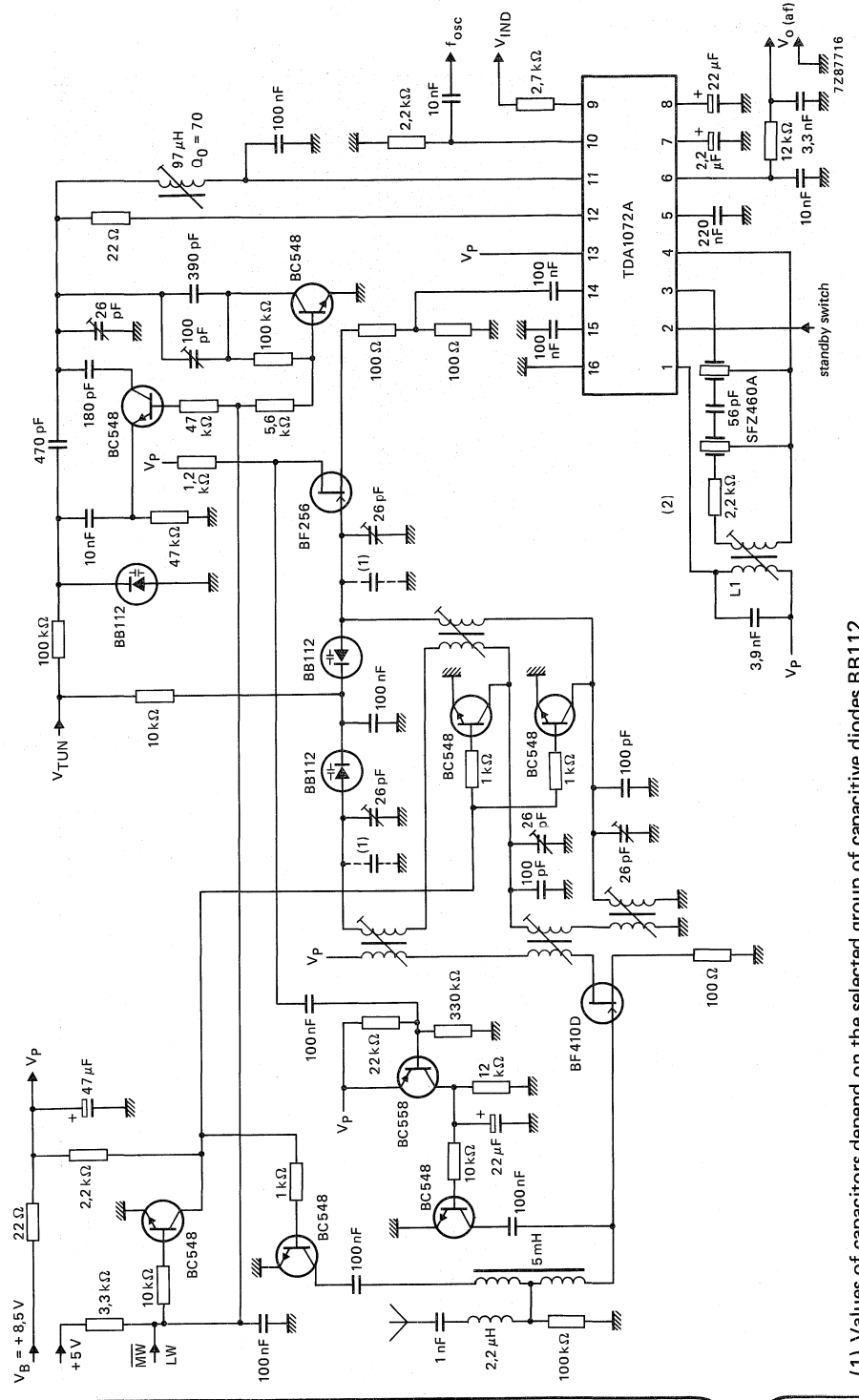


Fig. 17 Printed-circuit board showing track side.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.
(2) For i.f. filter and coil data refer to Fig. 1.

Fig. 18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage a.g.c. optimised for good large-signal handling.

AM RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TDA1072AT integrated AM receiver circuit performs the active and part of the filtering functions of an AM radio receiver. It is intended for use in mains-fed home receivers and car radios. The circuit can be used for oscillator frequencies up to 50 MHz and can handle RF signals up to 500 mV. RF radiation and sensitivity to interference are minimized by an almost symmetrical design. The voltage-controlled oscillator provides signals with extremely low distortion and high spectral purity over the whole frequency range even when tuning with variable capacitance diodes. If required, band switching diodes can easily be applied. Selectivity is obtained using a block filter before the IF amplifier.

Features

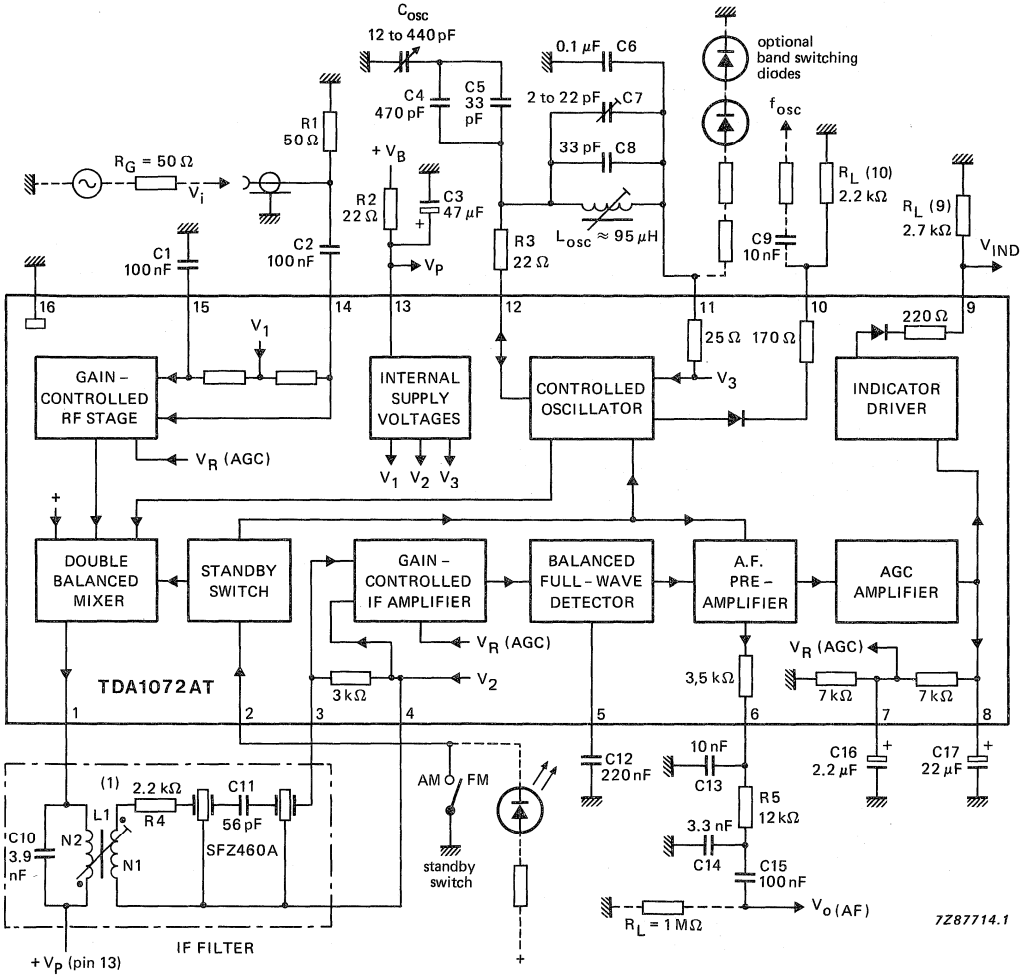
- Inputs protected against damage by static discharge
- Gain-controlled RF stage
- Double balanced mixer
- Separately buffered, voltage-controlled and temperature-compensated oscillator, designed for simple coils
- Gain-controlled IF stage with wide AGC range
- Full-wave, balanced envelope detector
- Internal generation of AGC voltage with possibility of second-order filtering
- Buffered field strength indicator driver with short-circuit protection
- AF preamplifier with possibilities for simple AF filtering
- Electronic standby switch

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	7.5	–	10	V
Supply current range		I_P	15	–	26	mA
RF input voltage for S+N/N = 6 dB at m = 30%		V_I	–	1.5	–	μV
RF input voltage for 3% total harmonic distortion (THD) at m = 80%		V_I	–	500	–	mV
AF output voltage with V_I = 2 mV; f_I = 1 MHz; m = 30% and f_m = 400 Hz		$V_{O(AF)}$	–	310	–	mV
AGC range: change of V_I for 1 dB change of $V_{O(AF)}$			–	86	–	dB
Field strength indicator voltage at V_I = 500 mV; $R_{L(9)}$ = 2.7 kΩ		V_{IND}	–	2.8	–	V

PACKAGE OUTLINE

16-lead mini-pack; plastic (SO16; SOT109A).



(1) Coil data: TOKO sample no. 7XNS-A7523DY; L1: N1/N2 = 12/32; Q_o = 65; Q_B = 57.
Filter data: Z_F = 700 Ω at R_{3-4} = 3 kΩ; Z_1 = 4.8 kΩ.

Fig.1 Block diagram and test circuit (connections shown in broken lines are not part of the test circuit).

FUNCTIONAL DESCRIPTION

Gain-controlled RF stage and mixer

The differential amplifier in the RF stage employs an AGC negative feedback network to provide a wide dynamic range. Very good cross-modulation behaviour is achieved by AGC delays at the various signal stages. Large signals are handled with low distortion and the S/N ratio of small signals is also improved. Low noise working is achieved in the differential amplifier by using transistors with a low base resistance.

A double balanced mixer provides the IF output to pin 1.

Oscillator

The differential amplifier oscillator is temperature compensated and is suitable for simple coil connection. The oscillator is voltage-controlled and has little distortion or spurious radiation. It is specially suitable for electronic tuning using variable capacitance diodes. Band switching diodes can easily be applied using the stabilized voltage $V_{11\text{-}16}$. An extra buffered oscillator output is available for driving a synthesizer. If this is not needed, resistor $R_{L(10)}$ can be omitted.

Gain-controlled IF amplifier

This amplifier comprises two cascaded, variable-gain differential amplifier stages coupled by a band-pass filter. Both stages are gain-controlled by the AGC negative feedback network.

Detector

The full-wave, balanced envelope detector has very low distortion over a wide dynamic range. The residual IF carrier is blocked from the signal path by an internal low-pass filter.

AF preamplifier

This stage preamplifies the audio frequency output. The amplifier output stage uses an emitter follower with a series resistor which, together with an external capacitor, provides the required low-pass filtering for AF signals.

AGC amplifier

The AGC amplifier provides a control voltage which is proportional to the carrier amplitude. Second-order filtering of the AGC voltage achieves signals with very little distortion, even at low audio frequencies. This method of filtering also gives a fast AGC settling time which is advantageous for electronic search tuning. The AGC settling time can be further reduced by using capacitors of smaller value in the external filter. The AGC voltage is fed to the RF and IF stages via suitable AGC delays. The capacitor at pin 7 can be omitted for low-cost applications.

Field strength indicator output

A buffered voltage source provides a high-level field strength output signal which has good linearity for logarithmic input signals over the whole dynamic range. If field strength information is not needed, $R_{L(9)}$ can be omitted.

FUNCTIONAL DESCRIPTION (continued)

Standby switch

This switch is primarily intended for AM/FM band switching. During standby mode the oscillator, mixer and demodulator are switched off.

Short-circuit protection

All pins have short-circuit protection to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	$V_P = V_{13-16}$	V_{13}	–	12	V
Input voltage					
pins 14-15		V_{14-15}	–	10	V
pins 14-16		V_{14-16}	–	V_P	V
pins 15-16		V_{15-16}	–	V_P	V
pins 14-16		V_{14-16}	–	–0.6	V
pins 15-16		V_{15-16}	–	–0.6	V
Input current (pins 14 and 15)		I_{14-15}	–	200	mA
Total power dissipation*		P_{tot}	–	300	mW
Operating ambient temperature range		T_{amb}	–40	+ 80	°C
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	+ 125	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	300 K/W
		160 K/W*

* Mounted on epoxiprint

CHARACTERISTICS

$V_P = V_{13-16} = 8.5$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz; $f_m = 400$ Hz; m = 30%; $f_{IF} = 460$ kHz; measured in test circuit of Fig.1; all measurements are with respect to ground (pin 16); unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 13)		V_{13}	7.5	8.5	10	V
Supply current (pin 13)		I_{13}	15	23	27	mA
RF stage and mixer						
Input voltage (DC value)		V_{14-15}	–	$V_P/2$	–	V
RF input impedance at $V_I < 300\ \mu V$		R_{14-15}	–	5.5	–	kΩ
		C_{14-15}	–	25	–	pF
RF input impedance at $V_I > 10$ mV		R_{14-15}	–	8	–	kΩ
		C_{14-15}	–	22	–	pF
IF output impedance		R_1	500	0	0	kΩ
		C_1	–	6	–	pF
Conversion transconductance before start of AGC		I_1/V_I	–	6.5	–	mA/V
Maximum IF output voltage, inductive coupling to pin 1, (peak-to-peak value)		$V_{1(p-p)}$	–	5	–	V
DC value of output current (pin 1) at $V_I = 0$ V		I_1	–	1.2	–	mA
AGC range of input stage			–	30	–	dB
RF signal handling capability: input voltage for THD = 3% at m = 80% (RMS value)		$V_{I(rms)}$	–	500	–	mV
Oscillator						
Frequency range		Δf	0.6	–	60	MHz
Oscillator amplitude (pins 11 to 12) (peak-to-peak value)		$V_{11-12(p-p)}$	–	130	150	mV
External load impedance		$R_{11-12(ext)}$	0.5	–	200	kΩ
External load impedance for no oscillation		$R_{11-12(ext)}$	–	–	60	Ω

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Ripple rejection at V_P = 100 mV (RMS value); f_p = 100 Hz ($RR = 20 \log [V_{13}/V_{11}]$)						
Source voltage for switching diodes (6 x V_{BE})		V_{11}	–	4.2	–	V
DC output current (for switching diodes)	$V_P = V_{13} \leqslant 9$ V	I_{11}	0	–	5	mA
Change of output voltage at ΔI_{11} = 20 mA (switch to maximum load)		ΔV_{11}	–	0.5	–	V
Buffered oscillator output						
DC output voltage		V_{10}	–	0.7	–	V
Output signal amplitude (peak-to-peak value)		$V_{10(p\text{-}p)}$	–	320	–	mV
Output impedance		R_{10}	–	170	–	Ω
Output current		$I_{10(peak)}$	–	–	–3	mA
IF, AGC and AF stages						
DC input voltage		$V_{3\text{-}4}$	–	2	–	V
IF input impedance		$R_{3\text{-}4}$	2.4	3.0	3.9	kΩ
		$C_{3\text{-}4}$	–	7	–	pF
IF input voltage for THD = 3% at m = 80%		$V_{3\text{-}4}$	–	90	–	mV
Voltage gain before start of AGC		$V_{3\text{-}4}/V_6$	–	68	–	dB
AGC range of IF stages: change of $V_{3\text{-}4}$ for 1 dB change of $V_{O(AF)}$; $V_{3\text{-}4(ref)}$ = 75 mV		$\Delta V_{3\text{-}4}$	–	55	–	dB
AF output voltage at $V_{3\text{-}4(IF)}$ = 50 μV		$V_{O(AF)}$	–	130	–	mV
AF output voltage at $V_{3\text{-}4(IF)}$ = 1 mV		$V_{O(AF)}$	–	310	–	mV
AF output impedance (pin 6)		$\lvert Z_O \rvert$	–	3.5	–	kΩ

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Indicator driver						
Output voltage at V_I = 0 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	–	20	150	mV
Output voltage at V_I = 500 mV	$R_{L(9)}$ = 2.7 kΩ	V_9	2.5	2.8	3.1	V
Load resistance		$R_{L(9)}$	2.7	–	–	kΩ
Standby switch						
Switching threshold at V_P = 7.5 to 18 V; T_{amb} = –40 to + 80 °C						
ON-voltage		V_2	0	–	2	V
OFF-voltage		V_2	3.5	–	20	V
ON-current	V_2 = 0 V	I_2	–	–	–200	μA
OFF-current	V_2 = 20 V	I_2	–	–	10	μA

OPERATING CHARACTERISTICS

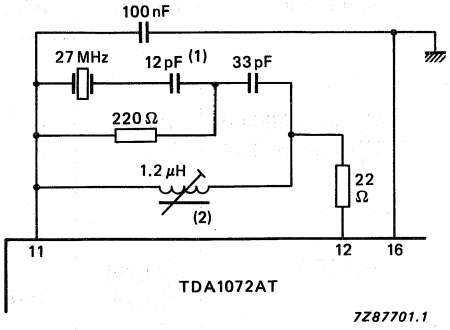
V_P = 8.5 V; f_I = 1 MHz; m = 30%; f_m = 400 Hz; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity						
RF input required for						
S+N/N = 6 dB		V_I	–	1.5	–	μV
S+N/N = 26 dB		V_I	–	15	–	μV
S+N/N = 46 dB		V_I	–	150	–	μV
RF input at start of AGC		V_I	–	30	–	μV
RF large signal handling						
RF input at						
THD = 3%; m = 80%		V_I	–	500	–	mV
THD = 3%; m = 30%		V_I	–	700	–	mV
THD = 10%; m = 30%		V_I	–	900	–	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
AGC range						
Change of V_I for						
1 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	86	–	dB
6 dB change of $V_{O(AF)}$	$V_{I(ref)}$ = 500 mV	ΔV_I	–	91	–	dB
Output signal						
AF output voltage at						
V_I = 4 μV	m = 80%	$V_{O(AF)}$	–	130	–	mV
V_I = 1 mV		$V_{O(AF)}$	240	310	390	mV
Total harmonic distortion at						
V_I = 1 mV	m = 80%	d_{tot}	–	0.5	–	%
V_I = 500 mV	m = 30%	d_{tot}	–	1	–	%
Signal-to-noise ratio	V_I = 100 mV	S+N/N	–	58	–	dB
Ripple rejection at						
V_I = 2 mV						
V_P = 100 mV (RMS value)						
f_p = 100 Hz						
(RR = 20 log [$V_P/V_{O(AF)}$])		RR	–	38	–	dB
Unwanted signals						
Suppression of IF whistles						
at V_I = 15 μV; m = 0%						
related to AF signal of						
m = 30%						
at $f_I \approx 2 \times f_{IF}$		α_{2IF}	–	37	–	dB
at $f_I \approx 3 \times f_{IF}$		α_{3IF}	–	44	–	dB
IF suppression at RF input						
for symmetrical input		α_{IF}	–	40	–	dB
for asymmetrical input		α_{IF}	–	40	–	dB
Residual oscillator signal						
at mixer output						
at f_{osc}		$I_{(osc)}$	–	1	–	μA
at 2 x f_{osc}		$I_{(2osc)}$	–	1.1	–	μA

APPLICATION INFORMATION



(1) Capacitor values depend on crystal type.
(2) Coil data: 9 windings of 0.1 mm dia laminated Cu wire on TOKO coil set 7K 199CN; Q_o = 80.

Fig.2 Oscillator circuit using quartz crystal; centre frequency = 27 MHz.

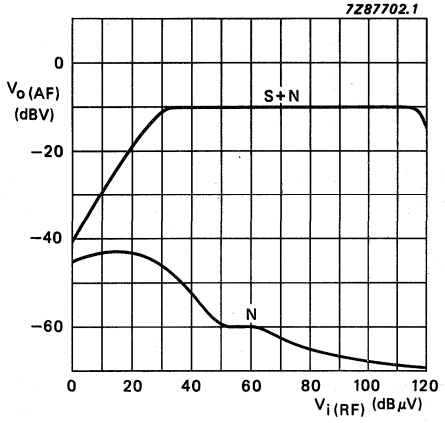


Fig.3 AF output as a function of RF input in the circuit of Fig.1; f_I = 1 MHz; f_m = 400 Hz; m = 30%.

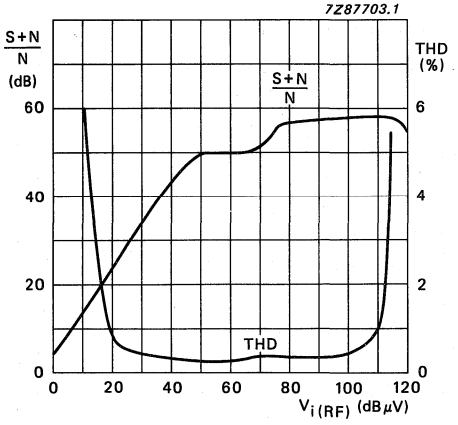


Fig.4 Total harmonic distortion and S+N/N as functions of RF input in the circuit of Fig.1; m = 30% for (S+N)/N curve and m = 80% for THD curve.

APPLICATION INFORMATION (continued)

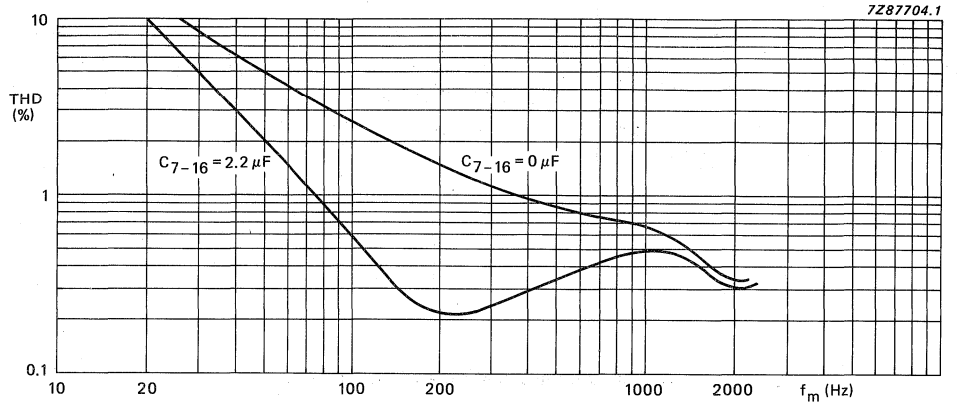


Fig.5 Total harmonic distortion as a function of modulation frequency at V_I = 5 mV; m = 80%; measured in the circuit of Fig.1 with $C_{7\text{-}16(ext)}$ = 0 μF and 2.2 μF.

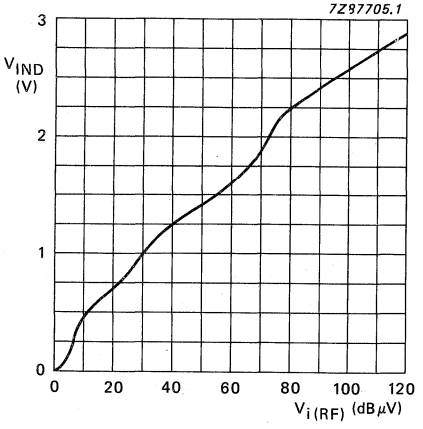
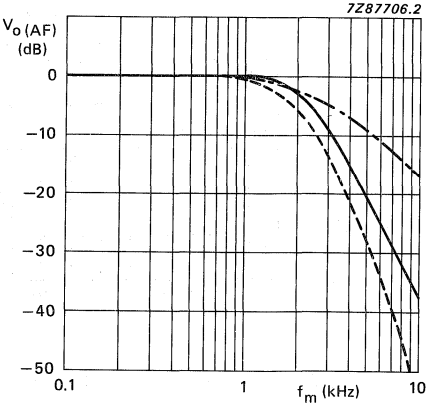


Fig.6 Indicator driver voltage as a function of RF input in the circuit of Fig.1.



—— with IF filter
—·— with AF filter
------ with IF and AF filter

Fig.7 Typical frequency response curves from Fig.1 showing the effects of filtering.

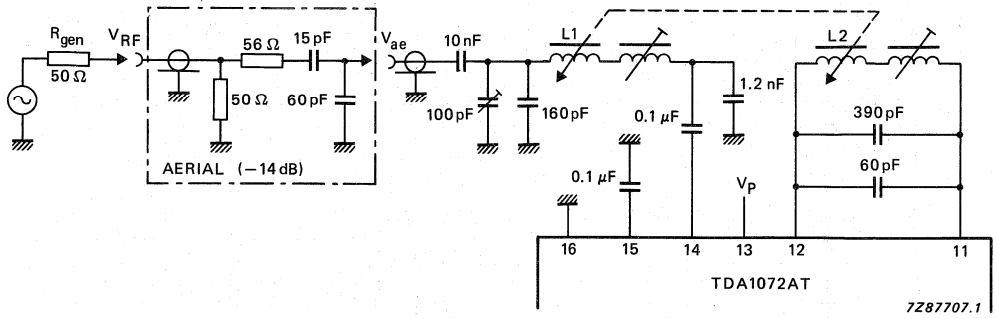


Fig.8 Car radio application with inductive tuning.

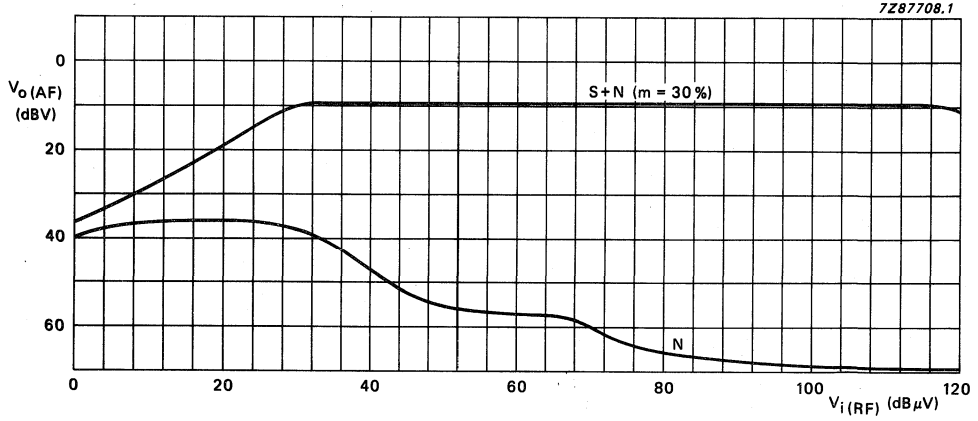


Fig.9 AF output as a function of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

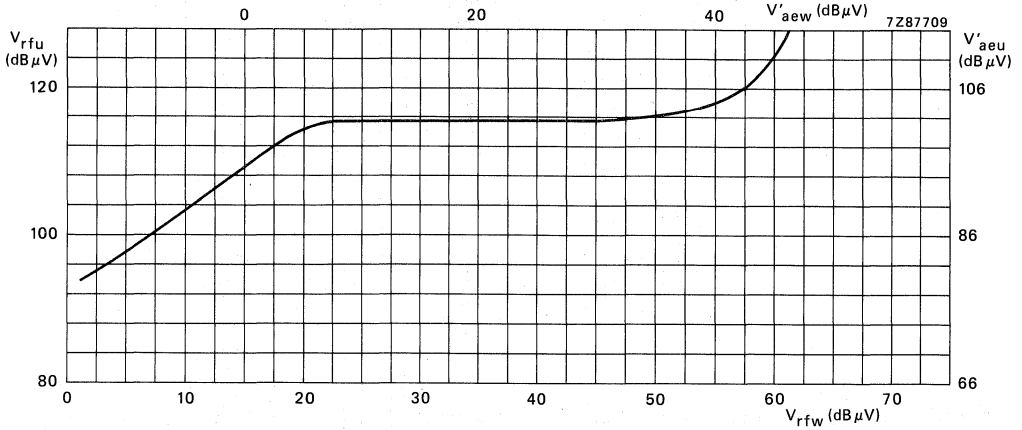


Fig.10 Suppression of cross-modulation as a function of input signal, measured in the circuit of Fig.8 with the input circuit as shown in Fig.11. Curve is for wanted $V_{O(AF)}$/unwanted $V_{O(AF)}$ = 20 dB; V_{rfw}, V_{rfu} are signals at the aerial input, V'_{aew}, V'_{aeu} are signals at the unloaded output of the aerial.

Wanted signal (V'_{aew}, V_{rfw}): f_i = 1 MHz; f_m = 400 Hz; m = 30%.

Unwanted signal (V'_{aeu}, V_{rfu}): f_i = 900 kHz; f_m = 400 Hz; m = 30%.

Effective selectivity of input tuned circuit = 21 dB.

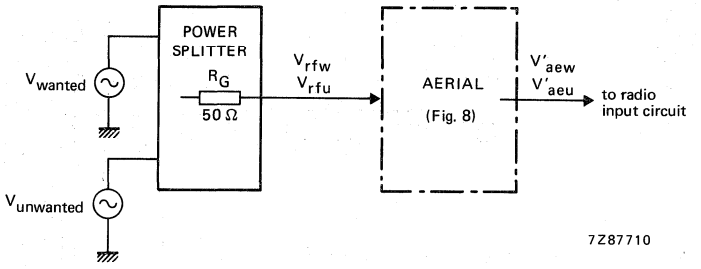


Fig.11 Input circuit to show cross-modulation suppression (see Fig.10).

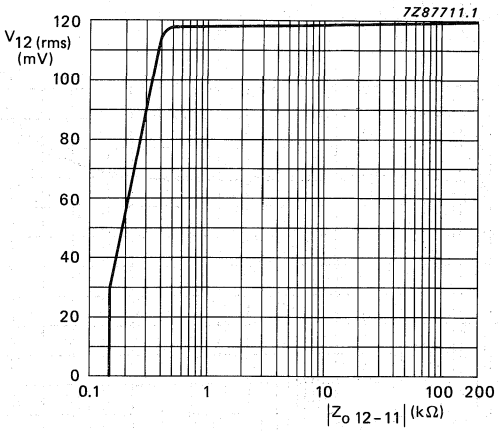


Fig.12 Oscillator amplitude as a function of the impedance at pins 11 and 12 in the circuit of Fig.8.

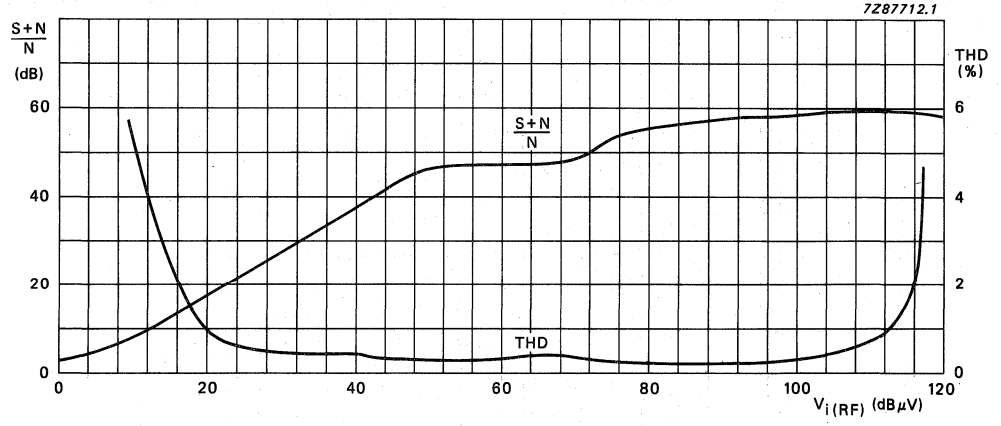


Fig.13 Total harmonic distortion and (S+N)/N as functions of RF input using the circuit of Fig.8 with that of Fig.1.

APPLICATION INFORMATION (continued)

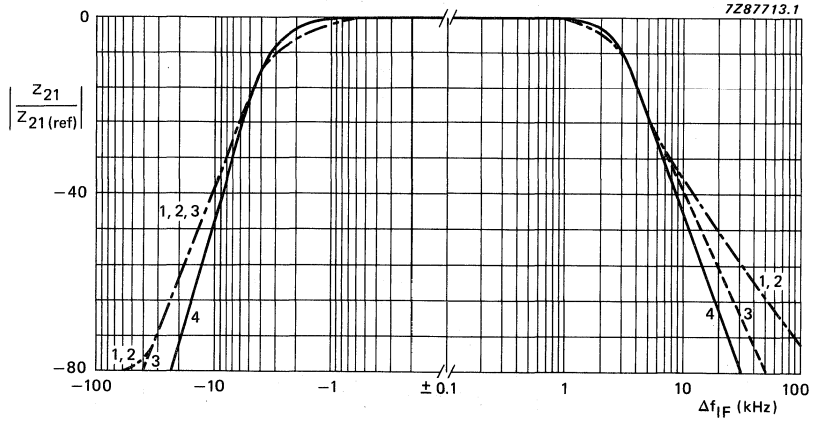


Fig.14 Forward transfer impedance as a function of intermediate frequency for filters 1 to 4 shown in Fig.14; centre frequency = 455 kHz.

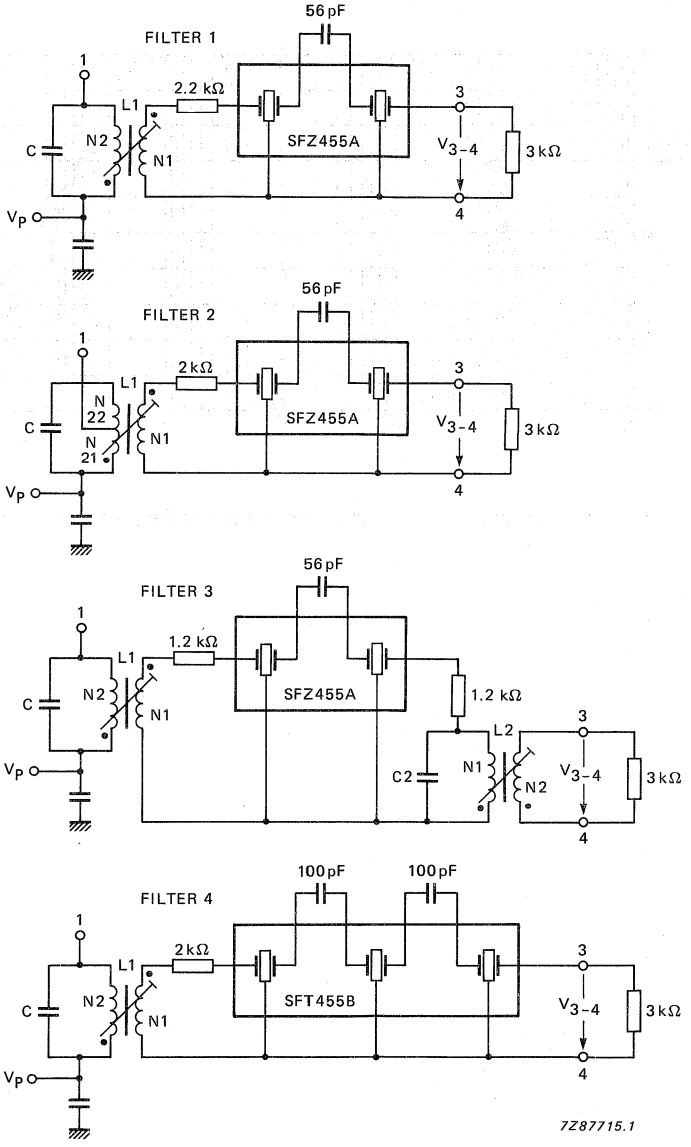
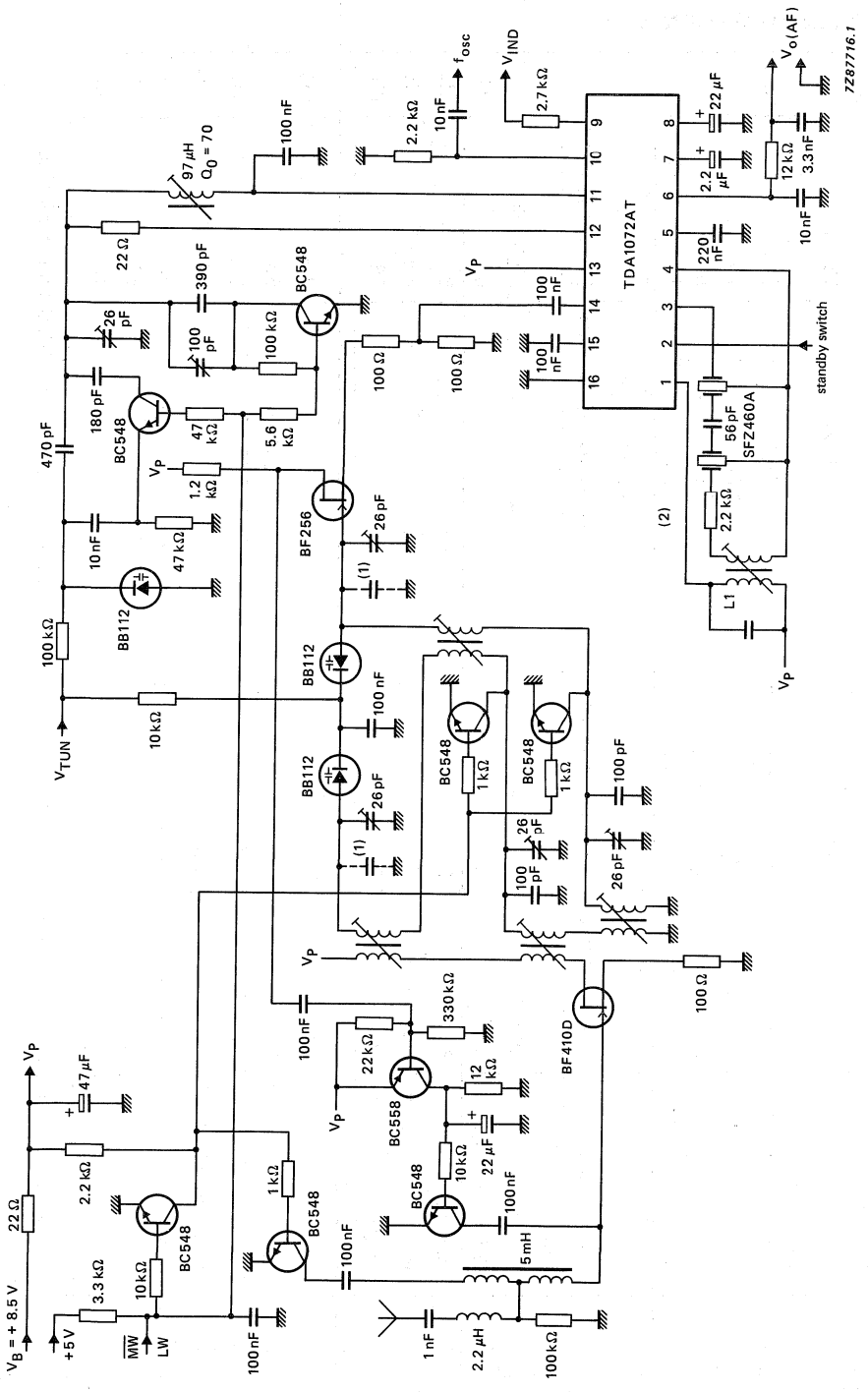


Fig.15 IF filter variants applied to the circuit of Fig.1; for filter data refer to Table 1.

filter no.	1	2	3		4	unit
Coil data	L1	L1	L1	L2	L1	
Value of C	3900	430	3900	4700	3900	pF
N1: N2	12 : 32	13 : (33 + 66)	15 : 31	29 : 29	13 : 31	
Diameter of Cu laminated wire	0.09	0.08	0.09	0.08	0.09	mm
Q_o	65 (typ.)	50	75	60	75	
Schematic* of windings	● ● 12 ● 32 ● ●	● ● 13 ● 33 = ● ●	● ● 15 ● 31 ● ●	● ● 29 ● 29 ● ● (N1) (N2)	● ● 13 ● 31 ● ●	
Toko order no.	7XNS-A7523DY	L7PES-A0060BTG	7XNS-A7518DY	7XNS-A7521AIH	7XNS-A7519DY	
Resonators						
Murata type	SFZ455A	SFZ455A	SFZ455A		SFT455B	
D (typical value)	4	4	4		6	dB
R_G, R_L	3	3	3		3	kΩ
Bandwidth (−3 dB)	4.2	4.2	4.2		4.5	kHz
S_{9kHz}	24	24	24		38	dB
Filter data						
Z_I	4.8	3.8	4.2		4.8	kΩ
Q_B	57	40	52 (L1)	18 (L2)	55	
Z_F	0.70	0.67	0.68		0.68	kΩ
Bandwidth (−3 dB)	3.6	3.8	3.6		4.0	kHz
S_{9kHz}	35	31	36		42	dB
S_{18kHz}	52	49	54		64	dB
S_{27kHz}	63	58	66		74	dB

* The beginning of an arrow indicates the beginning of a winding; N1 is always the inner winding. N2 the outer winding.

Table 1 Data for IF filters shown in Fig.15. Criterium for adjustment is Z_F = maximum (optional selectivity curve at centre frequency f_o = 455 kHz). See also Fig.14.



(1) Values of capacitors depend on the selected group of capacitive diodes BB112.

(2) For IF filter and coil data refer to Fig.1.

Fig.18 Car radio application with capacitive diode tuning and electronic MW/LW switching. The circuit includes pre-stage AGC optimised for good large-signal handling.

DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both 'ends' of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20	V
Supply current (pin 11)	I_P	typ.	22	mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6	V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6	V
Total harmonic distortion	THD	typ.	0,05	%
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50	μV
Control range	$\Delta\alpha$	typ.	110	dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80	dB
Ripple rejection (100 Hz)	α_{100}	typ.	46	dB
Tracking of ganged potentiometers	ΔG_v	typ.	0,5	dB
Supply voltage range	V_P		7,5 to 23	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

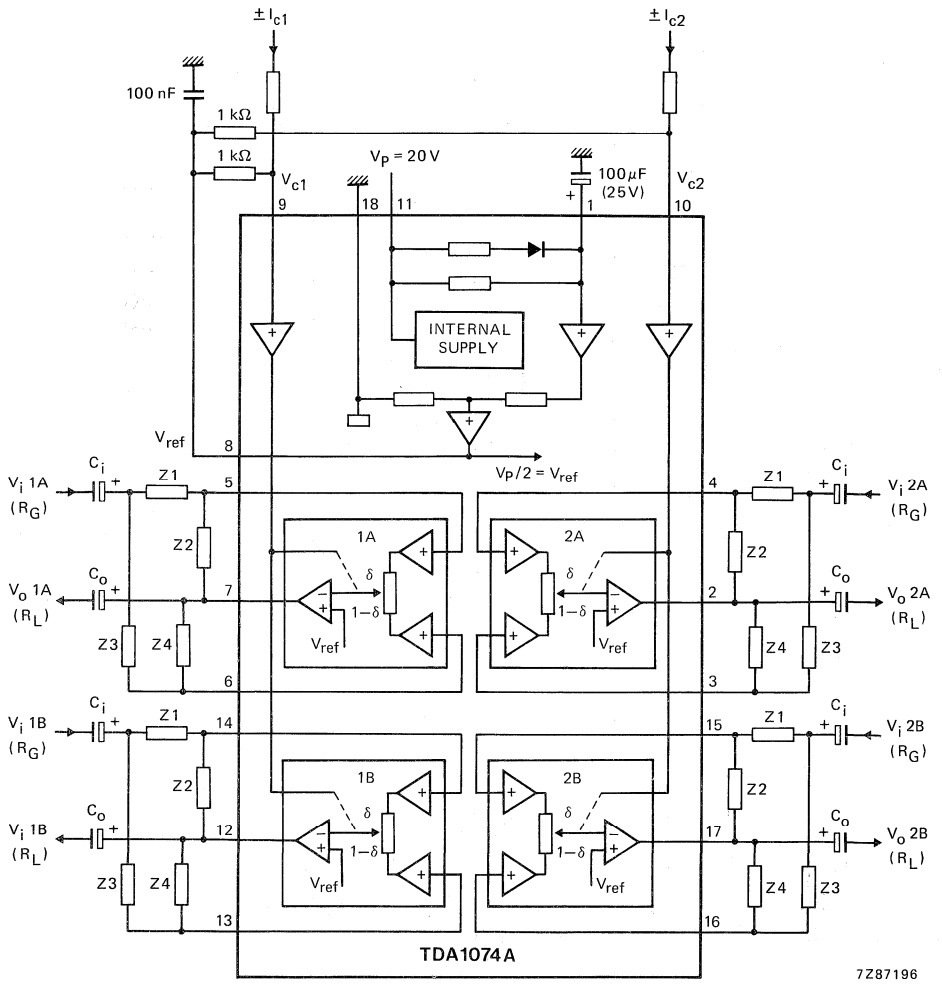


Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; Z1 = Z2 = Z3 = Z4 = 22 kΩ; the input generator resistance R_G = 60 Ω; the output load resistance R_L = 4,7 kΩ; the coupling capacitors at the inputs and outputs are C_i = 2,2 µF and C_o = 10 µF respectively.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23	V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1	V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i	0 to	V_P	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to +	150	°C
Operating ambient temperature range	T_{amb}	−30 to +	80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

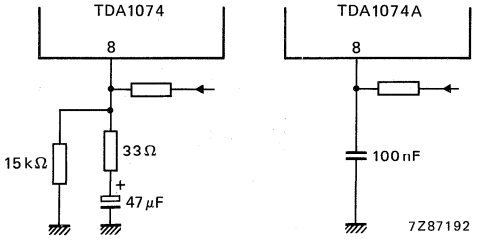


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; $R_L > 4{,}7$ kΩ; $C_L < 30$ pF; f = 1 kHz; with a linear frequency response ($V_{c1} = V_{c2} = 0$ V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) $V_{c1} = V_{c2} = 0$ V	f	10	–	20 000	Hz
Voltage gain at linear frequency response ($V_{c1} = V_{c2} = 0$ V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at $\pm V_{c1} = \pm V_{c2} = 120$ mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{c2} = 120$ mV		–	17,5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2} = 120$ mV		–	17,5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{c1} = 120$ mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1} = 120$ mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)} = 300$ mV					
f = 1 kHz (measured selectively)	THD	–	0,002	–	%
f = 20 Hz to 20 kHz	THD	–	0,005	–	%
at $V_{o(rms)} = 5$ V					
f = 1 kHz	THD	–	0,015	0,1	%
f = 20 Hz to 20 kHz	THD	–	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i;o(rms)}$	5,5	6,2	–	V
Power bandwidth at reference level $V_{o(rms)} = 5$ V (−3 dB); THD = 0,1%	B	–	40	–	kHz
Output noise voltages					
signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	–	86	–	dB
f = 20 Hz to 20 kHz	α_{ct}	–	80	–	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	–	20	–	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	–	46	–	dB

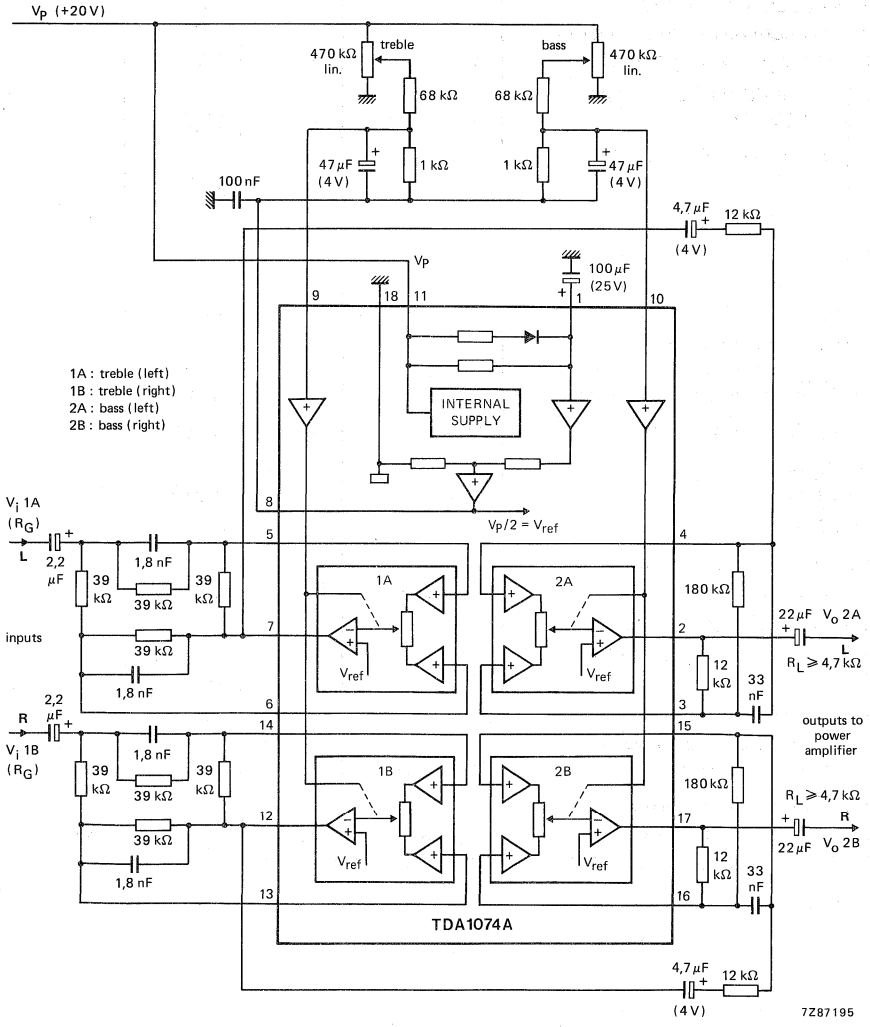


Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

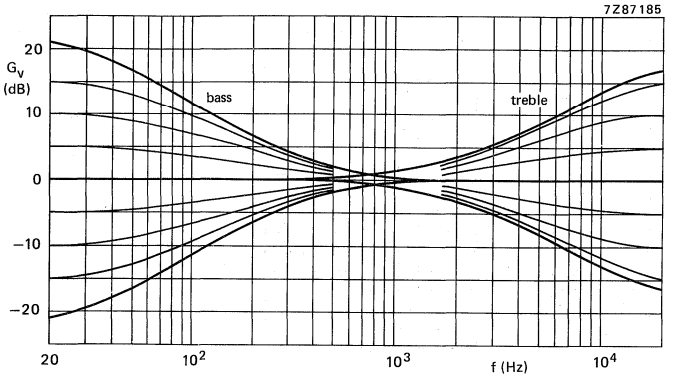


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

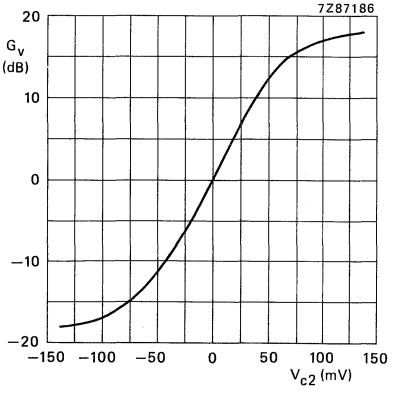


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

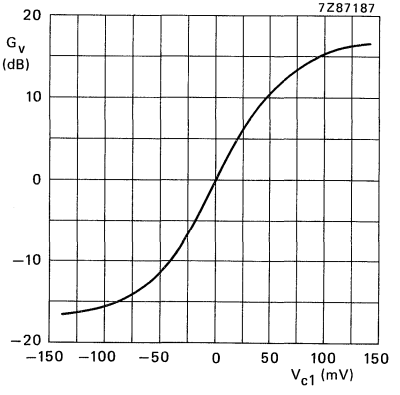
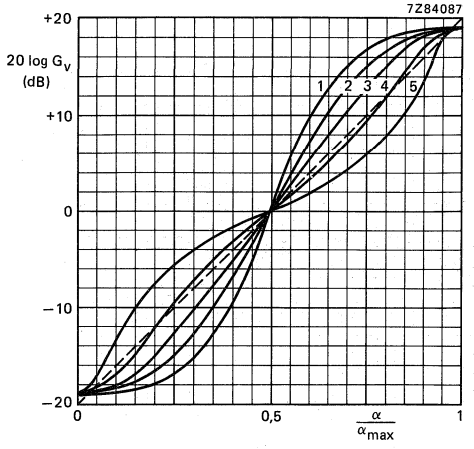


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

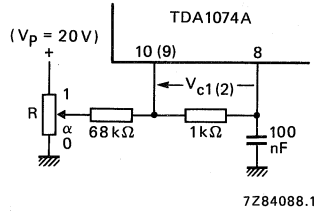


Fig. 8 Circuit diagram for measuring curves in Fig. 7.

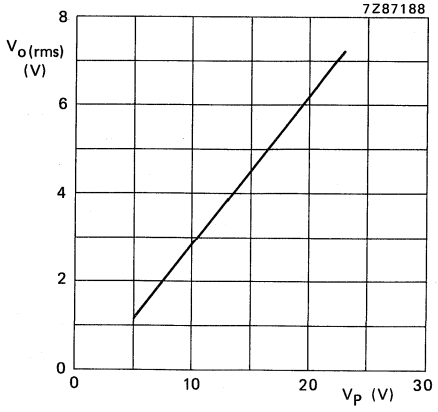


Fig. 9 Output signal level as a function of V_P; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

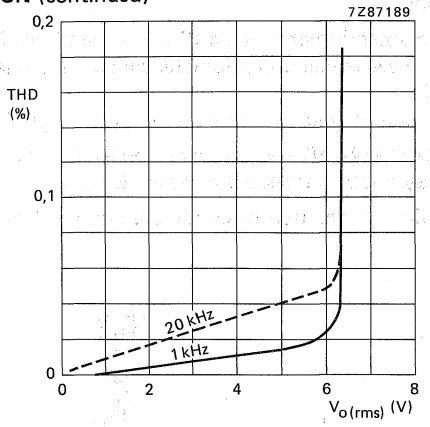


Fig. 10 Total harmonic distortion as a function of the output level; V_P = 20 V; R_L = 4,7 kΩ; $V_{c1} = V_{c2}$ = 0 V (linear, $G_{v\,tot}$ = 1). ——— f = 1 kHz; — — — — f = 20 kHz.

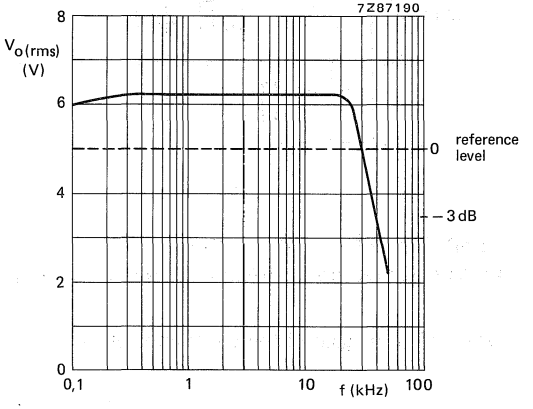


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

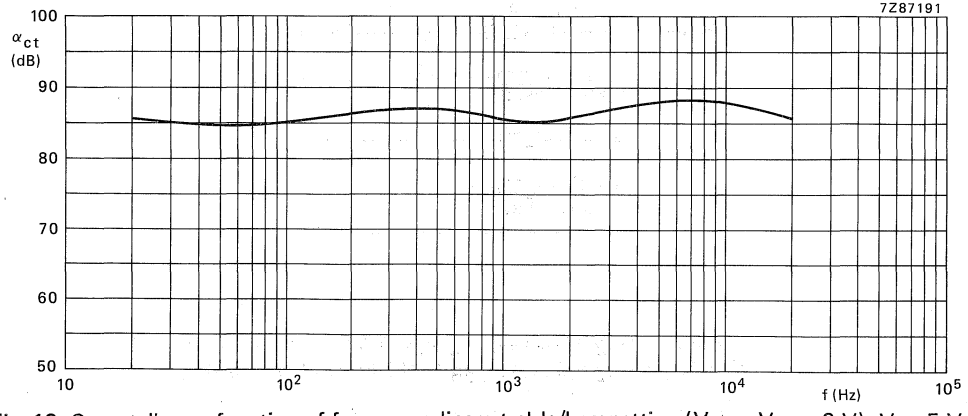
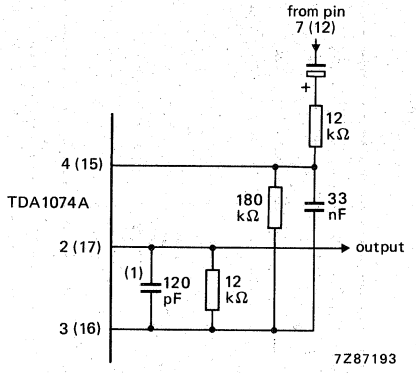


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1} = V_{c2}$ = 0 V); V_i = 5 V; R_G = 60 Ω; R_L = 4,7 kΩ.

Application recommendations

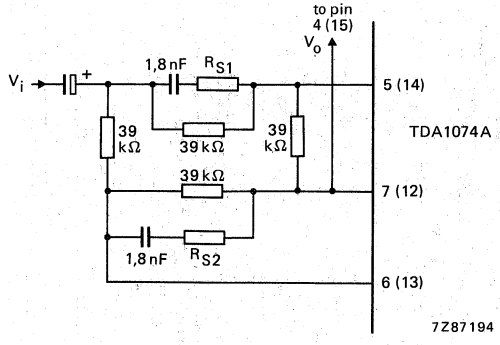
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8 (V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.



(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.



For $R_{S1} = R_{S2}$ = 3,3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

24 W BTL OR 2 × 12 W STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1510AQ is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6 Ω). With a supply voltage (V_P) of 14,4 V, an output power of 24 W can be delivered into a 4 Ω Bridge Tied Load (BTL), or when used as a stereo amplifier, 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Features

- Flexibility – stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range:						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	28,0	V
non-operating, load dump protection		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current		I_{so}	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$\lvert Z_I \rvert$	1	–	–	MΩ
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

TDA1510AQ: 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

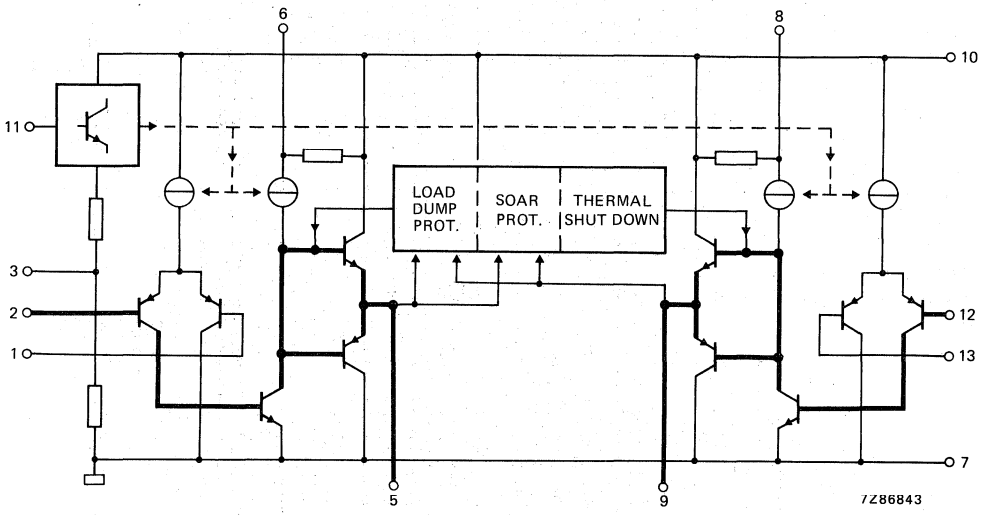


Fig. 1 Functional diagram; heavy lines indicate signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage:					
operating	pin 10	V_P	–	18	V
non-operating		V_P	–	28	V
non-operating, load dump protection	during 50 ms	V_P	–	45	V
Peak output current		I_{OM}	–	6	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Crystal temperature		T_c	–	+ 150	°C

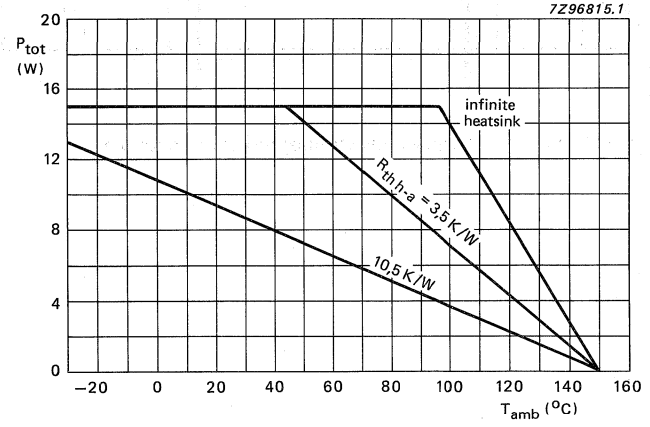


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

$(R_{th\ j\text{-}mb}) = 3{,}5$ K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3{,}5 = 3{,}5\ \text{K/W}$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
$T_{amb} = 65\ ^{o}C$ (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3{,}5 = 10{,}5\ \text{K/W}$$

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	6,0	14,4	18,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current	$V_{11} \leqslant V_{10}$; note 1	I_{so}	0,15	0,35	0,80	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

parameter	parameter	symbol	min.	typ.	max.	unit
Bridge Tied Load application (BTL)						
Output power with bootstrap	note 6; R_L = 4 Ω					
	V_P = 13,2 V					
	d_{tot} = 0,5%	P_o	–	15,0	–	W
	d_{tot} = 10%	P_o	–	20,0	–	W
	V_P = 14,4 V					
	d_{tot} = 0,5%	P_o	15,5	18,0	–	W
	d_{tot} = 10%	P_o	20,0	24,0	–	W
Open loop voltage gain		G_o	–	75	–	dB
Closed loop voltage gain	note 2	G_c	39,5	40,0	40,5	dB
Frequency response	at –3 dB; note 3	f_r	–	20 to > 20 k	–	Hz
Input impedance	note 4	$\|Z_i\|$	1	–	–	MΩ
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz					
	R_S = 0 Ω	$V_{n\ (rms)}$	–	0,2	–	mV
	R_S = 10 kΩ	$V_{n\ (rms)}$	–	0,35	0,8	mV
	R_S = 10 kΩ; according to IEC 179 curve A	$V_{n\ (rms)}$	–	0,25	–	mV
Supply voltage ripple rejection	f = 100 Hz; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$\|\Delta V_{5\text{-}9}\|$	–	2	50	mV
Power bandwidth	–1 dB; d_{tot} = 0,5%	B	–	30 to > 40 k	–	Hz

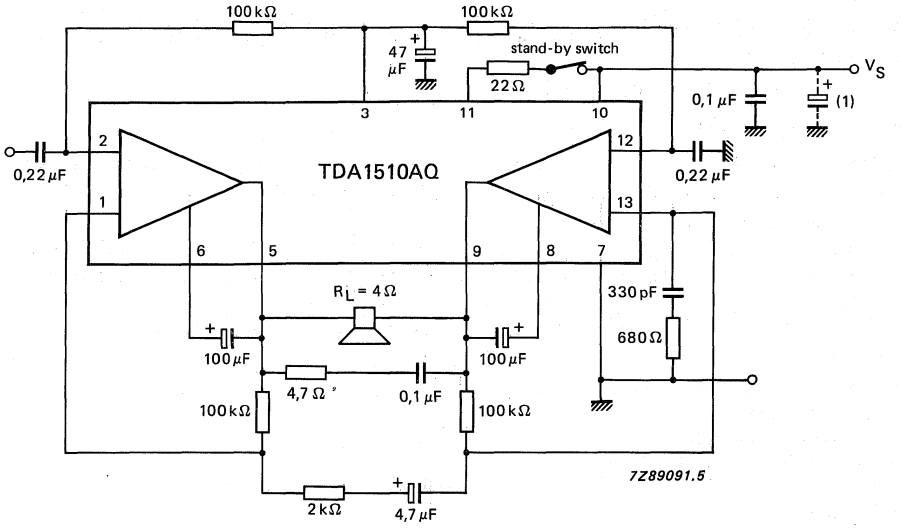
A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power; with bootstrap	note 6; $R_L = 4\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	4,5	–	W
	$d_{tot} = 10\%$	P_o	–	6,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	4,5	5,5	–	W
	$d_{tot} = 10\%$	P_o	6,0	7,0	–	W
	$R_L = 2\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	7,5	–	W
	$d_{tot} = 10\%$	P_o	–	10,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	7,75	9,0	–	W
	$d_{tot} = 10\%$	P_o	10,0	12,0	–	W
Output power; without bootstrap	notes 6, 8 and 9 $R_L = 4\ \Omega$ $V_P = 14{,}4$ V					
	$d_{tot} = 10\%$	P_o	–	6	–	W
Frequency response	notes 3 and 6					
	−3 dB	f_r	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	f = 1 kHz	SVRR	–	50	–	dB
Channel separation	$R_S = 10\ k\Omega$;					
	f = 1 kHz	α	40	50	–	dB
Closed loop voltage gain	note 7	G_c	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz;					
	$R_S = 0\ \Omega$	$V_{n(rms)}$	–	0,15	–	mV
	$R_S = 10\ k\Omega$	$V_{n(rms)}$	–	0,25	–	mV
	$R_S = 10\ k\Omega$; according to IEC179 curve A	$V_{n(rms)}$	–	0,2	–	mV

Notes to the characteristics

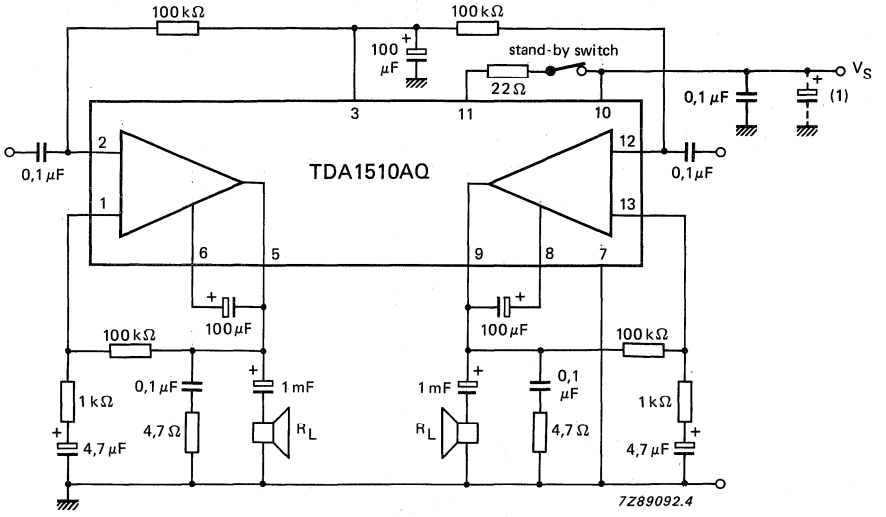
1. If $V_{11} > V_{10}$ then I_{11} must be < 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 and the 100 μF capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.

APPLICATION INFORMATION



(1) belongs to power supply

Fig. 3 Test and application circuit; Bridge Tied Load (BTL).



(1) belongs to power supply

Fig. 4 Test and application circuit; stereo mode.

50 W HIGH- PERFORMANCE HI-FI AMPLIFIER

GENERAL DESCRIPTION

The TDA1514A integrated circuit is a hi-fi power amplifier for use as a building block in radio, tv and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).
The circuit is totally protected, the two output transistors both having thermal and SOAR protection (see Fig.3). The circuit also has a mute function that can be arranged for a period after power-on with a delay time fixed by external components.
The device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features

- High output power
- Low harmonic distortion
- Low intermodulation distortion
- Low offset voltage
- Good ripple rejection
- Mute/stand-by facilities
- Thermal protection
- Protected against electrostatic discharge
- No switch-on or switch-off clicks
- Very low thermal resistance
- Safe Operating Area (SOAR) protection

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Total quiescent current	V_P = ± 27.5 V	I_{tot}	–	56	–	mA
Output power	THD = –60 dB; V_P = ± 27.5 V; R_L = 8 Ω	P_o	–	40	–	W
	V_P = ± 23 V; R_L = 4 Ω	P_o	–	48	–	W
Closed loop voltage gain	determined externally	G_c	–	30	–	dB
Input resistance	determined externally	R_i	–	20	–	kΩ
Signal plus noise-to-noise ratio	P_o = 50 mW	(S+N)/N	–	83	–	dB
Supply voltage ripple rejection	f = 100 Hz	SVRR	–	64	–	dB

PACKAGE OUTLINE

9-lead SIL, plastic power (SOT131R).

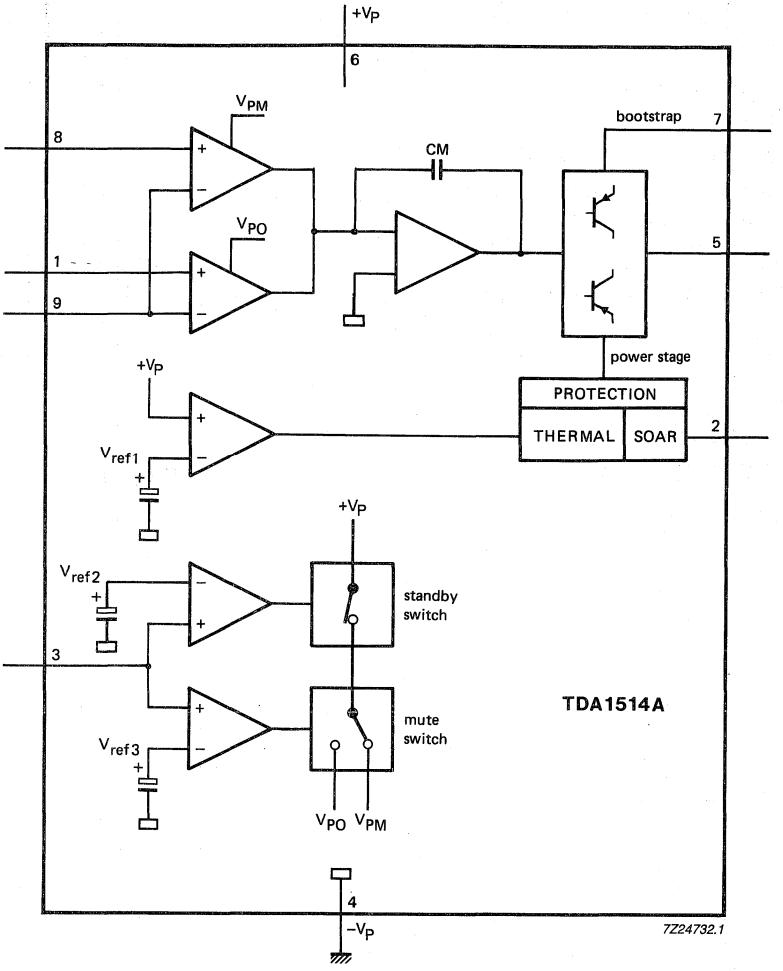


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 4)	V_P	–	±30	V
Bootstrap voltage (pin 7 to pin 4)	V_{bstr}	–	70	V
Output current (repetitive peak)	I_o	–	8	A
Operating ambient temperature range	T_{amb}	see Fig.2		
Storage temperature range	T_{stg}	–55	+150	°C
Power dissipation		see Fig.2		
Thermal shut-down protection time	t_{pr}	–	1	hour
Mute voltage (pin 3 to pin 4)	V_m	–	7.25	V

THERMAL RESISTANCE

From junction to mounting base $R_{th\ j\text{-}mb}$ 1 K/W

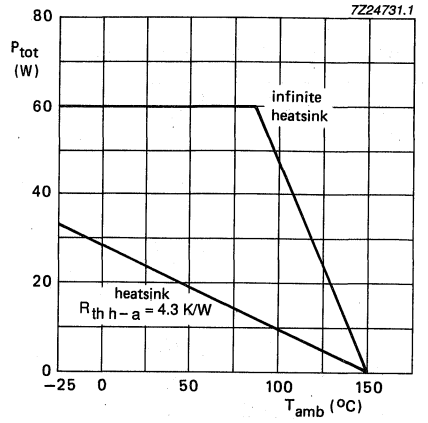


Fig.2 Power derating curve.

The theoretical maximum power dissipation for P_o = 40 W with a stabilized power supply is:

$$\frac{V_P^2}{2\pi^2 R_L} = 19\ W;\ \text{where}\ V_P = \pm 27.5\ V;\ R_L = 8\ \Omega$$

Considering, for example, a maximum ambient temperature of 50 °C and a maximum junction temperature of 150 °C the total thermal resistance is:

$$R_{th\ j\text{-}a} = \frac{150 - 50}{19} = 5.3\ K/W$$

Since the thermal resistance of the SOT131A encapsulation is $R_{th\ j\text{-}mb} < 1$ K/W, the thermal resistance required of the heatsink is $R_{th\ h\text{-}a} < 4.3$ K/W.

SAFE OPERATING AREA (SOAR) PROTECTION

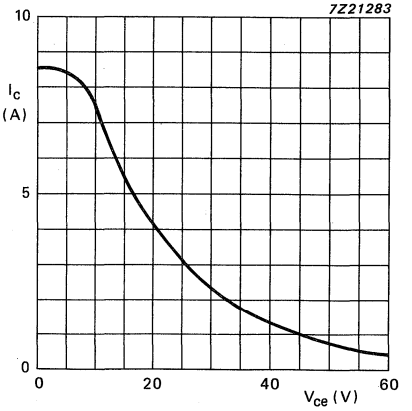


Fig.3 SOAR protection curve.

CHARACTERISTICS

V_P = ± 27.5 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; test circuit as Fig.4; unless otherwise specified.

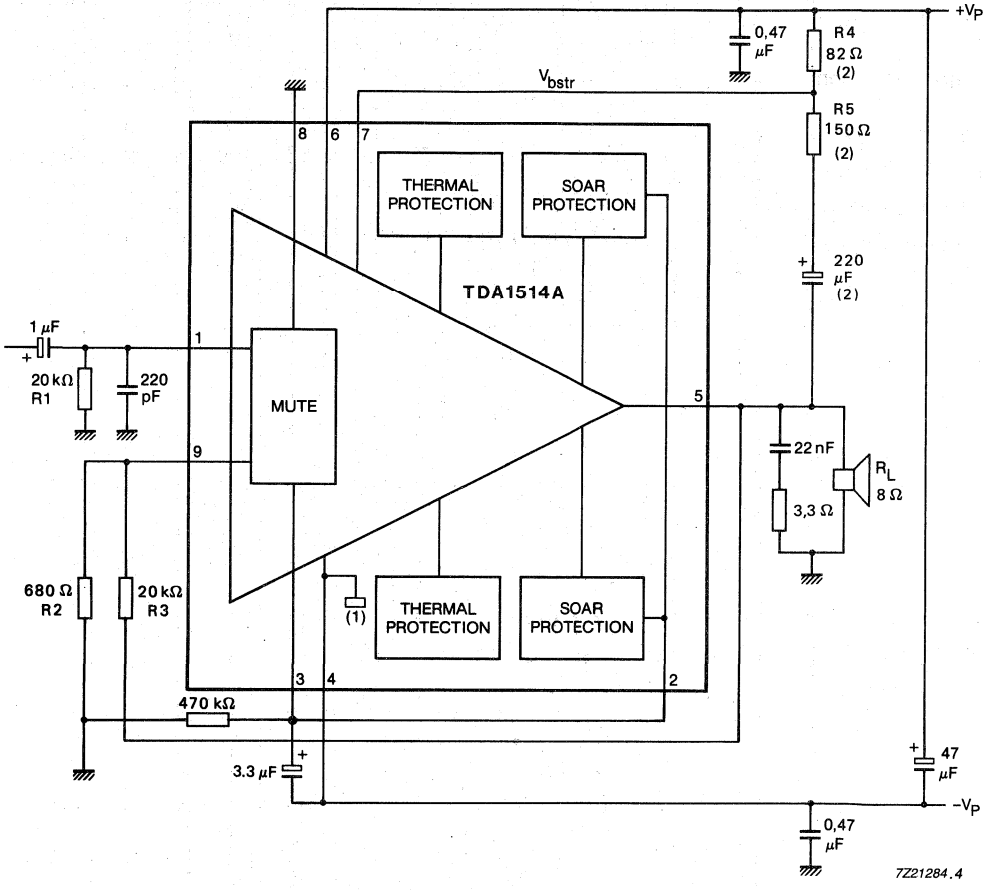
parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6 to pin 4)		V_P	± 10	–	± 30	V
Maximum output current (peak value)		$I_{OM\,max}$	6.4	–	–	A
Operating state						
Voltage (pins 3 to 4)		V_{3-4}	6	–	7.25	V
Total quiescent current	$R_L = \infty$	I_{tot}	30	56	90	mA
Output power	THD = –60 dB	P_o	37	40	–	W
	THD = –20 dB	P_o	–	51	–	W
Output power	V_P = ± 23 V; THD = –60 dB					
	R_L = 8 Ω	P_o	–	28	–	W
	R_L = 4 Ω	P_o	–	48	–	W
Total harmonic distortion	P_o = 32 W	THD	–	–90	–80	dB
Intermodulation distortion	P_o = 32 W note 1	d_{im}	–	–86	–	dB
Power bandwidth	(–3 dB); THD = –60 dB	B	–	20 to 25 000		Hz
Slew rate		dV/dt	–	14	–	V/μs
Closed loop voltage gain	note 2	G_c	–	30	–	dB
Open loop voltage gain		G_o	–	89	–	dB
Input impedance	note 3	$\|Z_i\|$	1	–	–	MΩ
Signal-to-noise ratio	note 4 P_o = 50 mW	S/N	80	83	–	dB
Output offset voltage		V_o	–	7	200	mV
Input bias current		I_I	–	0.1	1.0	μA
Output impedance		$\|Z_o\|$	–	–	0.1	Ω
Supply voltage ripple rejection	note 5	SVRR	58	64	–	dB
Quiescent current into pin 2	note 6	I_2	–	0.1	–	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute state						
Voltage on pin 3		V_{3-4}	2	–	4.5	V
Offset voltage		V_o	–	30	200	V
Output voltage	$V_{i(rms)}$ = 1 V f = 1 kHz	V_o	–	450	–	μV
Ripple rejection	note 5	RR	–	60	–	dB
Standby state						
Voltage on pin 3		V_{3-4}	0	–	0.9	V
Total quiescent current		I_{tot}	–	18	25	mA
Ripple rejection	notes 5 and 7	RR	–	60	–	dB
Supply voltage to obtain standby state		$\pm V_P$	5.0	–	7.0	V

Notes to the characteristics

1. Measured with two superimposed signals of 50 Hz and 7 kHz with an amplitude relationship of 4 : 1.
2. The closed loop gain is determined by external resistors (Fig.4, R2 and R3) and is variable between 20 and 46 dB.
3. The input impedance in the test circuit (Fig.4) is determined by the bias resistor R1.
4. The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistance of 2 kΩ.
5. f = 100 H_3; R_S = 2 kΩ; ripple voltage = 500 $mV_{(eff)}$ on positive and negative supply.
6. The quiescent current into pin 2 has an impact on the mute time.
7. Without bootstrap.



(1) Mounting base connected to $-V_P$.

(2) When used without a bootstrap these components are disconnected and pin 6 is connected to pin 7 thus decreasing the output power by approximately 4 W.

(3) When $R_L = 4\ \Omega$: R4 = 47 Ω and R5 = 82 Ω.

Fig.4 Application and test circuit.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515BQ is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use – mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 1 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- SOAR protection
- outputs short-circuit safe to ground in BTL
- reverse polarity safe

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	1	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\|Z_i\|$	>	1	MΩ
Bridge tied load application (BTL)	V_P	=	14,4 | 13,2	V
Output power at R_L = 4 Ω (with bootstrap)				
d_{tot} = 0,5%	P_o	typ.	18 | 15	W
d_{tot} = 10%	P_o	typ.	24 | 20	W
Supply voltage ripple rejection; R_S = 0 Ω; f = 100 Hz	RR	typ.	50 | 50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 | 50	mV
Stereo application				
Output power at d_{tot} = 10% (with bootstrap)				
R_L = 4 Ω	P_o	typ.	7 | 6	W
R_L = 2 Ω	P_o	typ.	12 | 10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)				
R_L = 4 Ω	P_o	typ.	5,5 | 4,5	W
R_L = 2 Ω	P_o	typ.	9 | 7,5	W
Channel separation	α	>	40 | 40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ.	0,2 | 0,2	mV

PACKAGE OUTLINE 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

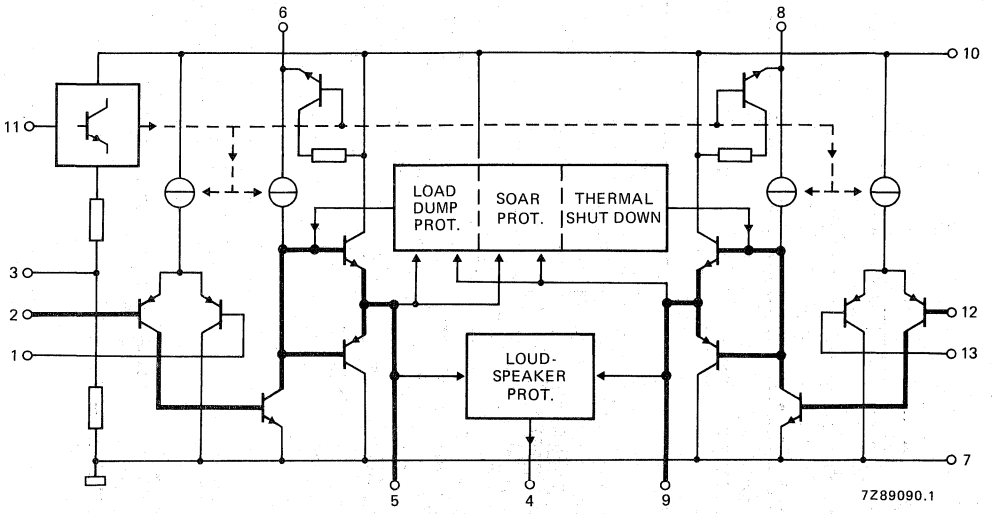


Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V
Reverse polarity		max.	10 V

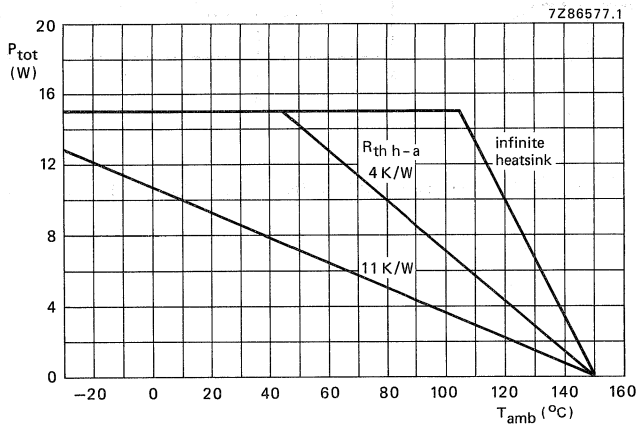


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)
maximum sine-wave dissipation: 12 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)
maximum sine-wave dissipation: 6 W
T_{amb} = 65 °C maximum

$$R_{th\ h-a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18 V
Repetitive peak output current	I_{ORM}	<	4 A
Total quiescent current	I_{tot}	typ.	75 mA
Switching level 11 : OFF	V_{11}	<	1,8 V
ON	V_{11}	>	3 V
Impedance between pins 10 and 6; 10 and 8 (stand-by position $V_{11} < 1,8$ V)	$\|Z_{OFF}\|$	>	100 kΩ
Stand-by current at V_{11} = 0 to 0,8 V	I_{sb}	typ.	1 μA
		<	100 μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ.	10 μA
		<	100 μA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)			
V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	>	15,5 W
		typ.	18 W
V_P = 14,4 V; d_{tot} = 10%	P_o	>	20 W
		typ.	24 W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15 W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20 W
Open loop voltage gain	G_o	typ.	75 dB
Closed loop voltage gain (note 2)	G_c	typ.	40 (± 0,5) dB
Output power without bootstrap (note 9)			
V_P = 14,4 V; d_{tot} = 10 %	P_o	typ.	15 W
V_P = 14,4 V; d_{tot} = 0,5 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 10 %	P_o	typ.	12 W
V_P = 13,2 V; d_{tot} = 0,5 %	P_o	typ.	9 W
Frequency response at −3 dB (note 3)	B		20 Hz to min. 20 kHz
Input impedance (note 4)	$\|Z_i\|$	>	1 MΩ
Noise input voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,35 mV
		<	0,8 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,25 mV
Supply voltage ripple rejection (note 5)			
f = 100 Hz	RR	>	42 dB
		typ.	50 dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5\text{-}9}\|$	<	50 mV
		typ.	2 mV
Loudspeaker protection (all conditions) maximum d.c. voltage (across the load)	$\|\Delta V_{5\text{-}9}\|$	<	1 V
Power bandwidth; −1 dB; **d_{tot} = 0,5%**	B		30 Hz to 40 kHz

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at d_{tot} = 0,5%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6, 8 and 9)	P_o	typ.	6 W
Frequency response at −3 dB (note 3)	B	40 Hz to min.	20 kHz
Supply voltage ripple rejection (note 5)	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC 179 curve A	V_n	typ.	0,2 mV

Notes

1. The internal circuit impedance at pin 11 is > 5 kΩ if $V_{11} > V_{10}$.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components. For further gain reduction see Application Report.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 (8 and 9) can be omitted. Pins 6, 8 and 10 have to be interconnected.

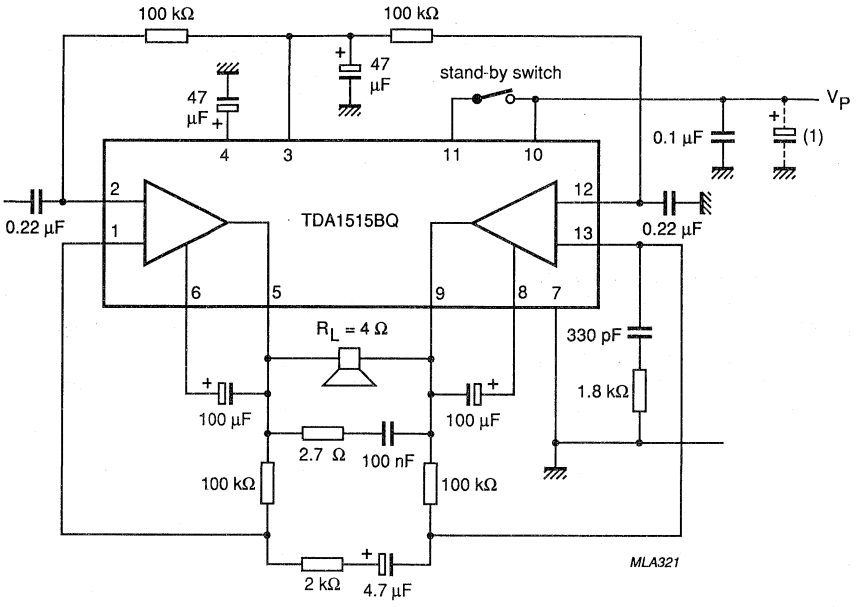


Fig. 3 Test/application circuit bridge tied load (BTL).

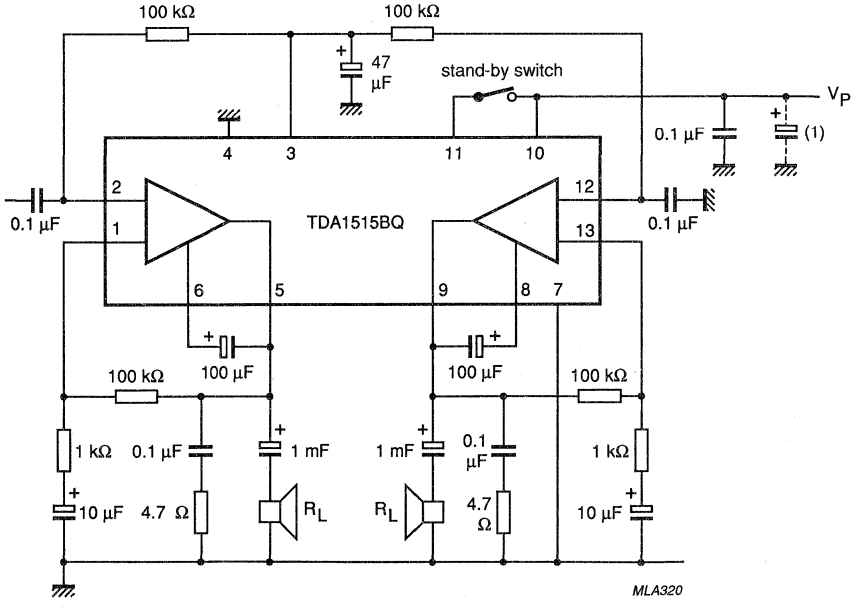


Fig. 4 Test/application circuit stereo.

1. Belongs to power supply.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1516BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use – stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1518Q (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	100	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

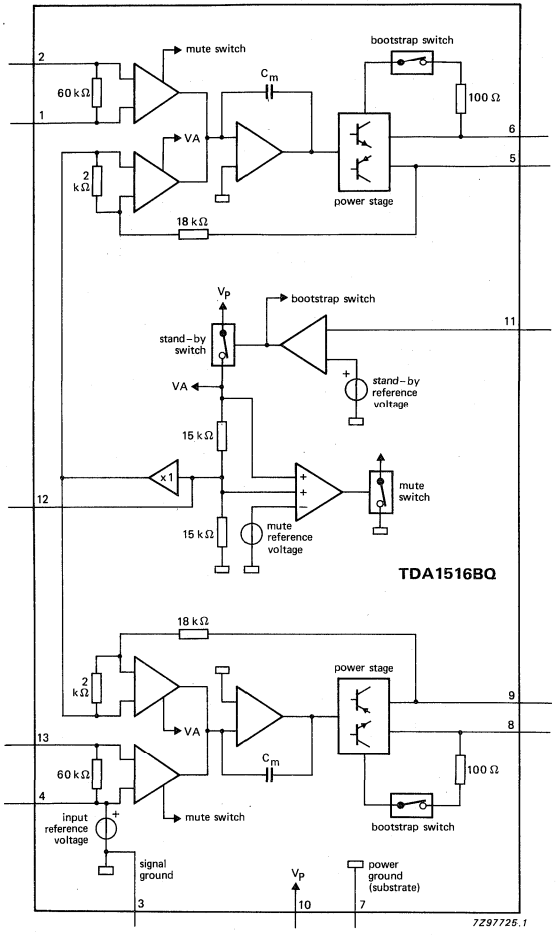


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1516BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+ 150	°C

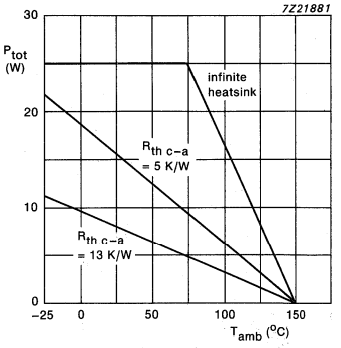


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	2	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7.5	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 9	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	–	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD =0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13,5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5% P_o = 15 W	B_W	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	25	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	100	200	μV
mute	note 9	$V_{no(rms)}$	–	60	–	μV

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,5 to 18 V.
3. At 18 V $< V_P <$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (Vp), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

APPLICATION INFORMATION

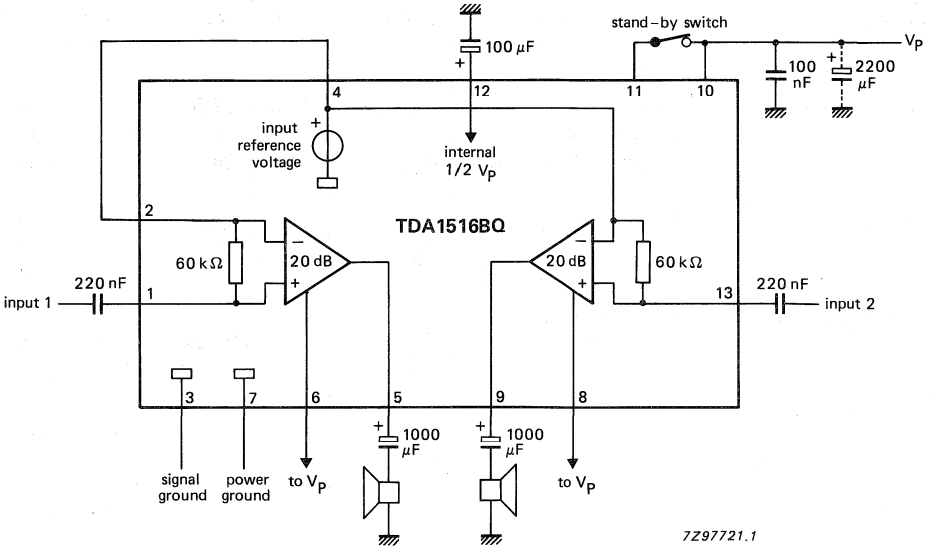


Fig. 3 Stereo application circuit diagram.

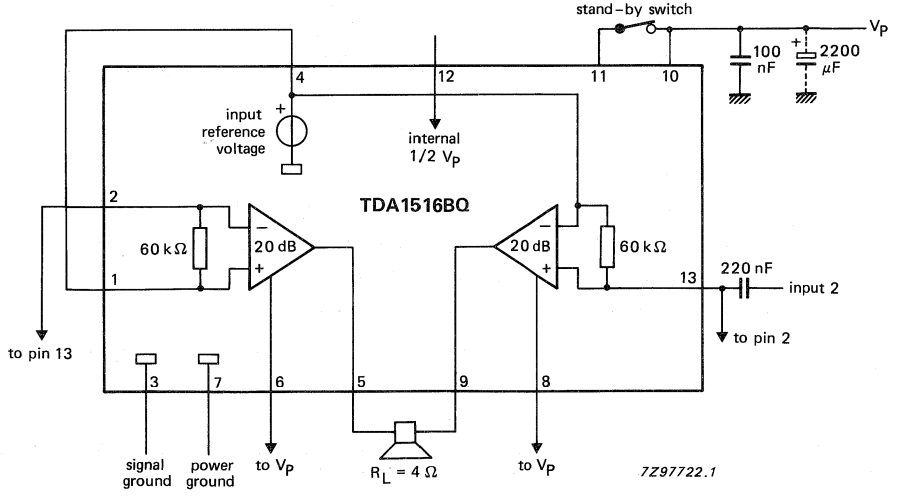


Fig. 4 BTL application circuit diagram (without bootstrapping).

22 W BTL car radio power amplifier TDA1516CQ

FEATURES

- Requires very few external components for Bridge-Tied-Load (BTL)
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA1516CQ is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range					
		operating	6.0	14.4	18	V
		non-operating	–	–	30	V
		load dump	–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	40	80	mA
I_{sb}	stand-by current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	60	μA
$\|Z_I\|$	input impedance BTL		25	–	–	kΩ
T_{XTAL}	crystal temperature		–	–	+150	°C
P_O	output power	THD = 10%; 4 Ω	–	22	–	W
SVRR	supply voltage ripple rejection	R_S = 0; f = 100 Hz	45	–	–	dB
		f = 1 to 10 kHz	48	–	–	dB
V_{no}	noise output voltage		–	70	–	μV
$\|\Delta V_{os}\|$	DC output offset voltage		–	–	100	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1516CQ	13	DIL	plastic	SOT141

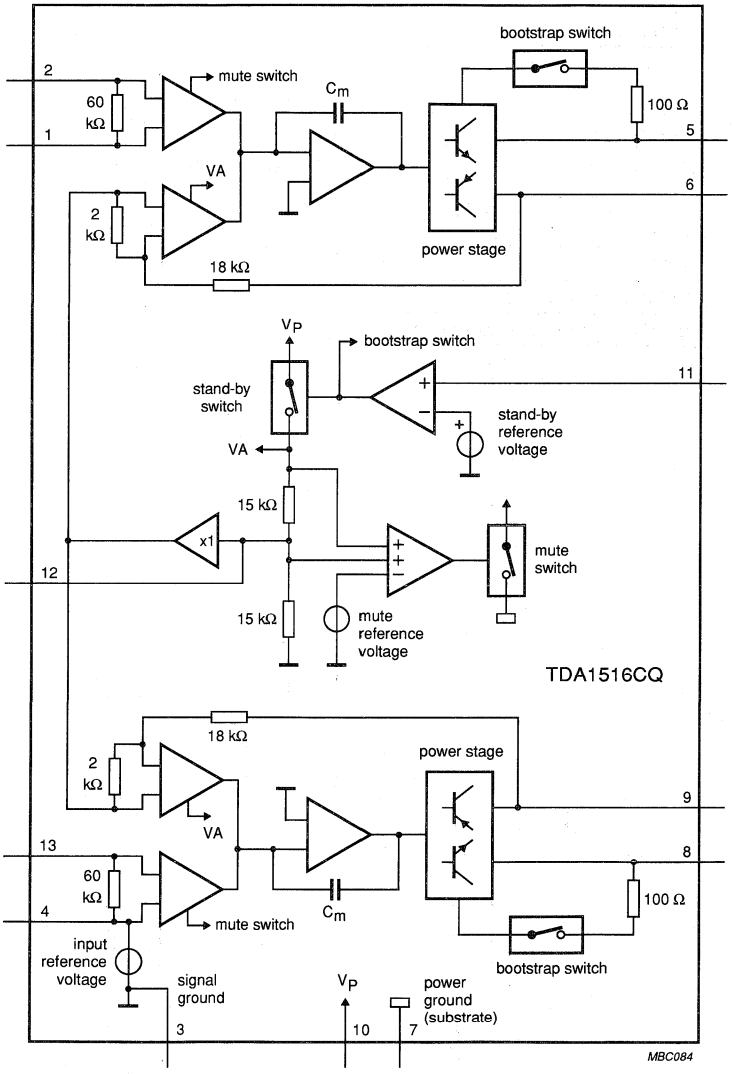


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
INV	2	inverting input
GND1	3	ground (signal)
V_{ref}	4	reference voltage
OUT1	5	output 1
BS1	6	bootstrap 1
GND2	7	ground (substrate)
BS2	8	bootstrap 2
OUT2	9	output 2
V_P	10	supply voltage
M/SB	11	mute/stand-by switch
RR	12	supply voltage ripple rejection
–INV2	13	non-inverting input 2

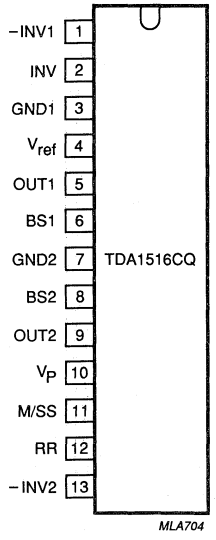


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1516CQ contains two identical amplifiers with differential input stages. It can be used for bridge applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch, which has the following features:

- low stand-by current (< 100 μA)
- low mute/stand-by switching current (low cost supply switch)
- mute condition.

LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
		operating	–	18	V
		non-operating	–	30	V
		load dump protected; during 50 ms; rise time ≥ 2.5 ms	–	45	V
V_{PSC}	AC and DC short-circuit safe voltage		–	18	V
V_{PR}	reverse polarity		–	6	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation	$T_{case} < 75$ °C; (see Fig.3)	–	25	W
T_{stg}	storage temperature range		−55	+150	°C
T_{vj}	virtual junction temperature		–	+150	°C

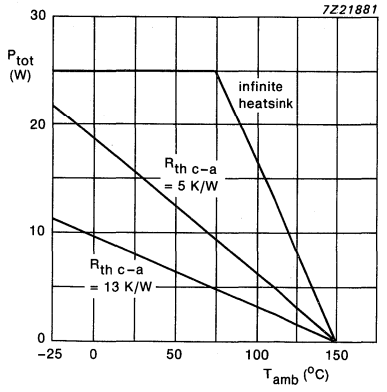


Fig.3 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage range	note 2	6.0	14.4	18	V
I_P	quiescent current		–	40	80	mA
V_O	DC output voltage	note 3	–	6.8	–	V
$\lvert\Delta V_{os}\rvert$	DC output offset voltage (pins 5 and 9)		–	–	100	mV
Mute/stand-by switch						
V_{sw}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	V_I = 1 V (max); f = 20 Hz to 10 kHz	–	–	2	mV
$\lvert\Delta V_{os}\rvert$	DC output offset voltage (pins 5 and 9)		–	–	100	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	DC standby current	$V_{11} \leq 0.5$ V	–	–	100	µA
		$0.5 < V_{11} \leq 2$ V	–	–	500	µA
I_{sw}	switch-on current	$V_{11} \leq V_{10}$; note 4	–	25	60	µA
I_P	supply current	short-circuit to GND; note 5	–	5.5	–	mA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified. See note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
		THD = 10%; note 6	21	24	–	W
		V_P = 13.2 V; THD = 0.5%	–	13.5	–	W
		V_P = 13.2 V; THD = 10%	–	17	–	W
		V_P = 13.2 V; THD = 10%; note 6	–	19	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.05	–	%
B	power bandwidth	THD = 0.5%; P_O = −1 dB with respect to 15 W	–	20 to 15 000	–	Hz
f_{low}	low frequency roll-off	−3 dB; note 7	–	25	–	Hz
f_{high}	high frequency roll-off	−1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection					
		ON; notes 8 and 9	45	–	–	dB
		ON; notes 8 and 10	48	–	–	dB
		MUTE; notes 8 to 10	48	–	–	dB
		stand-by; notes 8 to 10	80	–	–	dB
$\|Z_I\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
		ON; R_S = 0; note 11	–	70	–	μV
		R_S = 10 kΩ; note 12	–	100	200	μV
		MUTE; note 12	–	60	–	μV

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig.4
2. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V
3. At 18 V < V_P < 30 V, the DC output voltage ≤ V_P/2
4. If $V_{11} > V_{10}$, then I_{11} must be ≤ 10 mA
5. Conditions: V_{11} = 0; short-circuit output to GND; switch V_{11} to mute or on condition (rise time V_{11} > 10 μs)
6. With bootstrap and a resistor of 100 kΩ from V_P/2 to the positive supply voltage (V_P). (Bootstrap capacitor of 47 μF)
7. Frequency response externally fixed
8. Ripple rejection measured at the output with a source-impedance of 0 Ω (max. ripple amplitude of 2 V)
9. Frequency = 100 Hz
10. Frequency = 1 to 10 kHz
11. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz
12. Noise output voltage independent of R_S (V_{in} = 0)

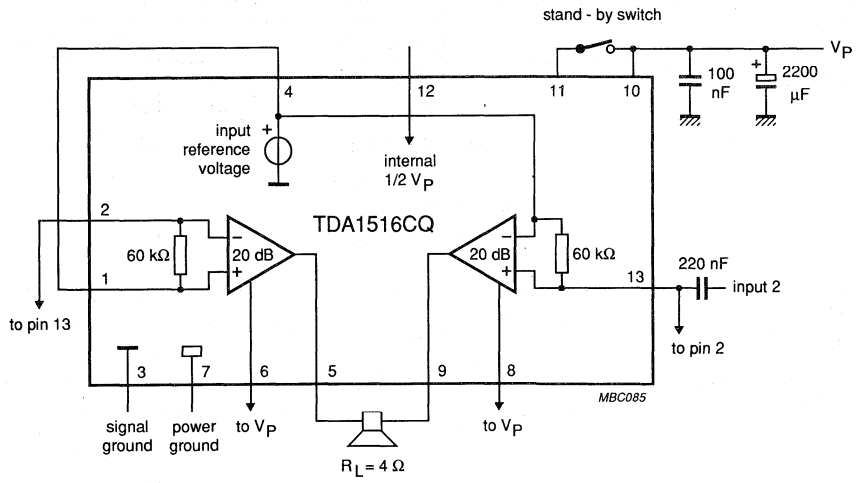


Fig.4 Application diagram.

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a 9-lead single-in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1519 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump protected		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	50	–	μV
Supply voltage ripple rejection	f = 100 Hz to 100 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

PINNING

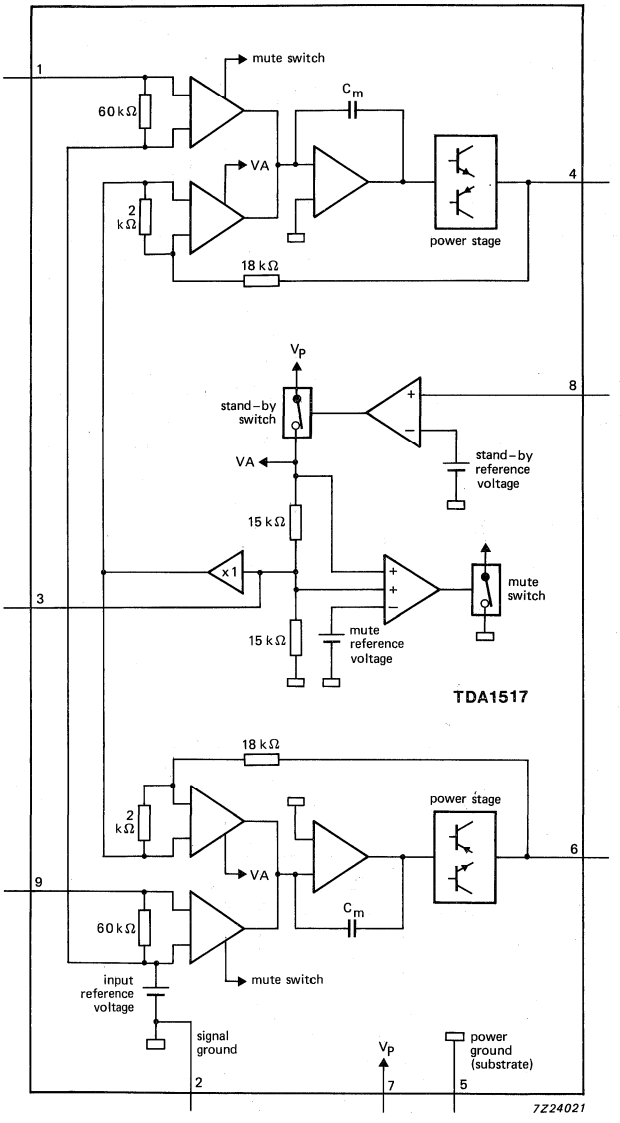


Fig. 1 Block diagram.

1	−INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-interting input 2

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+150	°C

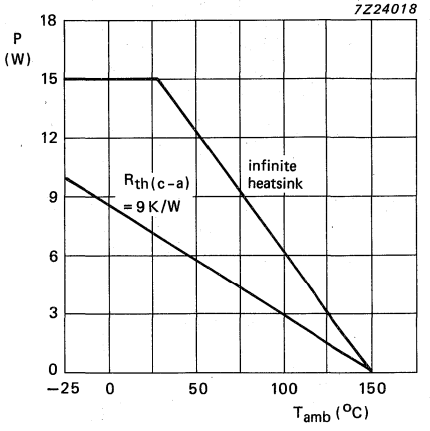


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch	see Fig. 3					
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max); f = 20 Hz to 15 kHz	V_O	–	–	2	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection:	note 6					
ON		SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage:	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	70	100	μV
mute	note 8	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V $<$ V_P $<$ 30 V the DC output voltage $\leqslant$ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

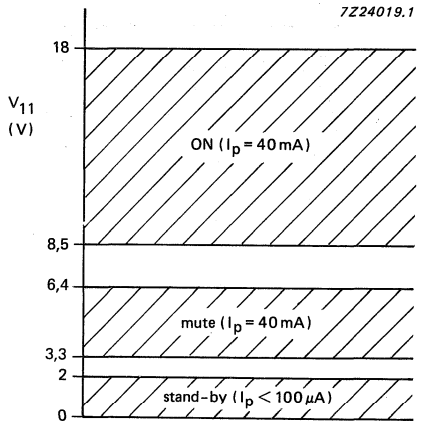


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

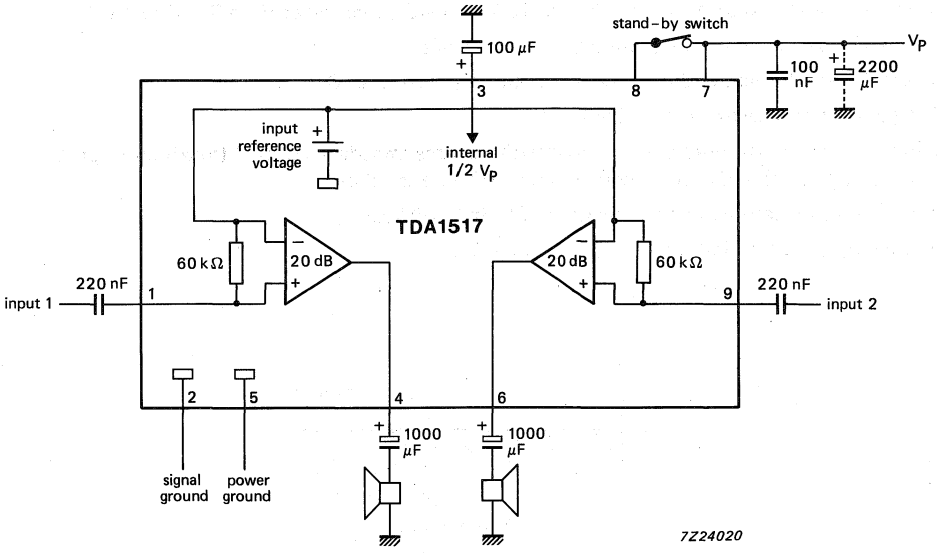


Fig. 4 Application circuit diagram.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1518BQ is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

FEATURES

- Requires very few external components
- Flexibility in use — stereo as well as mono BTL
- High output power (without bootstrap)
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- A.C. and d.c. short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1516BQ (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30,0	V
load dump		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	30	–	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
D.C. output offset voltage		$\|\Delta V_O\|$	–	–	250	mV

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141C).

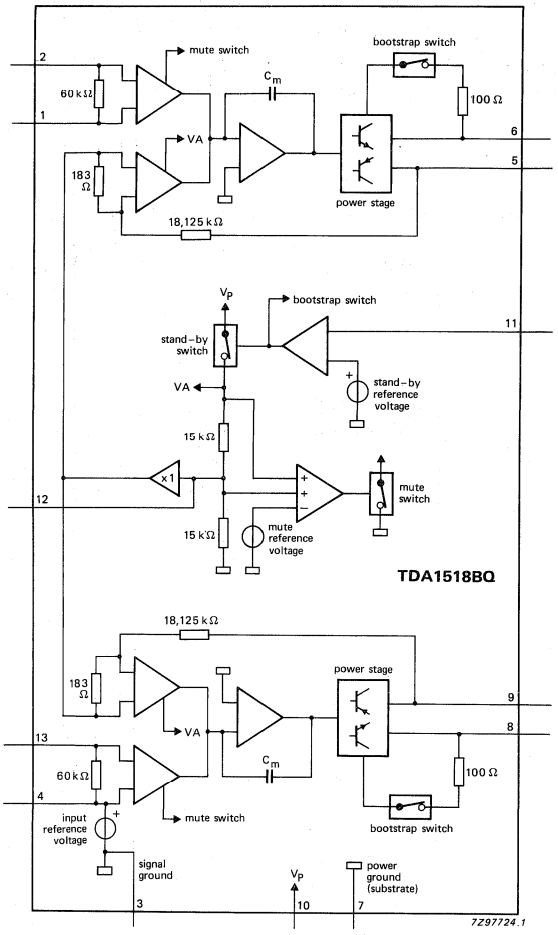


Fig. 1 Block diagram.

PINNING

1	−INV1	non-inverting input 1
2	INV	inverting input
3	GND1	ground (signal)
4	V_{ref}	reference voltage
5	OUT1	output 1
6	BS1	bootstrap 1
7	GND2	ground (substrate)
8	BS2	bootstrap 2
9	OUT2	output 2
10	V_P	supply voltage
11	M/SS	mute/stand-by switch
12	RR	supply voltage ripple rejection
13	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1518BQ contains two identical amplifiers with differential input stages. This device can be used for stereo or bridge applications. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
A.C. and d.c. short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	−55	+150	°C

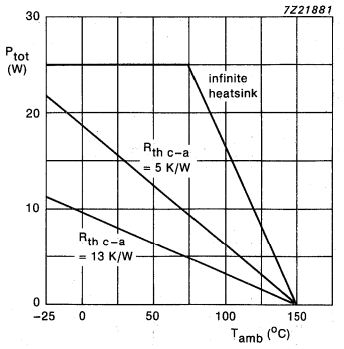


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS (note 1)

V_P = 14.4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	30	*	mA
D.C. output voltage at approximately $V_P/2$	note 3	V_O	–	6,8	–	V
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	200	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,0	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	*	20	mV
D.C. output offset voltage		$\lvert\Delta V_{5\text{-}9}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
D.C. current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

* Value to be fixed.

A.C. CHARACTERISTICS

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application	note 1					
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
	notes 4 and 5;					
	THD = 10%	P_o	6	7	–	W
Output power at	note 4;					
R_L = 2 Ω	THD = 0,5%	P_o	7,75	8,5	–	W
	THD = 10%	P_o	10	11	–	W
	notes 4 and 5;					
	THD = 10%	P_o	10,5	12,0	–	W
Low frequency roll-off	note 6;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		G_v	–	0.1	1	dB

A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application	note 10					
Output power	THD = 0,5%	P_o	15,5	17,0	–	W
	THD = 10%	P_o	20	22	–	W
	note 5; THD = 10%	P_o	21	24	–	W
Output power at V_P = 13,2 V	THD = 0,5%	P_o	–	13.5	–	W
	THD = 10%	P_o	–	17	–	W
	note 5; THD = 10%	P_o	–	19	–	W
Power bandwidth	THD = 0,5%; P_o = 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 6; –3 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection:	note 7					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_I\|$	25	30	38	kΩ
Noise output voltage:	note 8;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Switch-on/switch-off behaviour		dV/dt	–	–	*	V/ms

Notes to the characteristics

1. All characteristics, for stereo application are measured using the circuit shown in Fig. 3.
2. The circuit is d.c. adjusted at V_P = 6 V to 18 V and a.c. operating at V_P = 8,1 V to 18 V.
3. At 18 V $< V_P <$ 30 V the d.c. output voltage $\leqslant V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. With bootstrap and a 100 kΩ resistor from pin 12 to the positive supply voltage (V_P), value of bootstrap capacitor is 47 μF.
6. Frequency response externally fixed.
7. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).
10. All characteristics, for BTL application are measured using the circuit shown in Fig. 4.

* Value to be fixed.

APPLICATION INFORMATION

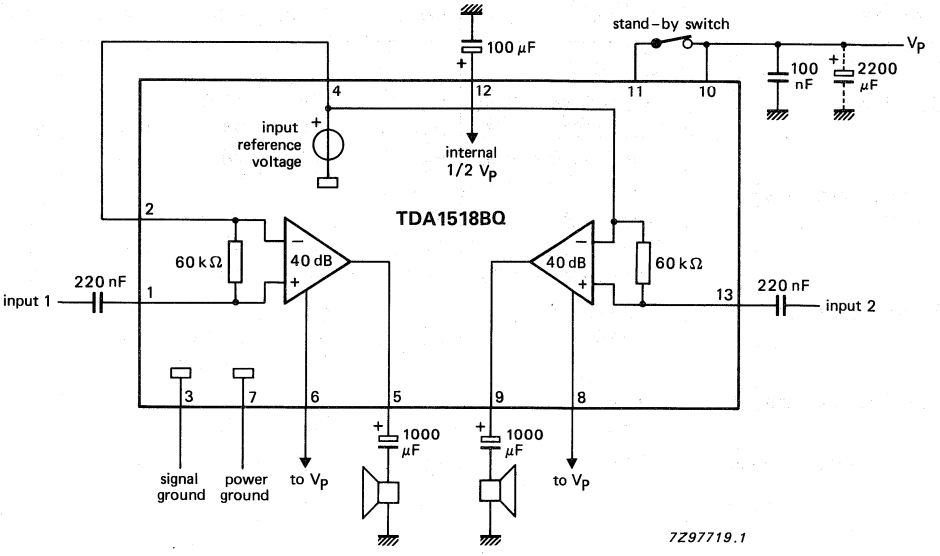


Fig. 3 Stereo application circuit diagram.

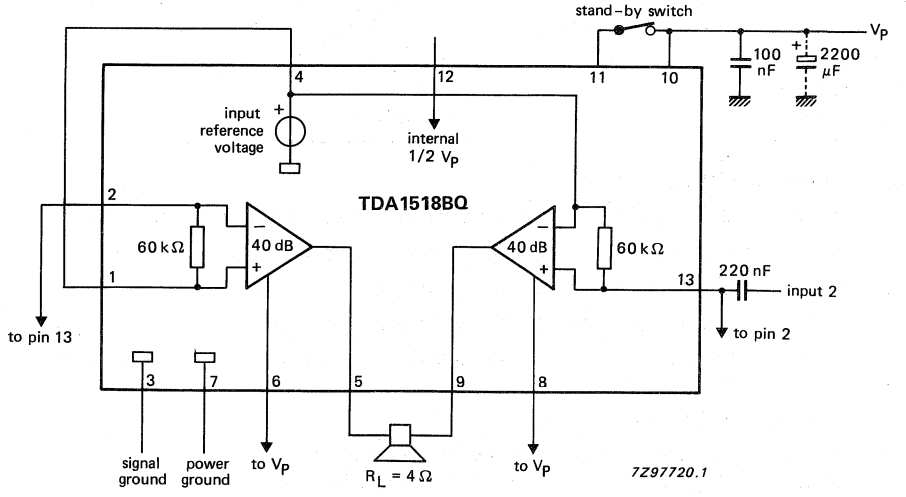


Fig. 4 BTL application circuit diagram (without bootstrapping).

2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519 is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Compatible with TDA1517 (except gain)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2,5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0,1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance		$\|Z_I\|$	50	–	–	kΩ
Output power	THD = 0,5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
Supply voltage ripple rejection	f = 100 Hz	SVRR	40	–	–	dB
	f = 1 kHz to 10 kHz	SVRR	48	–	–	dB
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL-bent-to-DIL; plastic (SOT110B).

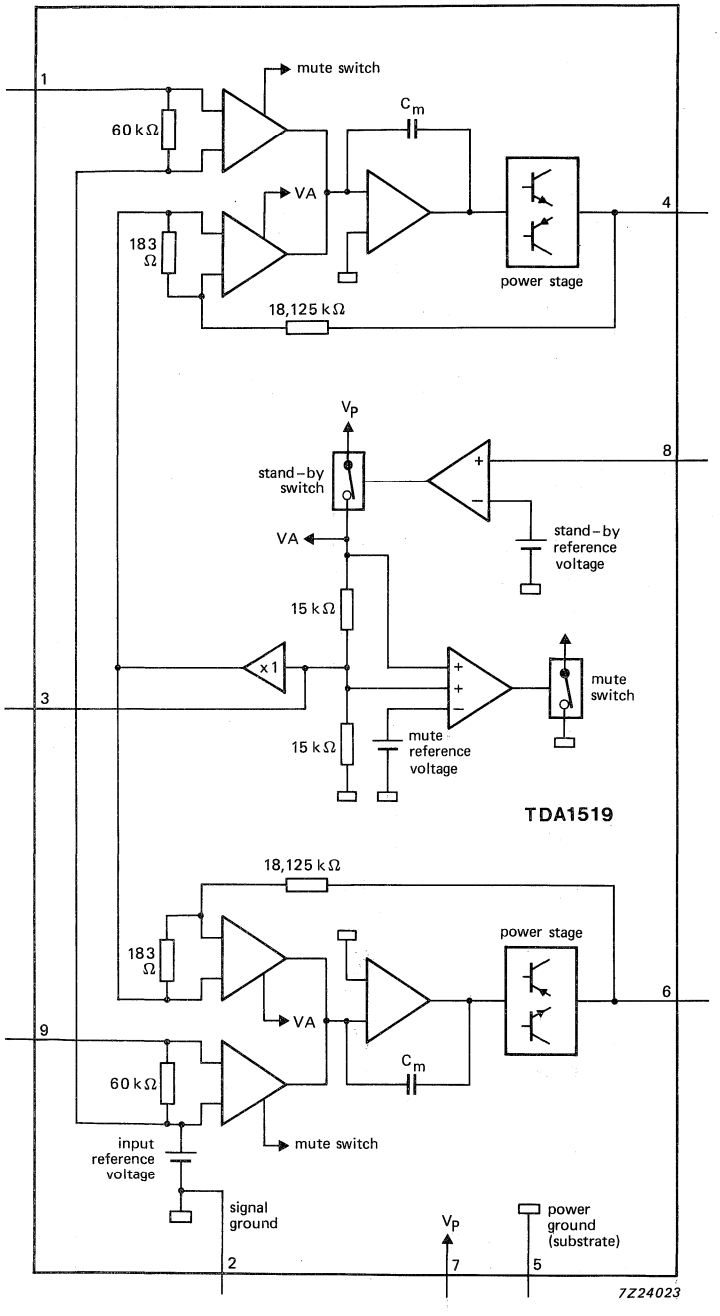


Fig. 1 Block diagram.

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	supply voltage
8	M/SS	mute/stand-by switch
9	−INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

The TDA1519 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2{,}5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2,5	A
Total power dissipation	see Fig. 2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+ 150	°C

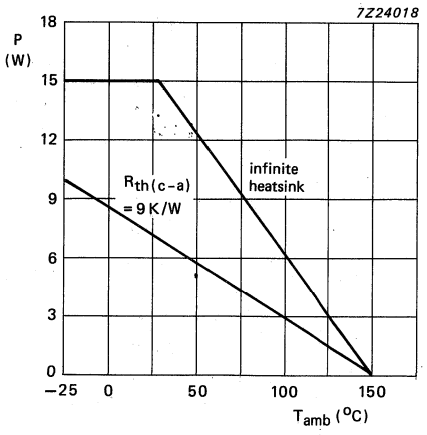


Fig. 2 Power derating curve.

DC CHARACTERISTICS (note 1)

V_P = 14,4 V; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 2	V_P	6,0	14,4	18,0	V
Quiescent current		I_P	–	40	80	mA
DC output voltage	note 3	V_O	–	6,95	–	V
Mute/stand-by switch						
Switch-on voltage level	see Fig. 3	V_{ON}	8,5	–	–	V
Mute condition		V_{mute}	3,3	–	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS (note 1)

V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_o	4	5	–	W
	THD = 10%	P_o	5,5	6,0	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0,1	–	%
Low frequency roll-off	note 5;					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection	note 6					
ON	f = 100 Hz	SVRR	40	–	–	dB
ON	f = 10 Hz to 10 kHz	SVRR	48	–	–	dB
mute		SVRR	48	–	–	dB
stand-by		SVRR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 8	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel balance		$\|\Delta G_v\|$	–	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8,5 V to 18 V.
3. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R_S (V_I = 0 V).

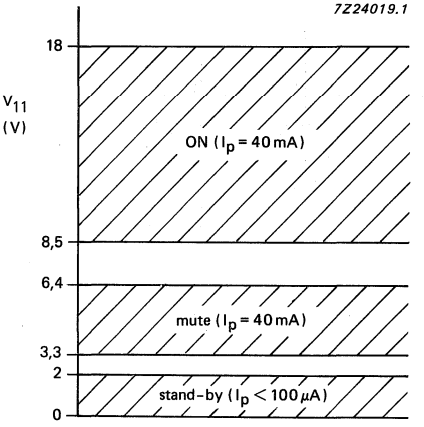


Fig. 3 Stand-by, mute and ON conditions.

APPLICATION INFORMATION

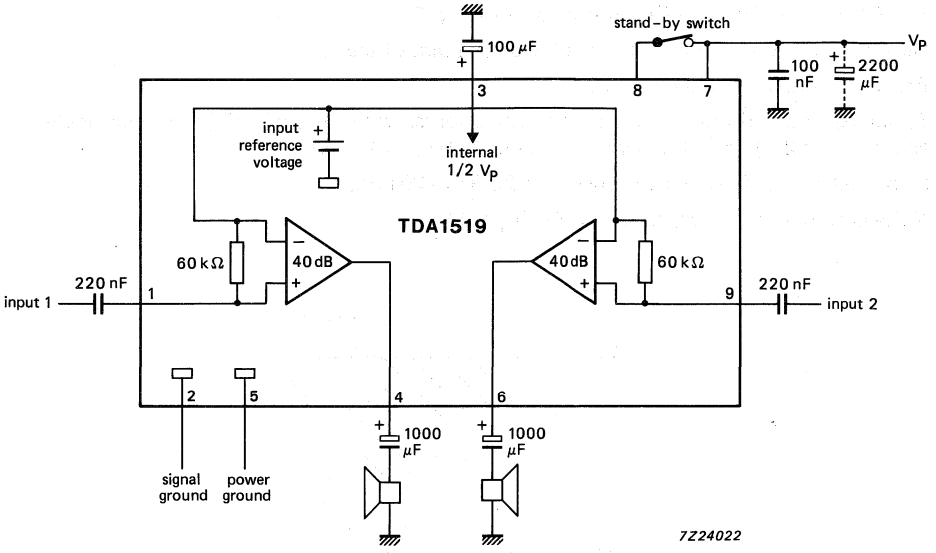


Fig. 4 Application circuit diagram.

22 W BTL OR 2 × 11 WATT STEREO CAR RADIO POWER AMLIFIER

GENERAL DESCRIPTION

The TDA1519A is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications.

Features

- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519B (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	17.5	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 10%; 4 Ω	P_o	–	6	–	W
	THD = 10%; 2 Ω	P_o	–	11	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 4 Ω	P_o	–	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

9-lead SIL; plastic power (SOT131).
9-lead SIL-bent-to-DIL; plastic power (SOT157).

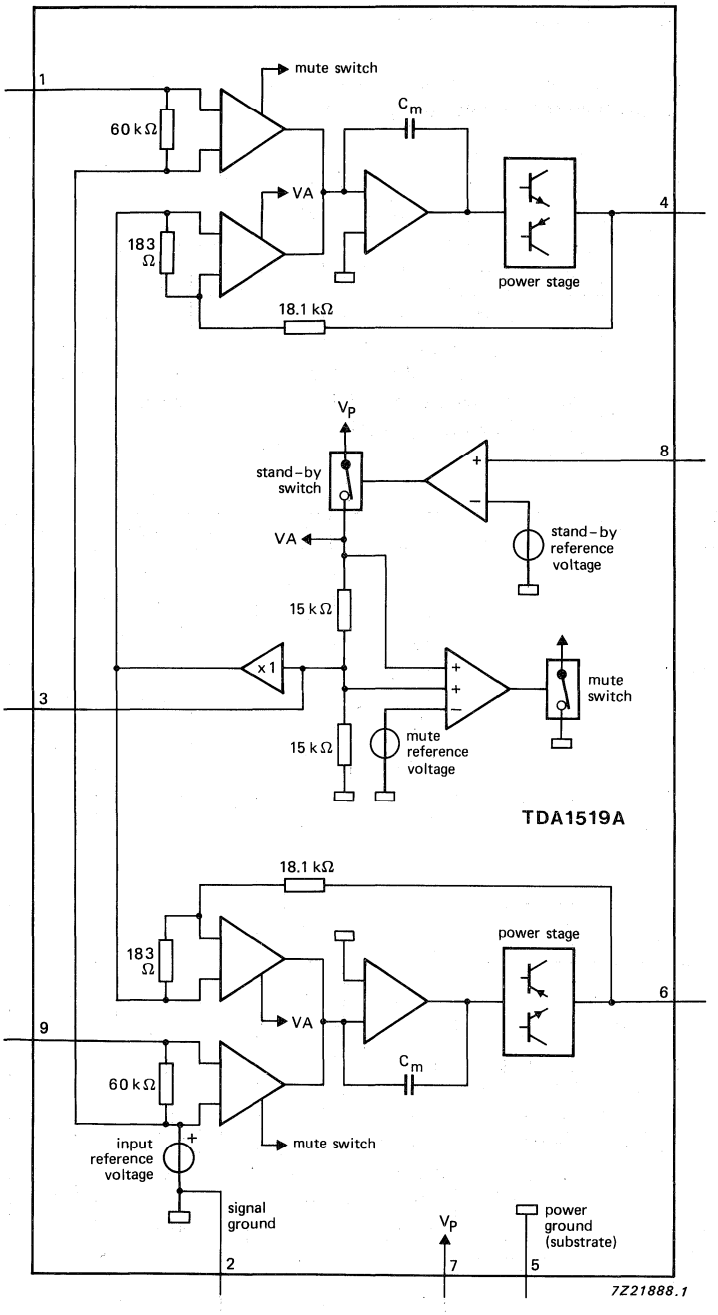


Fig.1 Block diagram.

PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

FUNCTIONAL DESCRIPTION

The TDA1519A contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	17.5	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Total power dissipation	see Fig.2	P_{tot}	–	25	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+150	°C

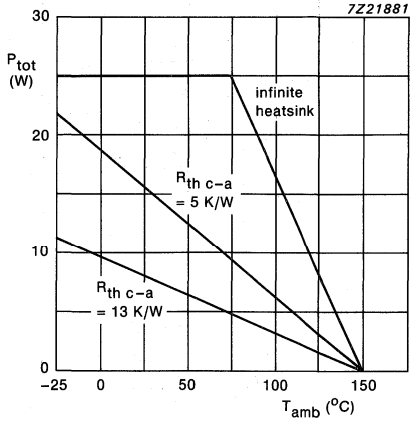


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	17.5	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6.0	–	W
Output power at R_L = 2 Ω	note 3					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5 and 8	RR	45	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 10	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	13	–	W
	THD = 10%	P_o	–	17.5	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = –1 dB; w.r.t. 15 W	B_w	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	–1 dB	f_L	–	45	–	Hz
High frequency roll-off	–1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5 and 8	RR	48	–	–	dB
stand-by	notes 5 and 8	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 9					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 10	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 17.5 V and AC operating at V_P = 8.5 V to 17.5 V.
2. At 17.5 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Frequency between 100 Hz and 10 kHz.
9. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
10. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

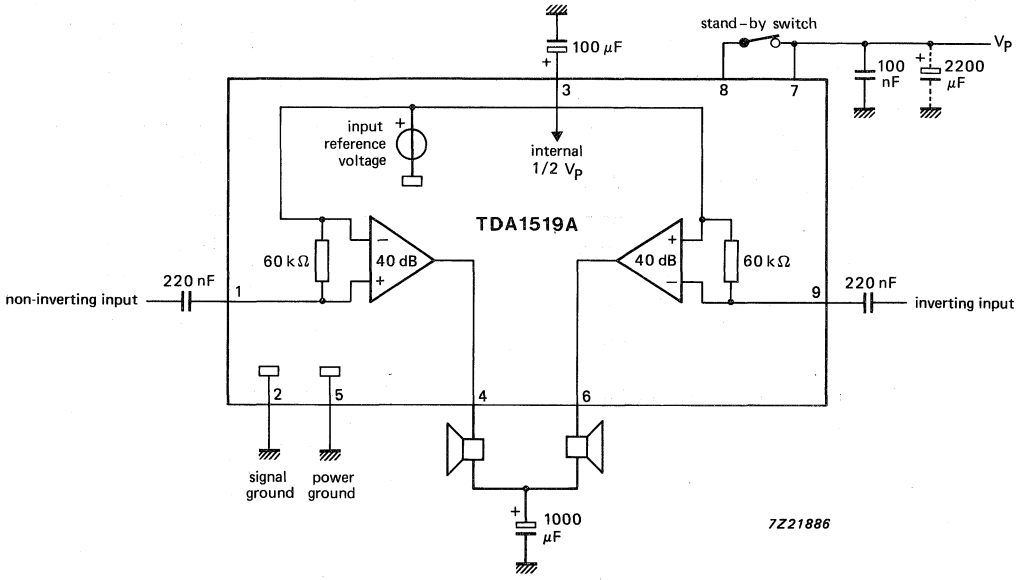


Fig.3 Stereo application circuit diagram.

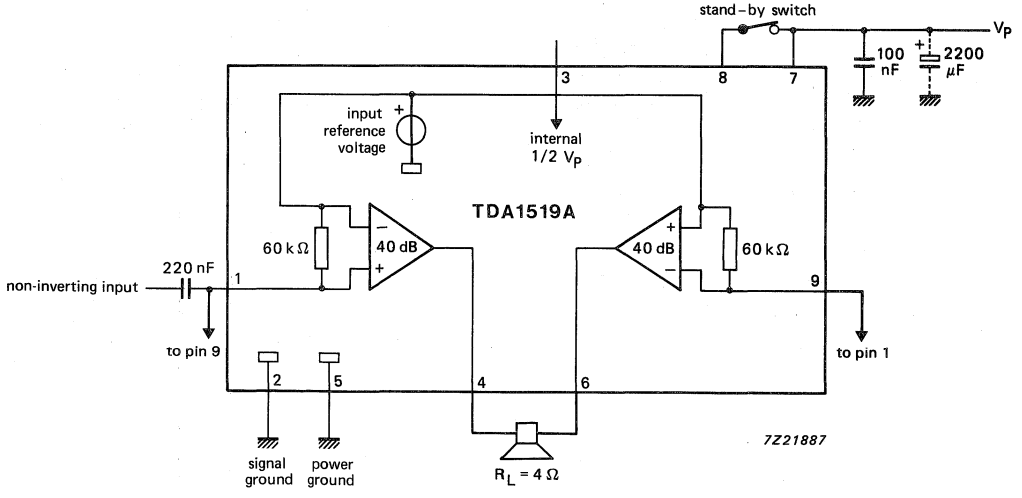


Fig.4 BTL application circuit diagram.

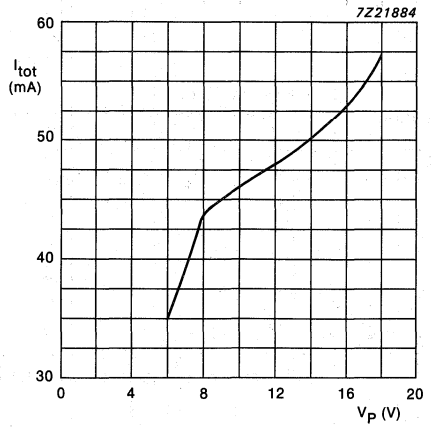


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

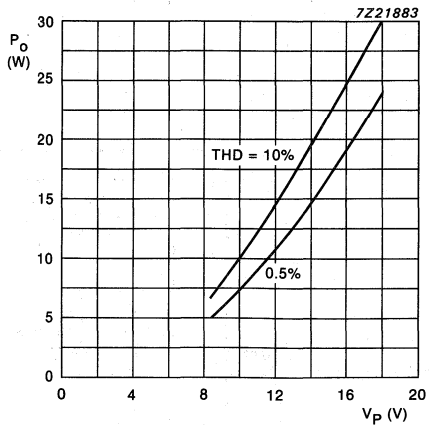


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

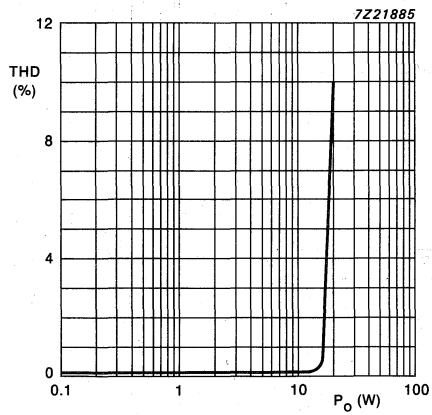


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for BTL application at $R_L = 4\ \Omega$; f = 1 kHz.

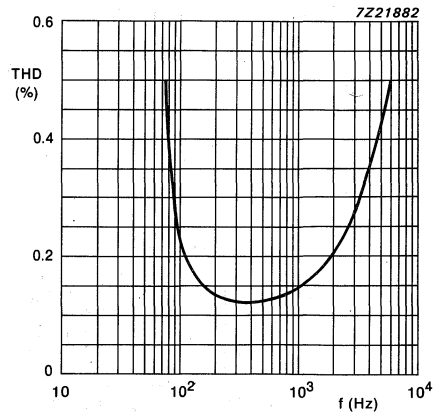


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for BTL application at $R_L = 4\ \Omega$; $P_o = 1$ W.

12 W BTL OR 2 × 6 WATT STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1519B is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

Features

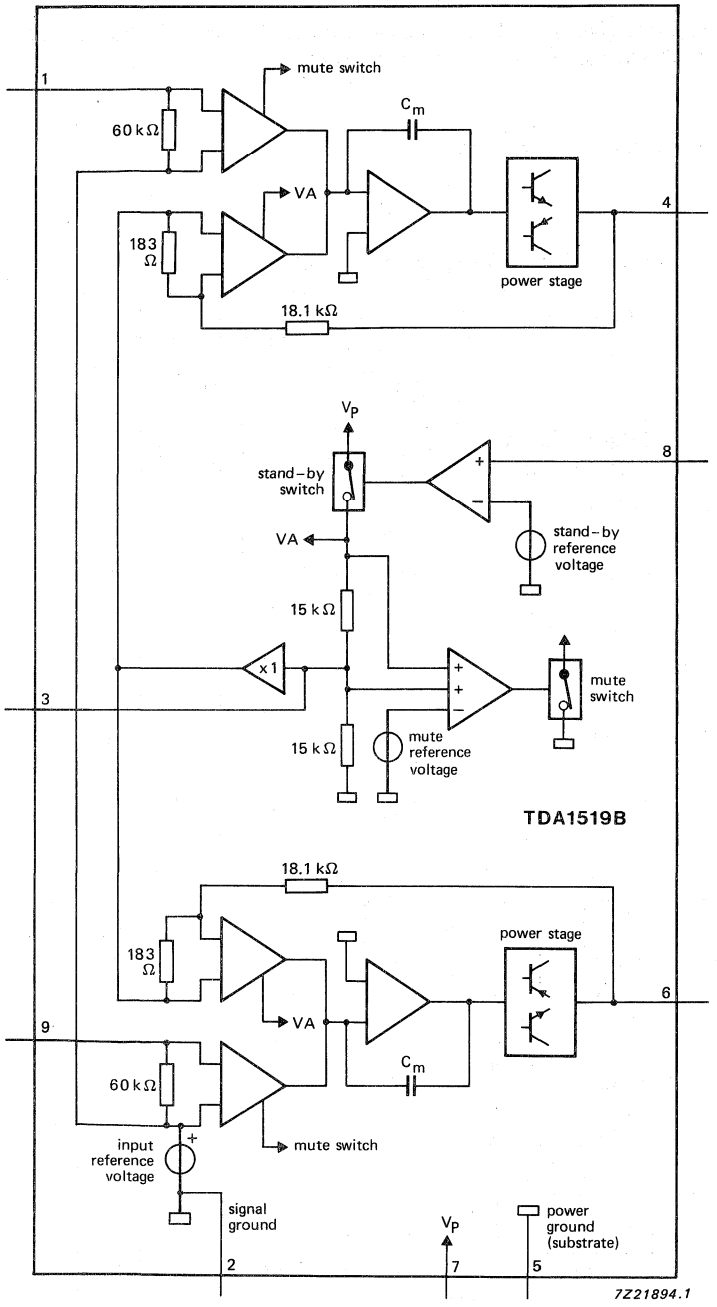
- Requires very few external components for Bridge Tied Load (BTL)
- Stereo or BTL application
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Protected against electrostatic discharge
- Identical inputs (inverting and non-inverting)
- Compatible with TDA1519A (except output power)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	2.5	A
Total quiescent current		I_{tot}	–	40	80	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	40	μA
Input impedance						
BTL		$\|Z_I\|$	25	–	–	kΩ
stereo		$\|Z_I\|$	50	–	–	kΩ
Stereo application						
Output power	THD = 5%; 4 Ω	P_o	–	5	–	W
	THD = 10%; 4 Ω	P_o	–	6	–	W
Channel separation		α	40	–	–	dB
Noise output voltage		$V_{no(rms)}$	–	150	–	μV
BTL application						
Output power	THD = 10%; 8 Ω	P_o	–	12	–	W
Supply voltage ripple rejection	R_S = 0 Ω					
	f = 100 Hz	RR	34	–	–	dB
	f = 1 kHz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	250	mV
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT110B).



PINNING

1	NINV	non-inverting input
2	GND1	ground (signal)
3	RR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	V_P	positive supply voltage
8	M/SS	mute/stand-by switch
9	INV	inverting input

Fig.1 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA1519B contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 40 dB. A special feature of this device is the mute/stand-by switch which has the following features:

- Low stand-by current ($< 100\ \mu A$)
- Low mute/stand-by switching current (low cost supply switch)
- Mute condition

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Reverse polarity		V_{PR}	–	6	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Non-repetitive peak output current		I_{OSM}	–	4	A
Repetitive peak output current		I_{ORM}	–	2.5	A
Total power dissipation	see Fig.2	P_{tot}	–	15	W
Crystal temperature		T_c	–	150	°C
Storage temperature range		T_{stg}	–55	+150	°C

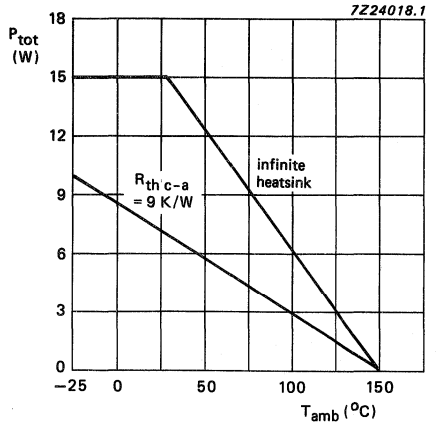


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	40	80	mA
DC output voltage	note 2	V_O	–	6.95	–	V
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	–	–	20	mV
DC output offset voltage		$\lvert\Delta V_{4\text{-}6}\rvert$	–	–	250	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power	note 3					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10!	P_o	5.5	6.0	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	3.5	–	W
	THD = 10%	P_o	–	4.8	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 4					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	39	40	41	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	40	–	–	dB
ON	notes 5 and 7	RR	45	–	–	dB
mute	notes 5, 6 and 7	RR	45	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	150	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	250	500	μV
mute	note 9	$V_{no(rms)}$	–	120	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	0.1	1	dB

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
BTL application						
Output power	note 3					
	THD = 0.5%	P_o	8	10	–	W
	THD = 10%	P_o	11	12	–	W
Output power at V_P = 13.2 V	note 3					
	THD = 0.5%	P_o	–	7.5	–	W
	THD = 10%	P_o	–	10	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB; w.r.t. 15 W	B_w	–	35 to 15 000	–	Hz
Low frequency roll-off	note 4					
	−1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	45	46	47	dB
Supply voltage ripple rejection						
ON	notes 5 and 6	RR	34	–	–	dB
ON	notes 5 and 7	RR	48	–	–	dB
mute	notes 5, 6 and 7	RR	48	–	–	dB
stand-by	notes 5, 6 and 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)	note 8					
ON	R_S = 0 Ω	$V_{no(rms)}$	–	200	–	μV
ON	R_S = 10 kΩ	$V_{no(rms)}$	–	350	700	μV
mute	note 9	$V_{no(rms)}$	–	180	–	μV

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V $< V_P <$ 30 V the DC output voltage $\leqslant V_P/2$.
3. Output power is measured directly at the output pins of the IC.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

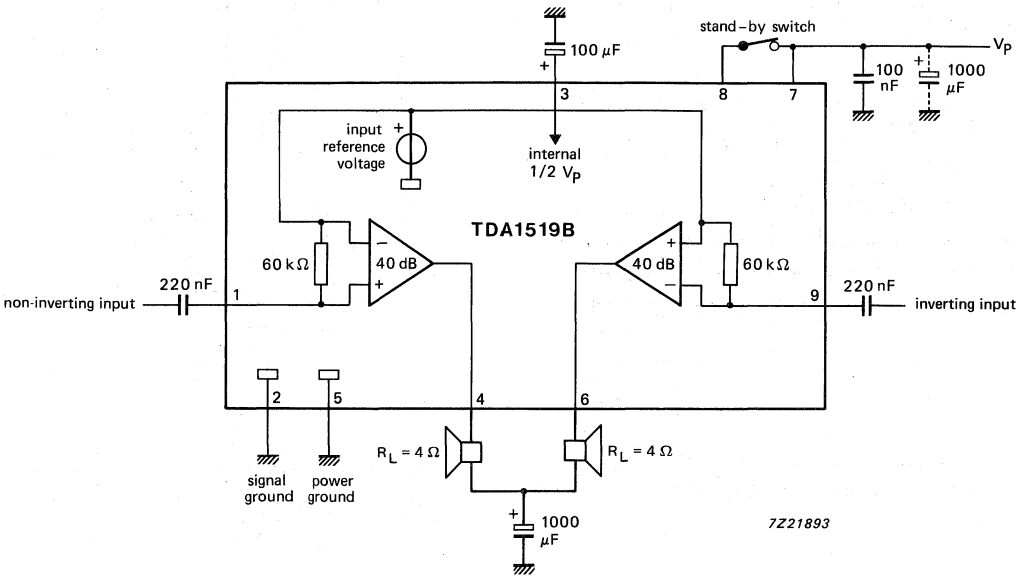


Fig.3 Stereo application circuit diagram.

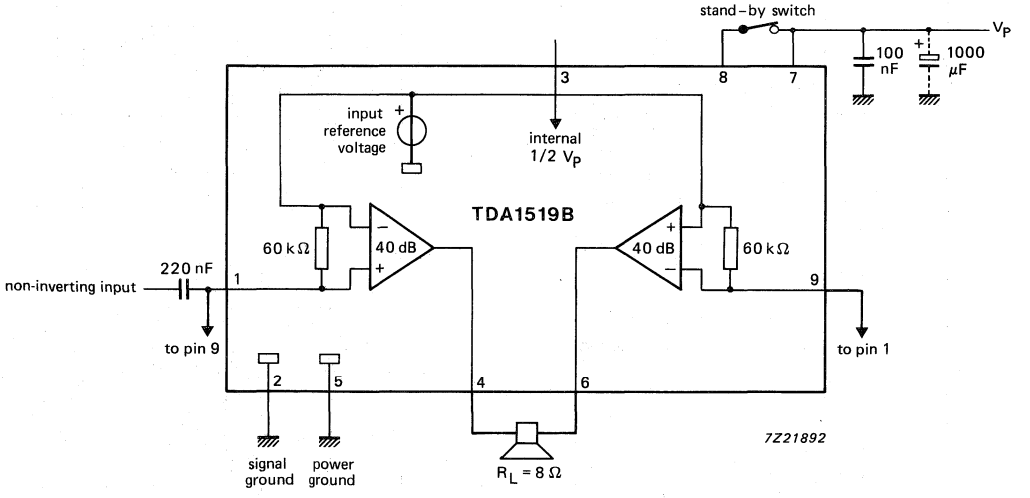


Fig.4 BTL application circuit diagram.

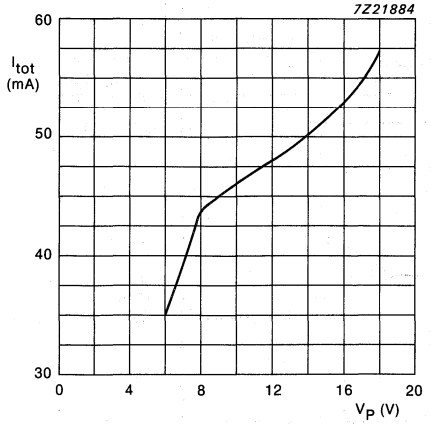


Fig.5 Total quiescent current (I_{tot}) as a function of supply voltage (V_P).

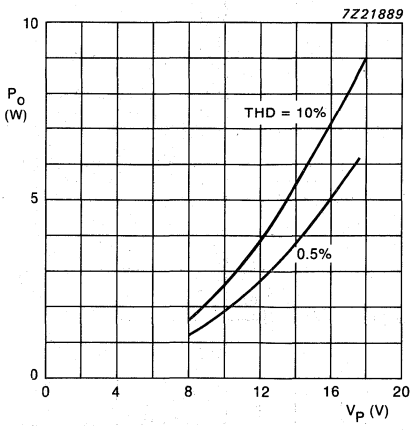


Fig.6 Output power (P_o) as a function of supply voltage (V_P) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

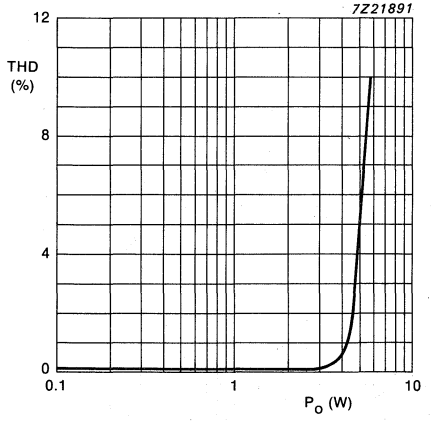


Fig.7 Total harmonic distortion (THD) as a function of output power (P_o) for stereo application at $R_L = 4\ \Omega$, f = 1 kHz.

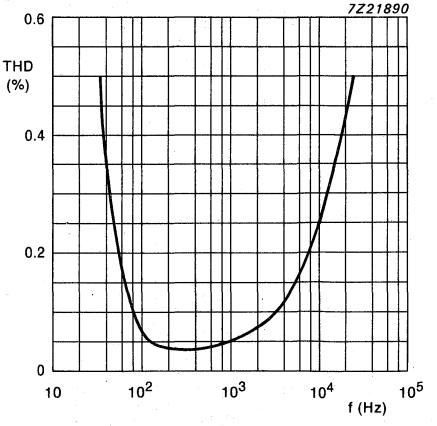


Fig.8 Total harmonic distortion (THD) as a function of operating frequency (f) for stereo application at $R_L = 4\ \Omega$, $P_o = 1$ W.

2 x 12 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521/TDA1521Q is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 16 V	P_o	typ. 12	W
Voltage gain	G_v	typ. 30	dB
Gain balance between channels	ΔG_v	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINES

TDA1521: 9-lead single in-line; plastic power (SOT131).
TDA1521Q: 9-lead SIL-bent-to-DIL; plastic power (SOT157).

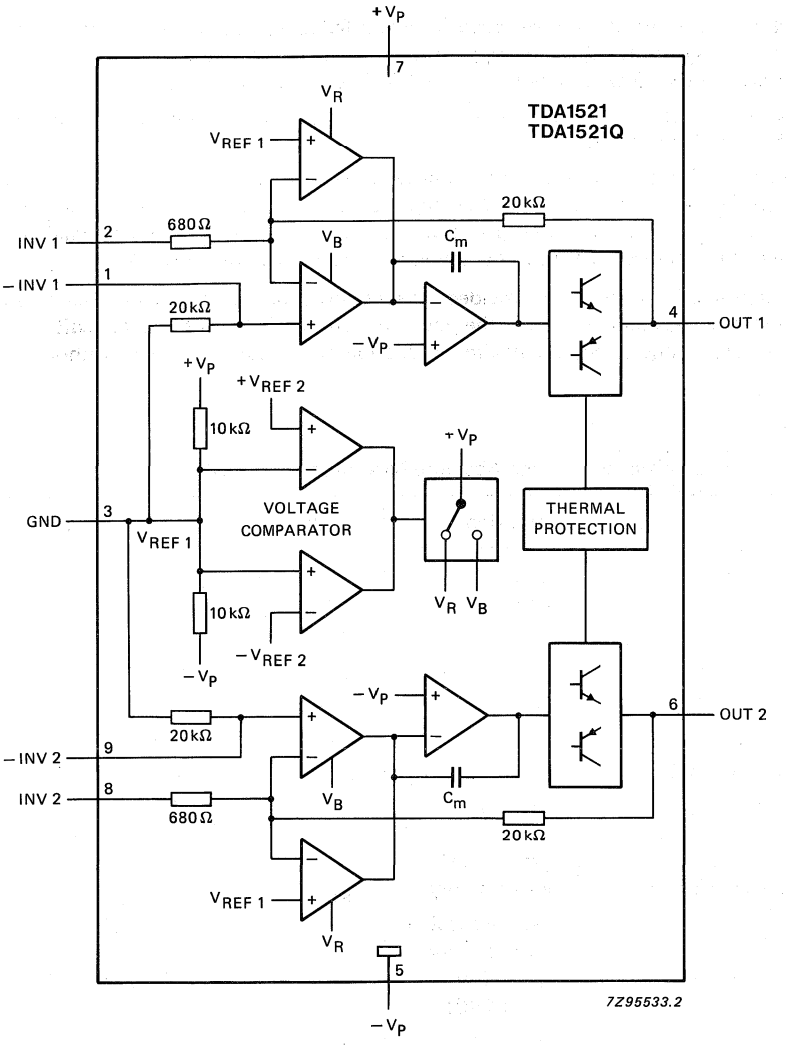


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) / ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) / ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 12 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 16 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 13, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply; $V_P < 32$ V (unloaded); $R_i \geqslant 4\ \Omega$	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V. If the total internal resistance of the supply (R_i) > 4 Ω, the maximum unloaded supply voltage is increased to 32 V.

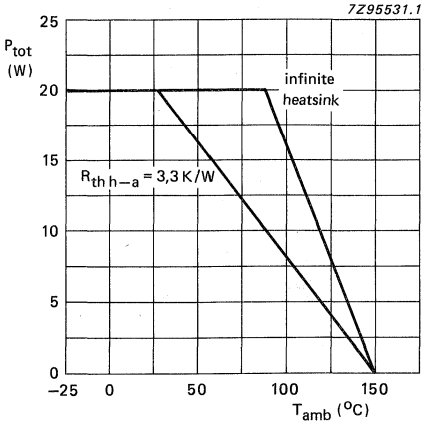


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j\text{-}c}$ = 2,5 K/W

HEATSINK DESIGN EXAMPLE

With derating of 2,5 K/W, the value of heatsink thermal resistance is calculated as follows:

given R_L = 8 Ω and V_P = ±16 V, the measured maximum dissipation is 14,6 W; then, for a maximum ambient temperature of 65 °C, the required thermal resistance of the heatsink is

$$R_{th\ h\text{-}a} = \frac{150 - 65}{14{,}6} - 2{,}5 = 3{,}3\ \text{K/W}$$

Note: The internal metal block (heatsink) has the same potential as pin 5 ($-V_P$)

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 16,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,8	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 16 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	10	12	–	W
	THD = 10%	P_o	12	15	–	W
Total harmonic distortion	P_o = 6 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 12; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 13; V_S = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 20k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	35	44	–	dB
Channel separation	R_S = 0 Ω	α	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

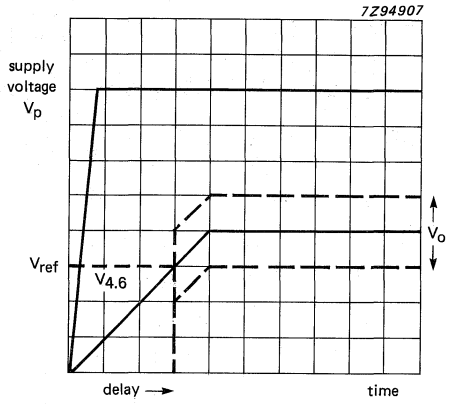


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

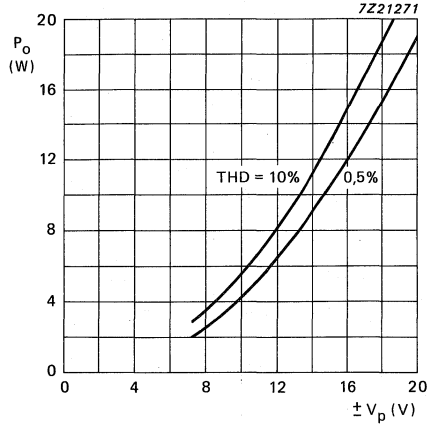


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

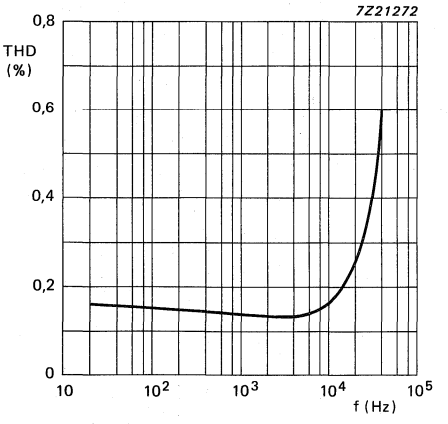


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; $P_O = 6$ W.

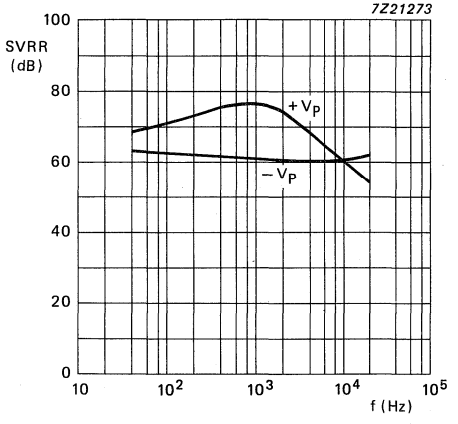


Fig. 6 Supply voltage ripple rejection; symmetrical supply; $V_P = \pm 16$ V; $V_{RR} = 200$ mV.

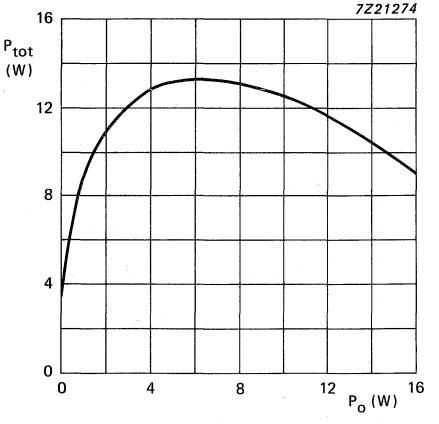


Fig. 7 Power dissipation as a function of output power; symmetrical supply; $V_P = \pm 16$ V; $R_L = 8\ \Omega$; f = 1 kHz.

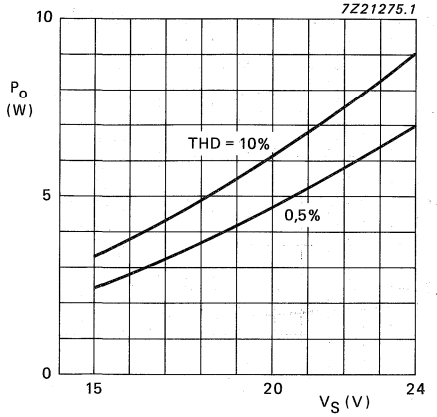


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

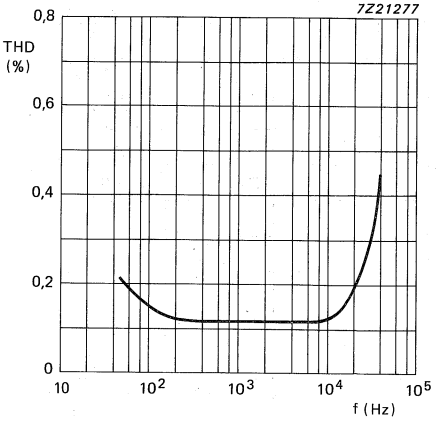


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 4$ W.

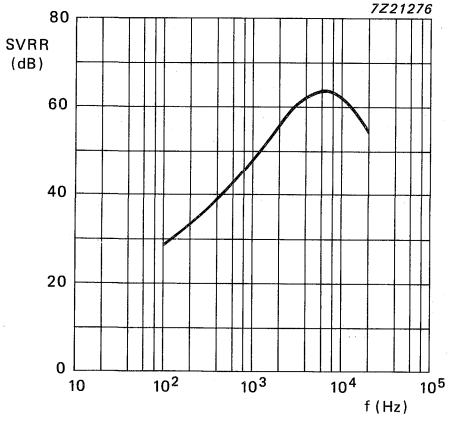


Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mV.

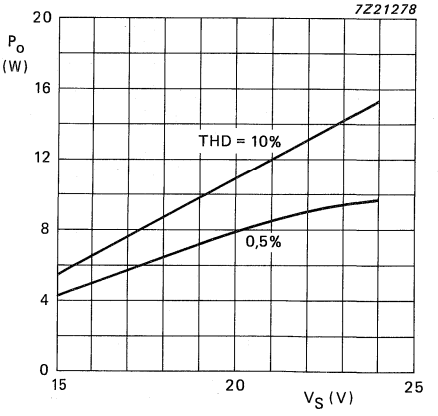
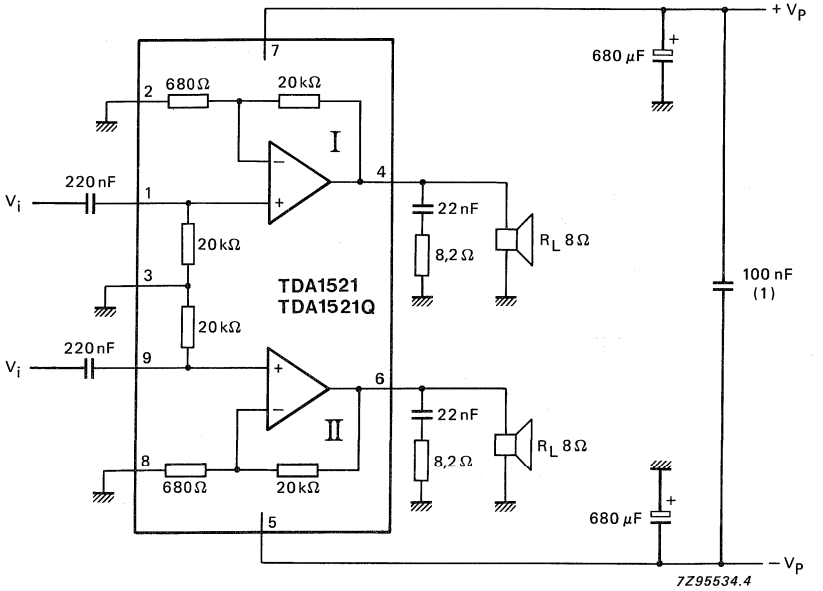
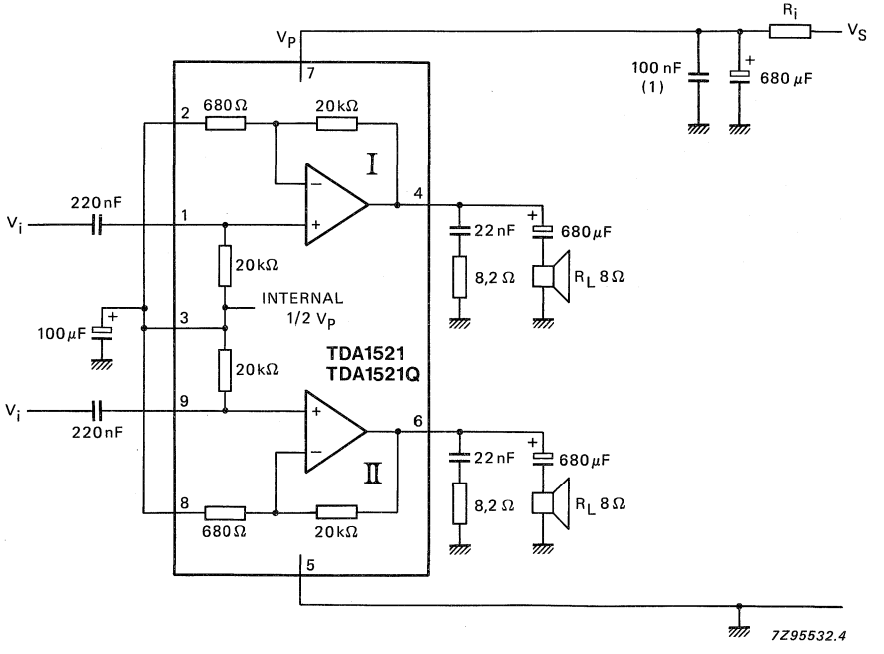


Fig. 11 Output power as a function of supply voltage; asymmetrical supply; $R_L = 4\ \Omega$; f = 1 kHz.



1 To be connected as close as possible to the IC

Fig. 12 Test and application circuit; symmetrical power supply.



1 To be connected as close as possible to the IC

Fig. 13 Test and application circuit; asymmetrical power supply.

2 x 6 W HI-FI AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1521A is a dual hi-fi audio power amplifier encapsulated in a 9-lead plastic power package. The device is especially designed for mains fed applications (e.g. stereo tv sound and stereo radio).

Features

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Excellent gain balance between channels
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected

QUICK REFERENCE DATA

Stereo applications			
Supply voltage range	V_P	± 7,5 to ± 20,0	V
Output power at THD = 0,5%, V_P = ± 12 V	P_O	typ. 6	W
Voltage gain	G_V	typ. 30	dB
Gain balance between channels	ΔG_V	typ. 0,2	dB
Ripple rejection	SVRR	typ. 60	dB
Channel separation	α	typ. 70	dB
Noise output voltage	$V_{no(rms)}$	typ. 70	μV

PACKAGE OUTLINE

TDA1521A: 9-lead single in-line; plastic power (SOT 110B).

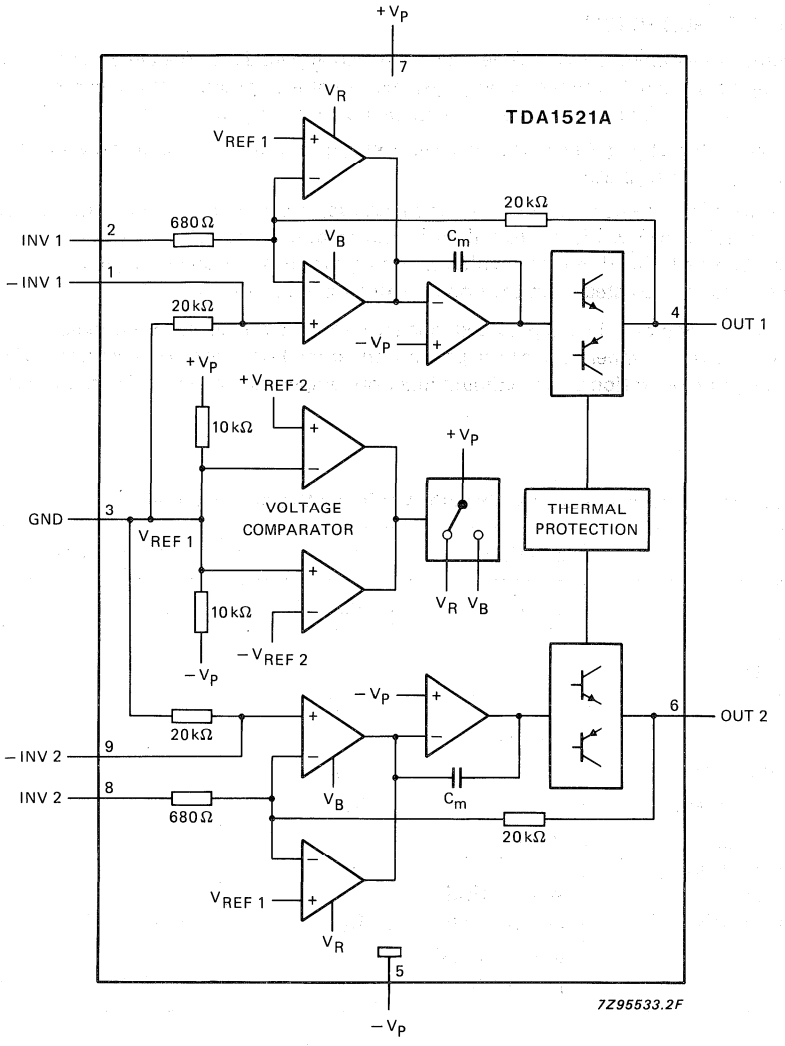


Fig. 1 Block diagram.

PINNING

1	–INV1	non-inverting input 1
2	INV1	inverting input 1
3	GND	ground (symmetrical) ½ VP (asymmetrical)
4	OUT1	output 1
5	–VP	negative supply (symmetrical) ground (asymmetrical)
6	OUT2	output 2
7	+ VP	positive supply
8	INV2	inverting input 2
9	–INV2	non-inverting input 2

FUNCTIONAL DESCRIPTION

This hi-fi stereo power amplifier is designed for mains fed applications. The circuit is designed for both symmetrical and asymmetrical power supply systems. An output power of 2 x 6 watts (THD = 0,5%) can be delivered into an 8 Ω load with a symmetrical power supply of ± 12 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread and very good balance between the amplifiers (0,2 dB).

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig. 12, the 100 μF capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifiers remain in their DC operating mode but are isolated from the non-inverting inputs on pins 1 and 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150 °C allowing safe operation to a maximum junction temperature of 150 °C without added distortion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	pin 7	$V_P = V_{7-3}$	–	+ 20	V
	pin 5	$-V_P = V_{5-3}$	–	−20	V
Non-repetitive peak output current	pins 4 and 6	I_{OSM}	–	4	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note				
	symmetrical power supply	t_{sc}	–	1	hour
	asymmetrical power supply	t_{sc}	–	1	hour

Note

For asymmetrical power supplies (at short circuiting of the load) the maximum supply voltage is limited to V_P = 28 V.

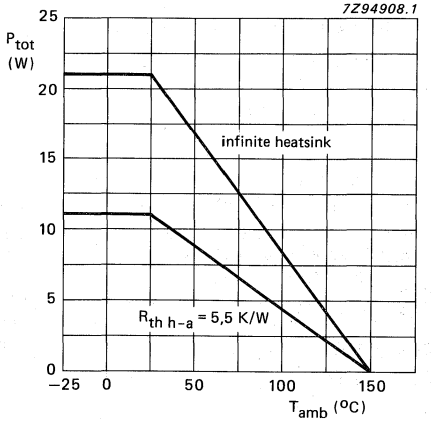


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to case $R_{th\ j-c} = 6$ K/W

HEATSINK DESIGN EXAMPLE

With derating of 6 K/W, the value of heatsink thermal resistance is calculated as follows:

given $R_L = 8\ \Omega$ and $V_P = \pm 12$ V, the measured maximum dissipation is 7,8 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is

$$R_{th\ h-a} = \frac{150 - 60}{7,8} - 6 = 5,5\ \text{K/W}$$

Note: The metal tab (heatsink) has the same potential as pin 5 ($-V_P$).

CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating mode		V_P	± 7,5	± 12,0	± 20,0	V
input mute mode		V_P	± 2,0	–	± 5,8	V
Repetitive peak output current		I_{ORM}	–	–	2,2	A
Operating mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 12 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8,0	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5% note 1	B		20 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection	note 2	SVRR	40	60	–	dB
Channel separation	R_S = 0 Ω	α	46	70	–	dB
Input bias current		I_{ib}	–	0,3	–	μA
DC output offset voltage	with respect to ground	V_{OFF}	–	30	200	mV
Input mute mode: symmetrical power supply; test circuit as per Fig. 11; V_P = ± 4 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current	without R_L	I_{tot}	9	30	40	mA
Output voltage	V_i = 600 mV	V_{out}	–	0,6	1,8	mV
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset voltage	with respect to ground	V_{OFF}	–	40	200	mV

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Operating mode: asymmetrical power supply; test circuit as per Fig. 12; V_P = 24 V; R_L = 8 Ω; T_{amb} = 25 °C; f = 1 kHz						
Total quiescent current		I_{tot}	18	40	70	mA
Output power	THD = 0,5%	P_o	5	6	–	W
	THD = 10%	P_o	6,5	8	–	W
Total harmonic distortion	P_o = 4 W	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5% note 1	B		40 to 16 k		Hz
Voltage gain		G_v	29	30	31	dB
Gain balance		ΔG_v	–	0,2	1,0	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)	R_S = 2 kΩ	$V_{no(rms)}$	–	70	140	μV
Input impedance		$\|Z_i\|$	14	20	26	kΩ
Ripple rejection		SVRR	35	44	–	dB
Channel separation	R_S = 0 Ω	∝	–	45	–	dB

Notes to the characteristics

1. Power bandwidth at $P_{o\ max}$ −3 dB.
2. Ripple rejection at R_S = 0 Ω, f = 100 Hz to 20 kHz; ripple voltage = 200 mV (r.m.s. value) applied to positive or negative supply rail.

APPLICATION INFORMATION

Input mute circuit

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the ½ supply voltage (at pin 3) with an internally fixed reference voltage (V_{ref}), derived directly from the supply voltage. When the voltage at pin 3 is lower than V_{ref} the non-inverting inputs (pins 1 and 9) are disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100 μF capacitor.
During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig. 3).

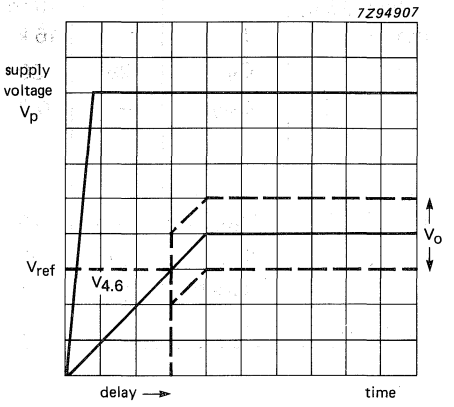


Fig. 3 Input mute circuit; time delay.

APPLICATION INFORMATION (continued)

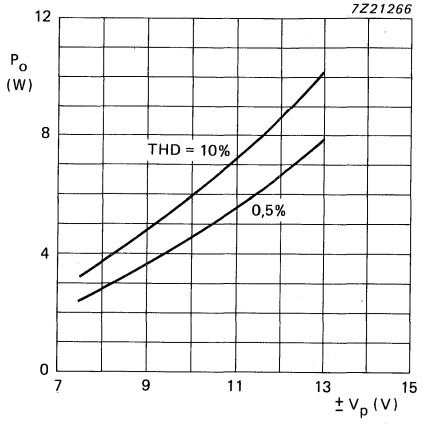


Fig. 4 Output power as a function of supply voltage; symmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

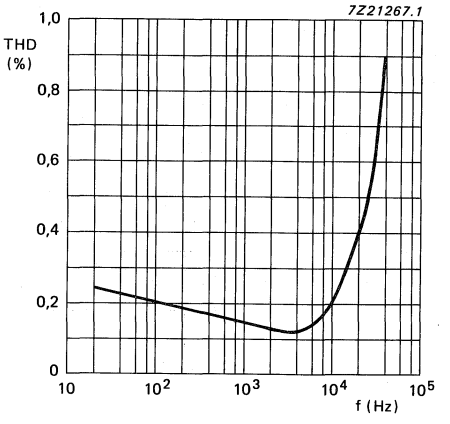


Fig. 5 Distortion as a function of frequency; symmetrical supply; $V_p = \pm 12$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

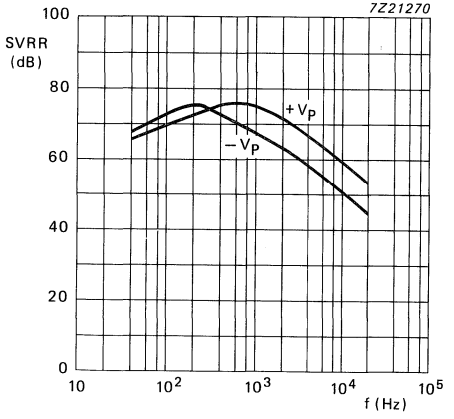


Fig. 6 Supply voltage ripple rejection; symmetrical supply, $V_P = \pm 12$ V; $V_{RR} = 200$ mV.

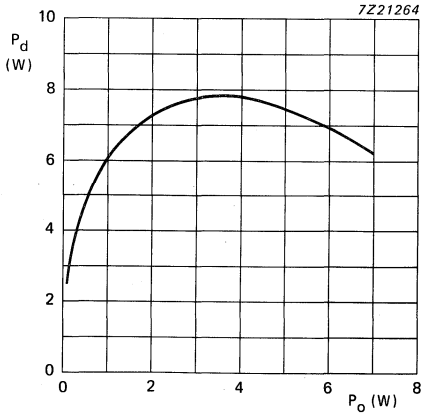


Fig. 7 Power dissipation as a function of output power; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; f = 1 kHz.

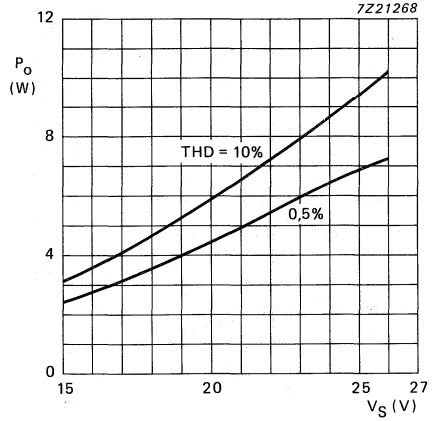


Fig. 8 Output power as a function of supply voltage; asymmetrical supply; $R_L = 8\ \Omega$; f = 1 kHz.

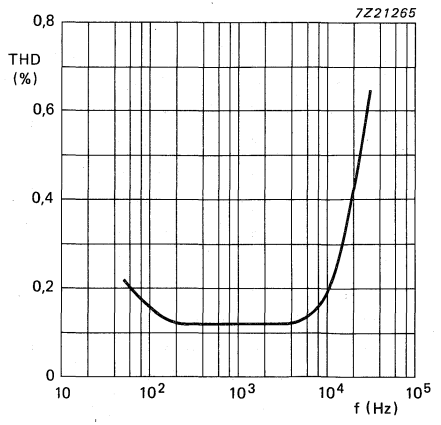


Fig. 9 Distortion as a function of frequency; asymmetrical supply; $V_S = 24$ V; $R_L = 8\ \Omega$; $P_o = 3$ W.

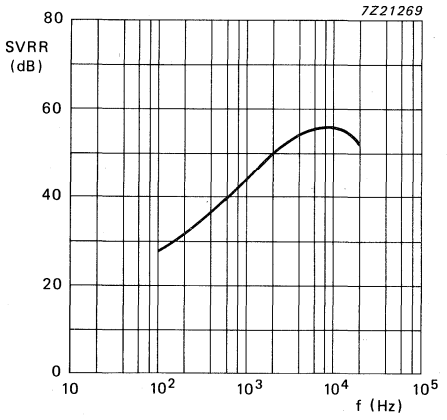
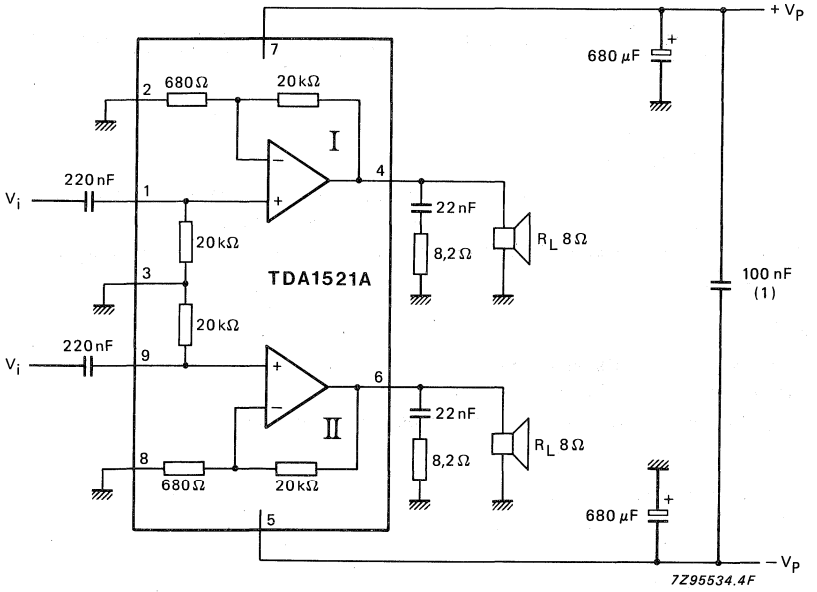


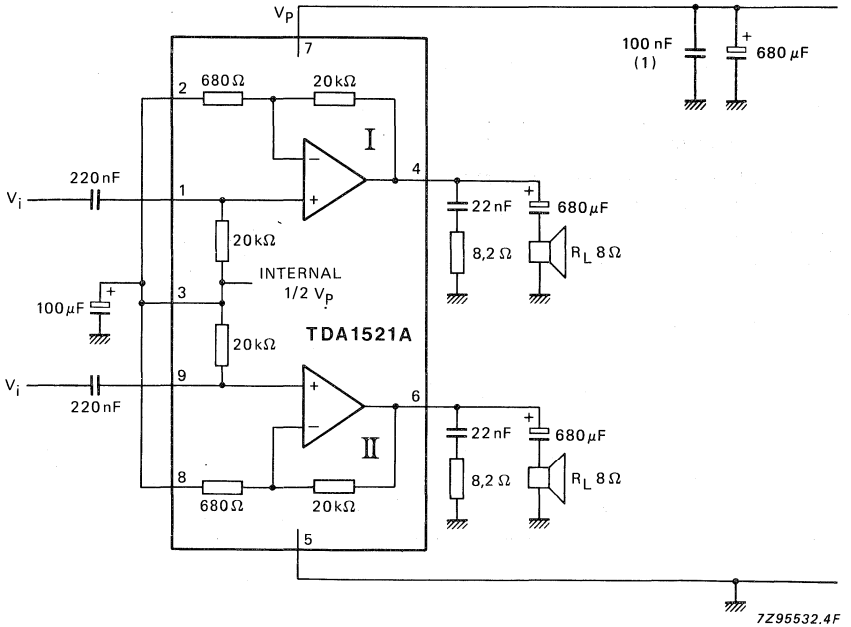
Fig. 10 Supply voltage ripple rejection; asymmetrical supply; $V_S = 24$ V; $V_{RR} = 200$ mW.

APPLICATION INFORMATION (continued)



(1) To be connected as close as possible to the I.C.

Fig. 11 Test and application circuit; symmetrical power supply.



(1) To be connected as close as possible to the I.C.

Fig. 12 Test and application circuit; asymmetrical power supply.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

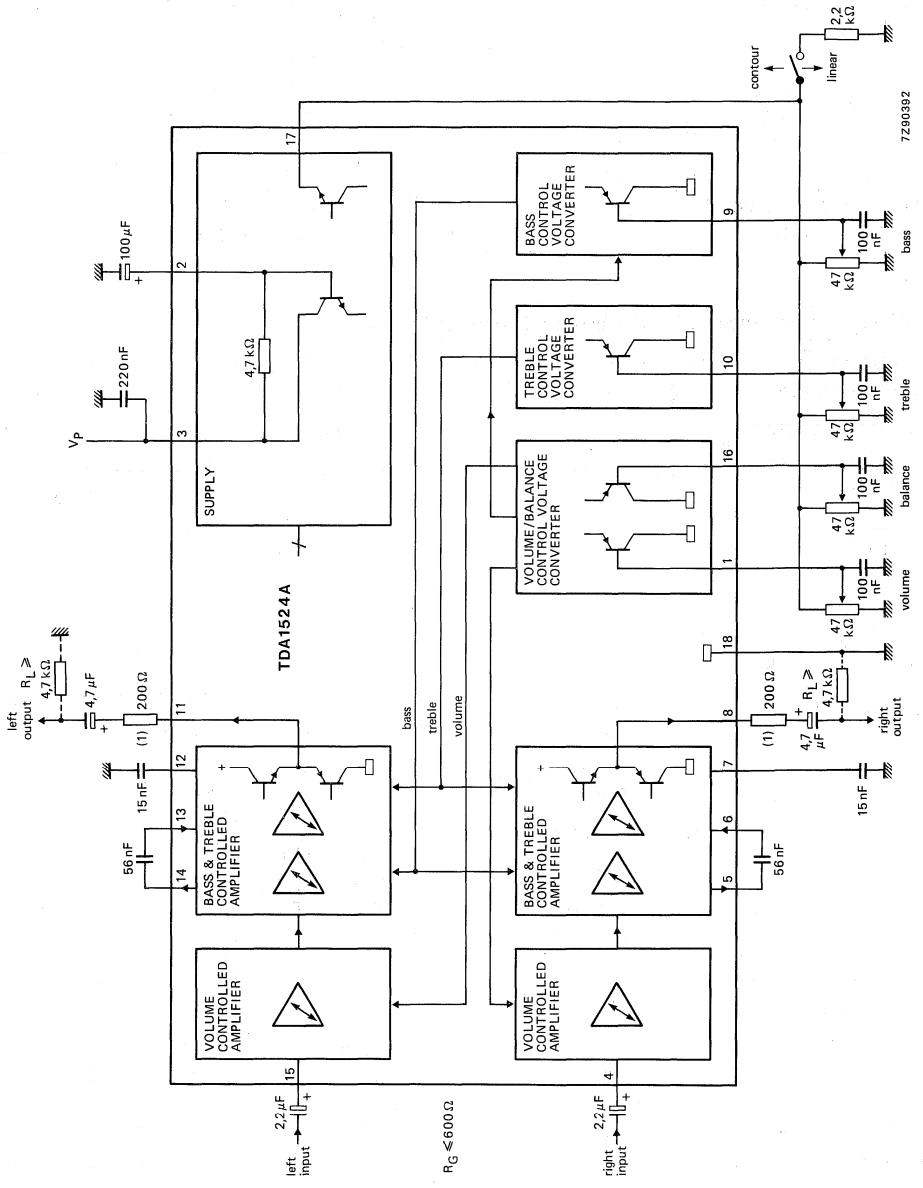
- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12 V
Supply current (pin 3)	$I_P = I_3$	typ.	35 mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	2,5 V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3 V
Volume control range	G_V		−80 to + 21,5 dB
Bass control range at 40 Hz	ΔG_V		−19 to + 17 dB
Treble control range at 16 kHz	ΔG_V	typ.	± 15 dB
Total harmonic distortion	THD	typ.	0,3 %
Output noise voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz; V_P = 12 V;			
for max. voltage gain	$V_{no(rms)}$	typ.	310 μV
for voltage gain G_V = −40 dB	$V_{no(rms)}$	typ.	100 μV
Channel separation at G_V = −20 to + 21,5 dB	α_{cs}	typ.	60 dB
Tracking between channels at G_V = −20 to + 26 dB	ΔG_V	max.	2,5 dB
Ripple rejection at 100 Hz	RR	typ.	50 dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5 V
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig. 1 Block diagram and application circuit with single-pole filter.

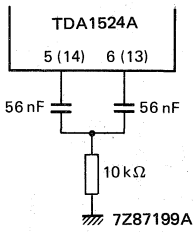


Fig. 2 Double-pole low-pass filter for improved bass-boost.

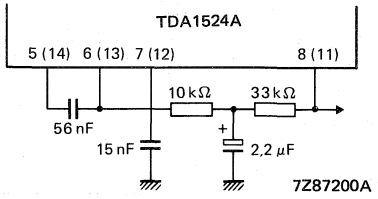


Fig. 3 D.C. feedback with filter network for improved signal handling.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	max.	20 V
Total power dissipation	P_{tot}	max.	1200 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

D.C. CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7,5	–	16,5	V
Supply current					
at $V_P = 8{,}5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
D.C. input levels (pins 4 and 15)					
at $V_P = 8{,}5$ V	$V_{4,15-18}$	3,8	4,25	4,7	V
at $V_P = 12$ V	$V_{4,15-18}$	5,3	5,9	6,6	V
at $V_P = 15$ V	$V_{4,15-18}$	6,5	7,3	8,2	V
D.C. output levels (pins 8 and 11) under all control voltage conditions with d.c. feedback (Fig. 3)					
at $V_P = 8{,}5$ V	$V_{8,11-18}$	3,3	4,25	5,2	V
at $V_P = 12$ V	$V_{8,11-18}$	4,6	6,0	7,4	V
at $V_P = 15$ V	$V_{8,11-18}$	5,7	7,5	9,3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8{,}5$ V	V_{17-18}	3,5	3,75	4,0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0,5	mA
linear (switch closed)	$-I_{17}$	1,5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10{,}8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4,5	–	$V_P/2 - V_{BE}$	V
D.C. control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1,0	–	4,25	V
using internal supply	$V_{1,9,10,16}$	0,25	–	3,8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

A.C. CHARACTERISTICS

$V_P = V_{3-18} = 8{,}5$ V; $T_{amb} = 25\ ^oC$; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4{,}7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Max. gain of volume (Fig. 5)	$G_{V\,max}$	20,5	21,5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; $G_V = 0$ dB (Fig. 6)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 7)	ΔG_V	–	–19 to + 17 ± 3		dB
Treble control range at 16 kHz (Fig. 8)	ΔG_V	–	± 15 ± 3	–	dB
Contour characteristics		see Figs 9 and 10			
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: $G_V = 20$ dB	$R_{i4,15}$	10	–	–	kΩ
$G_V = -40$ dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; $G_V = 0$ dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at $G_V = -20$ to + 21,5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0{,}5\ V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0{,}5\ V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1,5	dB
Tracking between channels					
for $G_V = 21{,}5$ to –26 dB					
f = 250 Hz to 6,3 kHz; balance adjusted at					
$G_V = 10$ dB	ΔG_V	–	–	2,5	dB

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with d.c. feedback (Fig. 3)					
Input signal handling					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 8,5 V; THD = 0,7%; f = 1 kHz (r.m.s. value)	$V_{i(rms)}$	1,8	2,4	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 12 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	1,4	–	–	V
at V_P = 15 V; THD = 0,7%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{i(rms)}$	2,0	3,2	–	V
Output signal handling (note 2 and note 3)					
at V_P = 8,5 V; THD = 0,5%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	1,8	2,0	–	V
at V_P = 8,5 V; THD = 10%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	–	2,2	–	V
at V_P = 12 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	2,5	3,0	–	V
at V_P = 15 V; THD = 0,5%; f = 40 Hz to 16 kHz (r.m.s. value)	$V_{o(rms)}$	–	3,5	–	V
Noise performance (V_P = 8,5 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	260	–	μV
for G_v = −3 dB (note 4)	$V_{no(rms)}$	–	70	140	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	890	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	360	–	μV
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	310	–	μV
for G_v = −16 dB (note 4)	$V_{no(rms)}$	–	100	200	μV
Output noise voltage; weighted as DIN 45405 of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	940	–	μV
for maximum emphasis of bass and treble (contour off; G_v = −40 dB)	$V_{no(m)}$	–	400	–	μV

parameter	symbol	min.	typ.	max.	unit
Noise performance (V_P = 15 V)					
Output noise voltage (unweighted; Fig. 15)					
at f = 20 Hz to 20 kHz (r.m.s. value; note 5)					
for maximum voltage gain (note 4)	$V_{no(rms)}$	–	350	–	μV
for G_V = 16 dB (note 4)	$V_{no(rms)}$	–	110	220	μV
Output noise voltage; weighted as DIN 45405					
of 1981, CCIR recommendation 468-2 (peak value)					
for maximum voltage gain (note 4)	$V_{no(m)}$	–	980	–	μV
for maximum emphasis of bass and treble					
(contour off; G_V = −40 dB)	$V_{no(m)}$	–	420	–	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 4)

$$R_i = \frac{160\ k\Omega}{1 + G_V}\ ;\ G_{V\ max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. Linear frequency response.
5. For peak values add 4,5 dB to r.m.s. values.

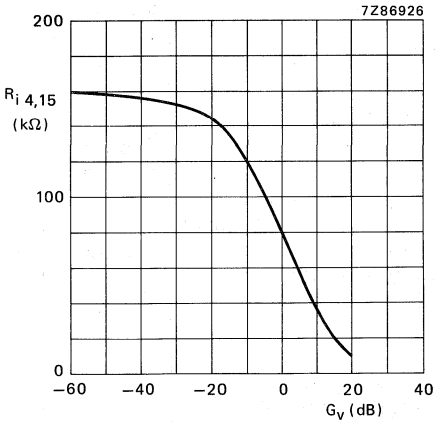


Fig. 4 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig. 1.

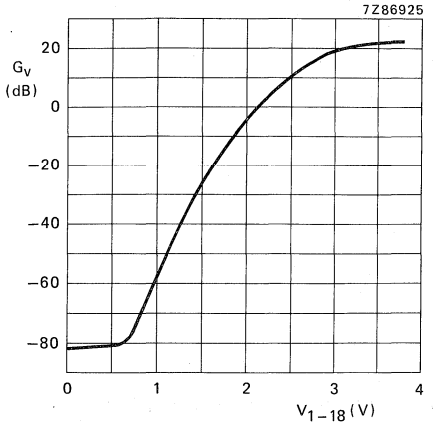


Fig. 5 Volume control curve; voltage gain (G_V) as a function of control voltage ($V_{1\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 1 kHz.

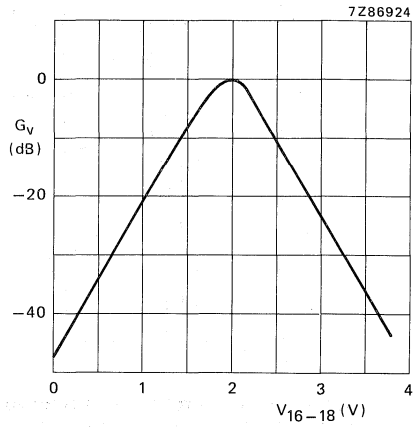


Fig. 6 Balance control curve; voltage gain (G_V) as a function of control voltage ($V_{16\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V.

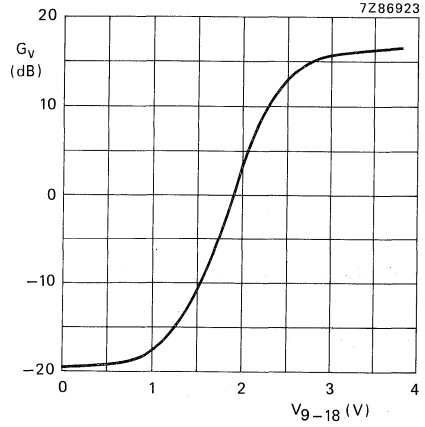


Fig. 7 Bass control curve; voltage gain (G_V) as a function of control voltage ($V_{9\text{-}18}$). Measured in Fig. 1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 40 Hz.

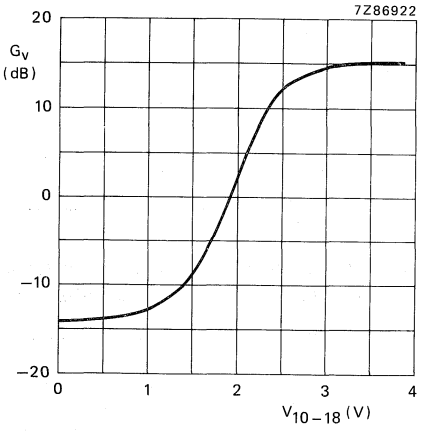


Fig. 8 Treble control curve; voltage gain (G_V) as a function of control voltage ($V_{10\text{-}18}$). Measured in Fig. 1 (internal potentiometer supply from pin 17 used); V_P = 8,5 V; f = 16 kHz.

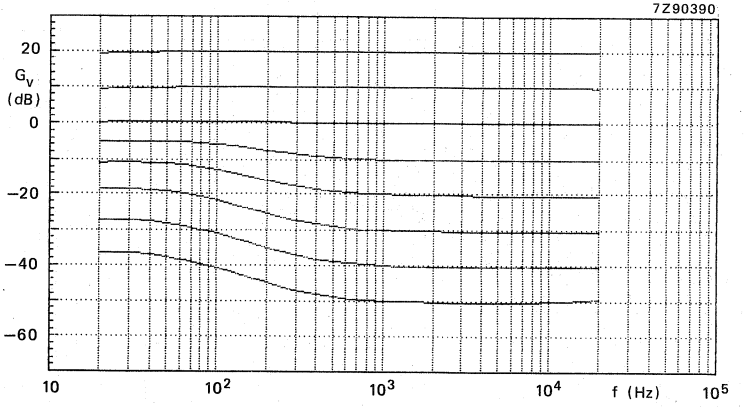


Fig. 9 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

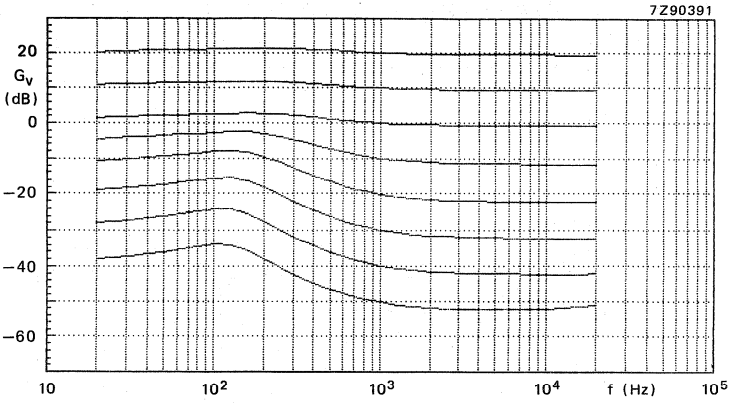


Fig. 10 Contour frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

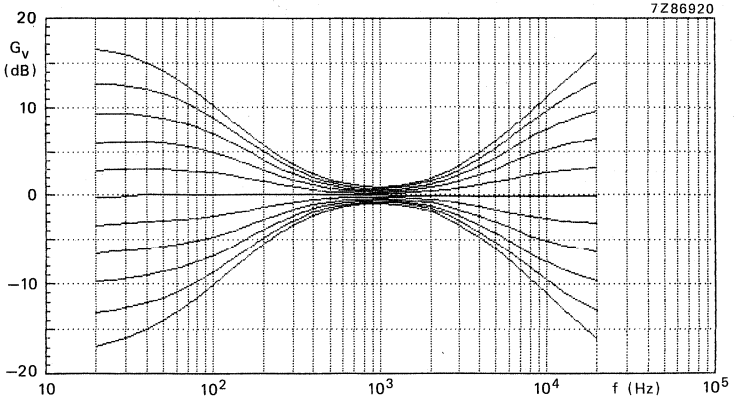


Fig. 11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with single-pole filter; V_P = 8,5 V.

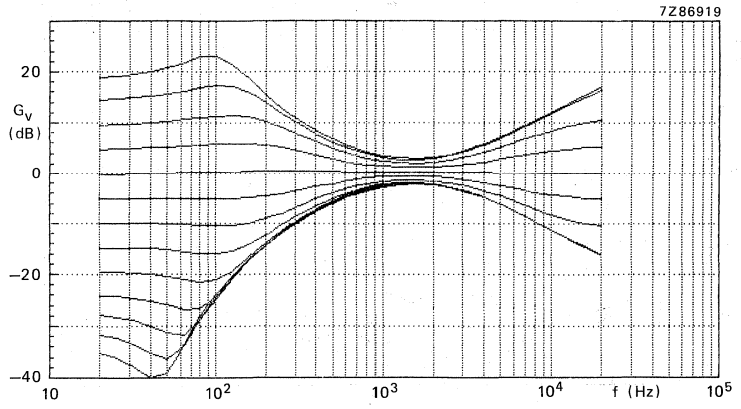


Fig. 12 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig. 1 with double-pole filter; V_P = 8,5 V.

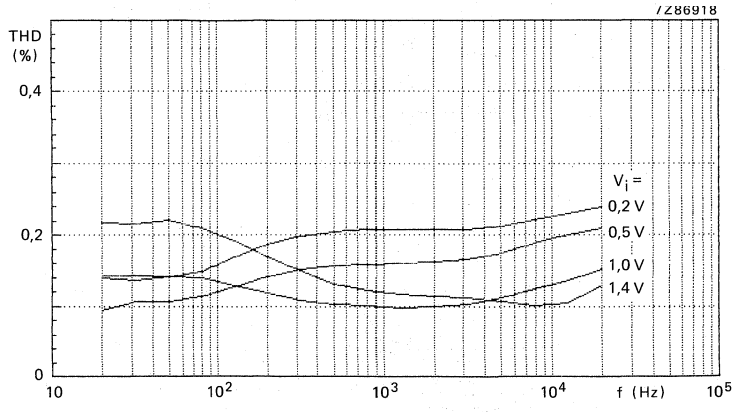


Fig. 13 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig. 1; V_P = 8,5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

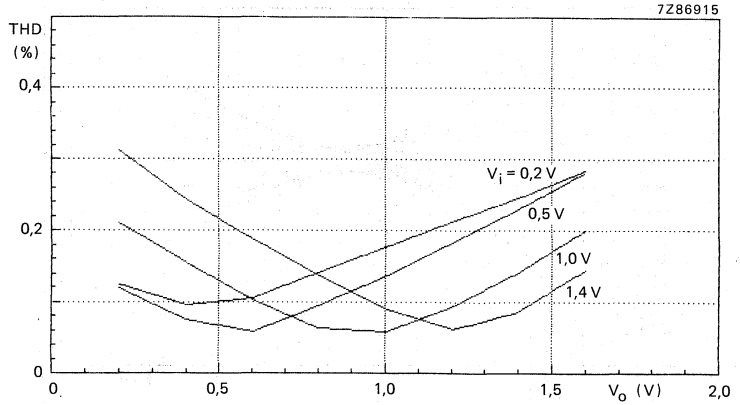
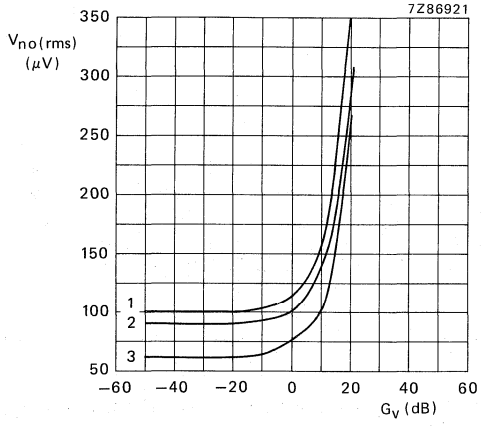


Fig. 14 Total harmonic distortion (THD); as a function of output voltage (V_o). Measured in Fig. 1; V_P = 8,5 V; f_i = 1 kHz.



(1) V_P = 15 V.
(2) V_P = 12 V.
(3) V_P = 8,5 V.

Fig. 15 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig. 1; f = 20 Hz to 20 kHz.

STEREO-TONE/VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The device is designed as an active stereo-tone/volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by DC voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Bass emphasis can be increased by a double-pole low-pass filter
- Wide power supply voltage range

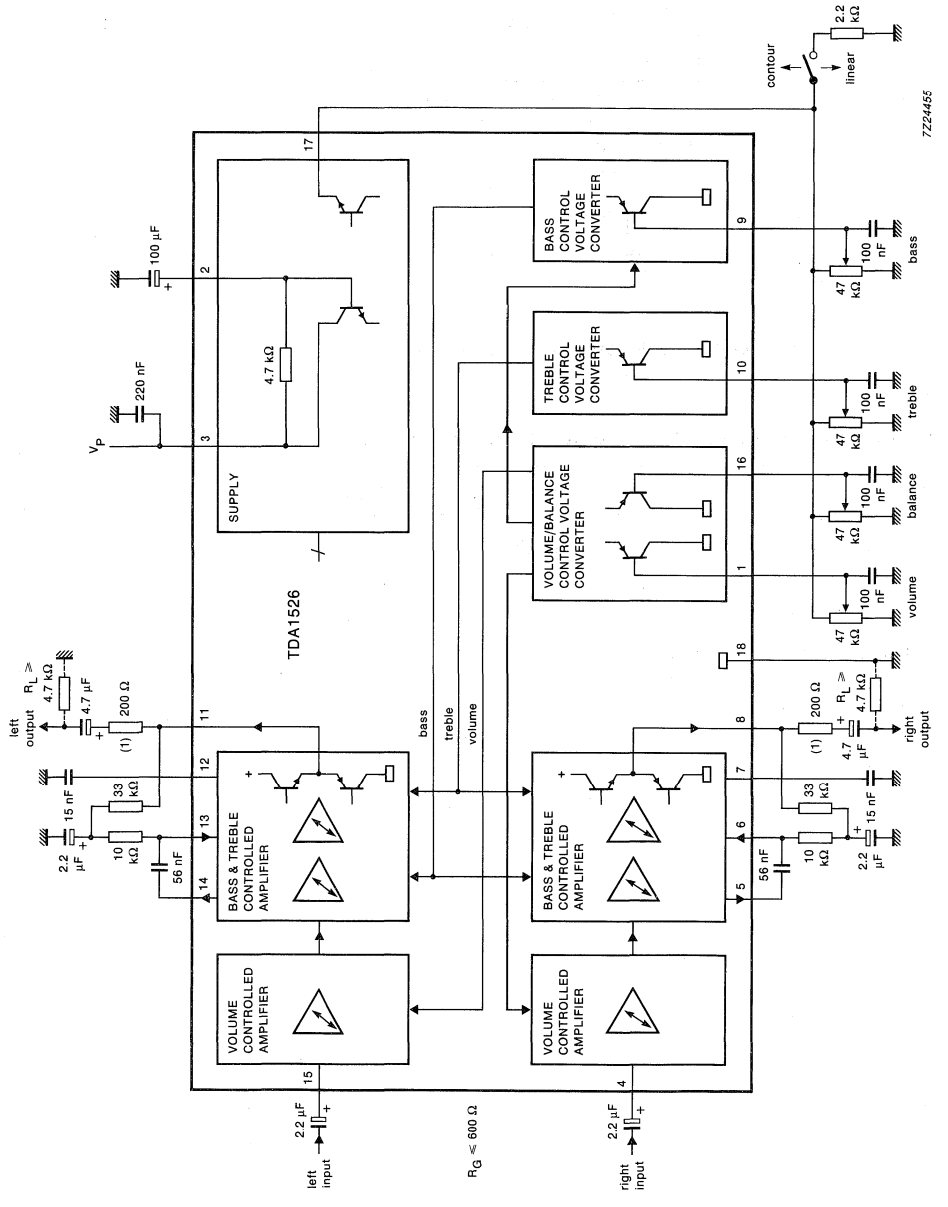
QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		V_P	7.5	12	16.5	V
Supply current (pin 3)	V_P = 12 V	I_P	25	35	45	mA
Signal handling with DC feedback	V_P = 8.5 to 15 V; THD = 0.7%; f = 1 kHz					
Input signal handling (RMS value)		$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (RMS value)	notes 2 and 3	$V_{o(rms)}$	1.8	2.0	–	V
Control range						
Maximum gain of volume	see Fig. 4	$G_{v\,max}$	20.5	21.5	23	dB
Volume control range	$G_{v\,max}/G_{v\,min}$	ΔG_v	90	100	–	dB
Balance control range	G_v = 0 dB; see Fig. 5	ΔG_v	–	–40	–	dB
Bass control range	at 40 Hz; see Fig. 6	ΔG_v	–	–19 to +17 ±3	–	dB
Treble control range	at 16 kHz; see Fig. 7	ΔG_v	–	±15 ±3	–	dB
Total harmonic distortion		THD	–	–	0.5	%
Noise performance	V_P = 12 V					
Output noise voltage (unweighted) at f = 20 Hz to 20 kHz for G_v = –16 dB	RMS value; note 4 note 5	$V_{no(rms)}$	–	100	200	μV
Signal processing						
Channel separation at G_v = –20 to 21.5 dB	f = 250 Hz to 10 kHz	α_{cs}	46	60	–	dB
Tracking between channels	f = 250 Hz to 6.3 kHz; balance at G_v = 10 dB					
for G_v = 21.5 to –26 dB		ΔG_v	–	–	2.5	dB
Ripple rejection	$V_{P(rms)} = \leqslant 200$ mV; f = 100 Hz; G_v = 0 dB	RR	35	50	–	dB
Operating ambient temperature range		T_{amb}	–30	–	+85	°C

For explanation of notes see **Notes to the characteristics.**

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) Series resistor is recommended in the event of the capacitive loads exceeding 200 pF.

Fig.1 Block diagram and application circuit with single-pole filter.

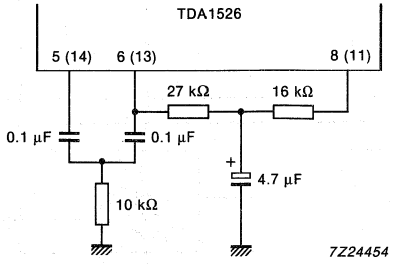


Fig.2 Double-pole low-pass filter for improved bass-boost.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	20	V
Total power dissipation	P_{tot}	–	1200	mW
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−30	+ 80	°C

DC CHARACTERISTICS

$V_P = V_{3-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	$V_P = V_{3-18}$	7.5	–	16.5	V
Supply current					
at $V_P = 8.5$ V	$I_P = I_3$	19	27	35	mA
at $V_P = 12$ V	$I_P = I_3$	25	35	45	mA
at $V_P = 15$ V	$I_P = I_3$	30	43	56	mA
DC input levels (pins 4 and 15)					
at $V_P = 8.5$ V	$V_{4,15-18}$	3.8	4.25	4.7	V
at $V_P = 12$ V	$V_{4,15-18}$	5.3	5.9	6.6	V
at $V_P = 15$ V	$V_{4,15-18}$	6.5	7.3	8.2	V
DC output levels (pins 8 and 11) under all control voltage conditions with DC feedback					
at $V_P = 8.5$ V	$V_{8,11-18}$	3.3	4.25	5.2	V
at $V_P = 12$ V	$V_{8,11-18}$	4.6	6.0	7.4	V
at $V_P = 15$ V	$V_{8,11-18}$	5.7	7.5	9.3	V
Pin 17					
Internal potentiometer supply voltage at $V_P = 8.5$ V	V_{17-18}	3.5	3.75	4.0	V
Contour on/off switch (control by I_{17})					
contour (switch open)	$-I_{17}$	–	–	0.5	mA
linear (switch closed)	$-I_{17}$	1.5	–	10	mA
Application without internal potentiometer supply voltage at $V_P \geqslant 10.8$ V (contour cannot be switched off)					
Voltage range forced to pin 17	V_{17-18}	4.5	–	$V_P/2-V_{BE}$	V
DC control voltage range for volume, bass, treble and balance (pins 1, 9, 10 and 16 respectively)					
at $V_{17-18} = 5$ V	$V_{1,9,10,16}$	1.0	–	4.25	V
using internal supply	$V_{1,9,10,16}$	0.25	–	3.8	V
Input current of control inputs (pins 1, 9, 10 and 16)	$-I_{1,9,10,16}$	–	–	5	μA

AC CHARACTERISTICS

$V_P = V_{3-18} = 8.5$ V; $T_{amb} = 25$ °C; measured in Fig. 1; contour switch closed (linear position); volume, balance, bass, and treble controls in mid-position; $R_G \leqslant 600\ \Omega$; $R_L \geqslant 4.7$ kΩ; $C_L \leqslant 200$ pF; f = 1 kHz; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Control range					
Maximum gain of volume (Fig. 4)	$G_{V\,max}$	20.5	21.5	23	dB
Volume control range; $G_{V\,max}/G_{V\,min}$	ΔG_V	90	100	–	dB
Balance control range; G_V = 0 dB (Fig. 5)	ΔG_V	–	–40	–	dB
Bass control range at 40 Hz (Fig. 6)	ΔG_V	–	–19 to +17 ±3		dB
Treble control range at 16 kHz (Fig. 7)	ΔG_V	–	±15 ±3	–	dB
Contour characteristics			see Figs 9 and 10		
Signal inputs, outputs					
Input resistance; pins 4 and 15 (note 1)					
at gain of volume control: G_V = 20 dB	$R_{i4,15}$	10	–	–	kΩ
G_V = –40 dB	$R_{i4,15}$	–	160	–	kΩ
Output resistance (pins 8 and 11)	$R_{o8,11}$	–	–	300	Ω
Signal processing					
Power supply ripple rejection					
at $V_{P(rms)} \leqslant 200$ mV; f = 100 Hz; G_V = 0 dB	RR	35	50	–	dB
Channel separation (250 Hz to 10 kHz)					
at G_V = –20 to +21.5 dB	α_{cs}	46	60	–	dB
Spread of volume control with					
constant control voltage $V_{1-18} = 0.5\,V_{17-18}$	ΔG_V	–	–	±3	dB
Gain tolerance between left and right					
channel $V_{16-18} = V_{1-18} = 0.5\,V_{17-18}$	$\Delta G_{V,L-R}$	–	–	1.5	dB
Tracking between channels					
for G_V = 21.5 to –26 dB					
f = 250 Hz to 6.3 kHz; balance adjusted at					
G_V = 10 dB	ΔG_V	–	–	2.5	dB

AC CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Signal handling with DC feedback					
Input signal handling at V_P = 8.5 V – 15 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{i(rms)}$	1.8	2.0	–	V
Output signal handling (note 2 and note 3) at V_P = 8.5 V; THD = 0.7%; f = 1 kHz (RMS value)	$V_{o(rms)}$	1.8	2.0	–	V
Noise performance (V_P = 12 V)					
Output noise voltage (unweighted; Fig. 14) at f = 20 Hz to 20 kHz (RMS value; note 4) for G_V = –16 dB (note 5)	$V_{no(rms)}$	–	100	200	μV

Notes to characteristics

1. Equation for input resistance (see also Fig. 3)

$$R_i = \frac{160\,k\Omega}{1 + G_V}; G_{V\,max} = 12.$$

2. Frequencies below 200 Hz and above 5 kHz have reduced voltage swing, the reduction at 40 Hz and at 16 kHz is 30%.
3. In the event of bass boosting the output signal handling is reduced. The reduction is 1 dB for maximum bass boost.
4. For peak values add 4.5 dB to RMS values.
5. Linear frequency response.

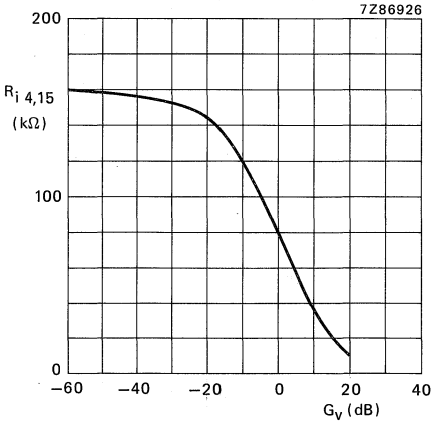


Fig.3 Input resistance (R_i) as a function of gain of volume control (G_V). Measured in Fig.1.

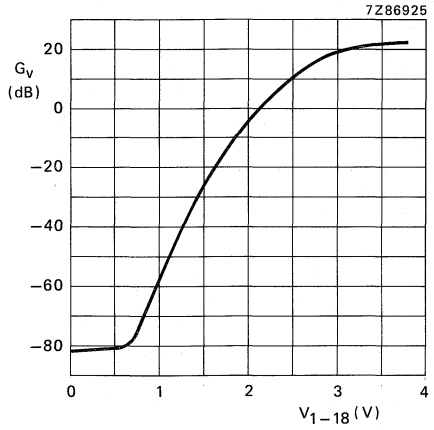


Fig.4 Volume control curve; voltage gain (G_V) as a function of control voltage (V_{1-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 1 kHz.

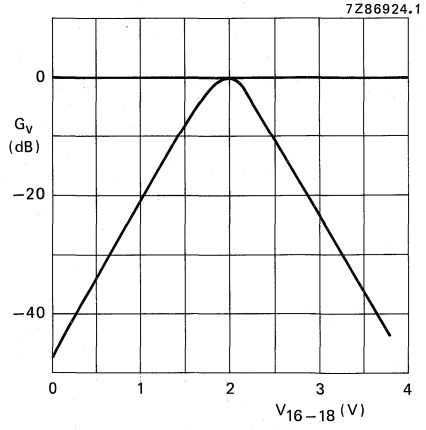


Fig.5 Balance control curve; voltage gain (G_V) as a function of control voltage (V_{16-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V.

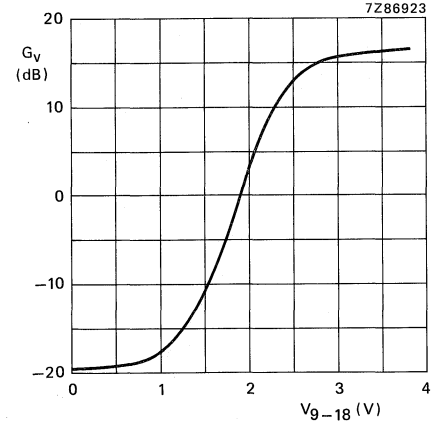


Fig.6 Bass control curve; voltage gain (G_V) as a function of control voltage (V_{9-18}). Measured in Fig.1 with single-pole filter (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 40 Hz.

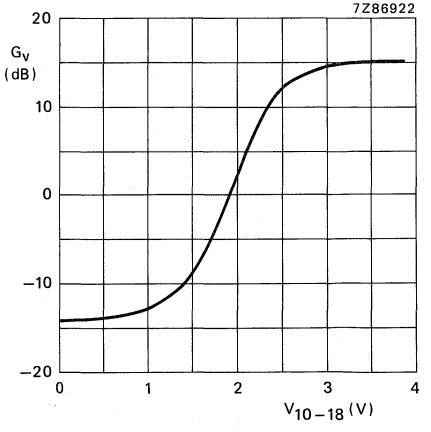


Fig.7 Treble control curve; voltage gain (G_V) as a function of control voltage (V_{10-18}). Measured in Fig.1 (internal potentiometer supply from pin 17 used); V_P = 8.5 V; f = 16 kHz.

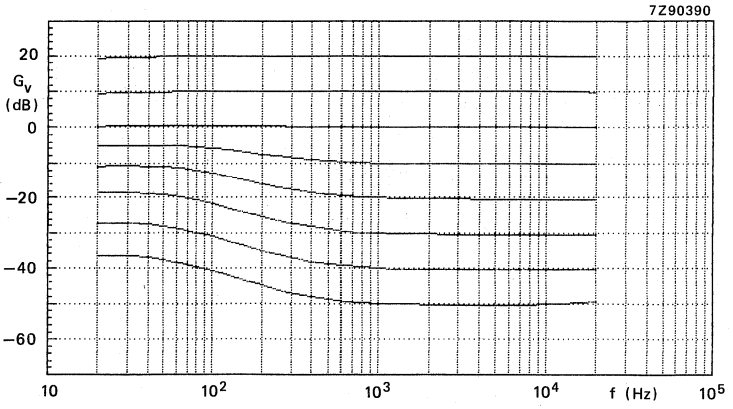


Fig.8 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

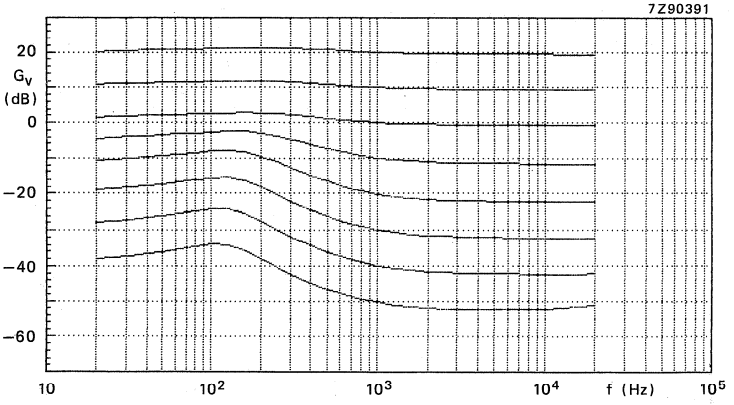


Fig.9 Contour frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

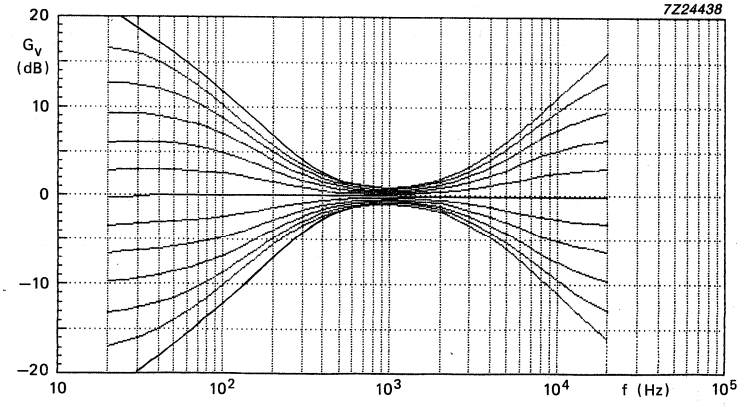


Fig.10 Tone control frequency response curves; voltage gain (G_v) as a function of audio input frequency. Measured in Fig.1 with single-pole filter; V_P = 8.5 V.

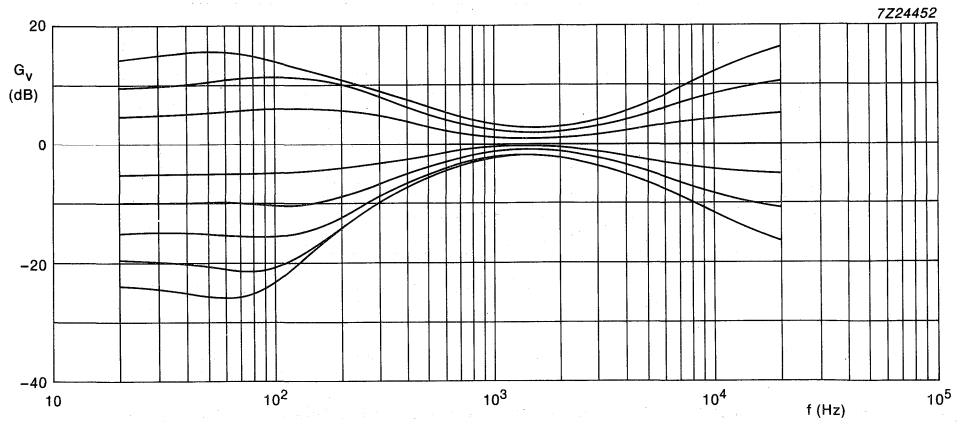


Fig.11 Tone control frequency response curves; voltage gain (G_V) as a function of audio input frequency. Measured in Fig.1 with double-pole filter; V_P = 8.5 V.

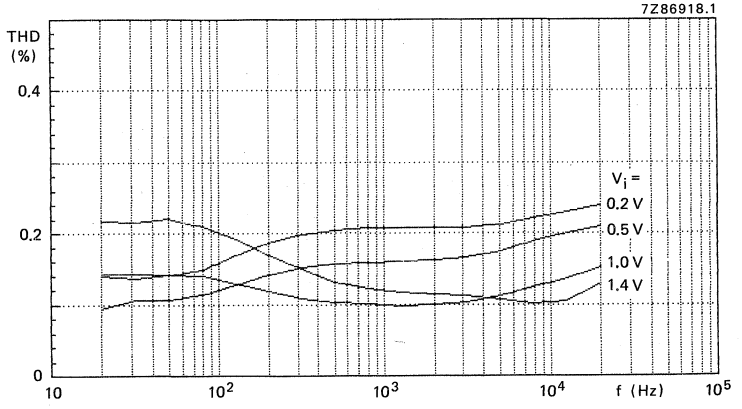


Fig.12 Total harmonic distortion (THD); as a function of audio input frequency. Measured in Fig.1; V_P = 8.5 V; volume control voltage gain at

$$G_V = 20 \log \frac{V_o}{V_i} = 0 \text{ dB}.$$

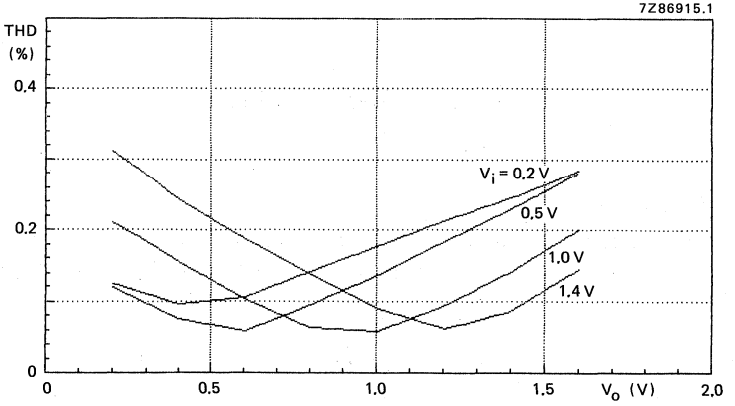


Fig.13 Total harmonic distortion (THD); as a function of output voltage (V_O). Measured in Fig.1; V_P = 8.5 V; f_i = 1 kHz.

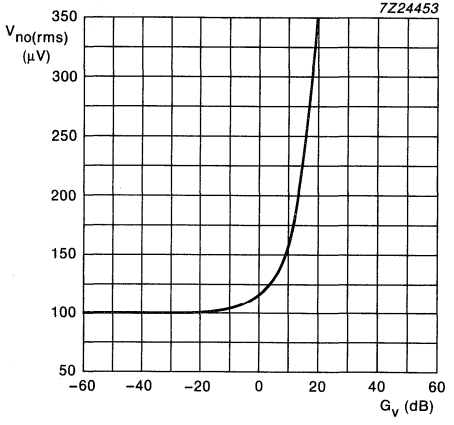


Fig.14 Noise output voltage ($V_{no(rms)}$; unweighted); as a function of voltage gain (G_V). Measured in Fig.1; V_P = 15 V; f = 20 Hz to 20 kHz.

DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time

QUICK REFERENCE DATA

Supply voltages			
pin 28	V_{DD}	typ.	5 V
pin 26	V_{DD1}	typ.	−5 V
pin 15	V_{DD2}	typ.	−15 V
Supply currents			
pin 28	I_{DD}	typ.	45 mA
pin 26	I_{DD1}	typ.	45 mA
pin 15	I_{DD2}	typ.	25 mA
Signal-to-noise ratio (full scale sine-wave) at analogue outputs (AOL; AOR)	S/N	typ.	95 dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB
Current settling time to ± 1 LSB	t_{cs}	typ.	1 μs
Maximum input bit rate at data input (pin 3)	BR_{max}	min.	6 Mbits/s
Maximum clock frequency			
at clock input (pin 2)	f_{BCKmax}	min.	6 MHz
at clock input (pin 4)	f_{SCKmax}	min.	12 MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	typ.	± 200 x 10^{-6} K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Total power dissipation	P_{tot}	typ.	850 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117).

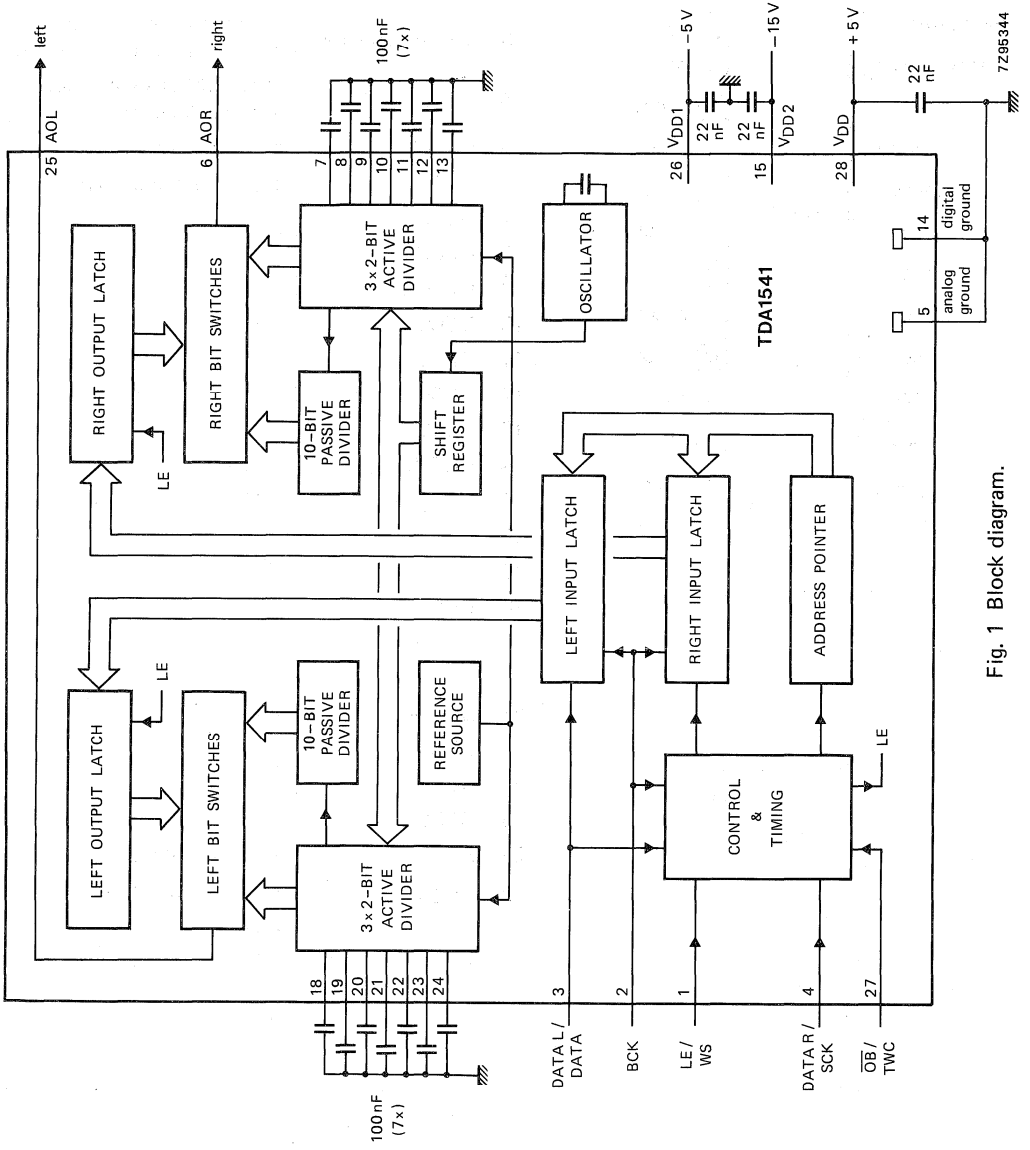


Fig. 1 Block diagram.

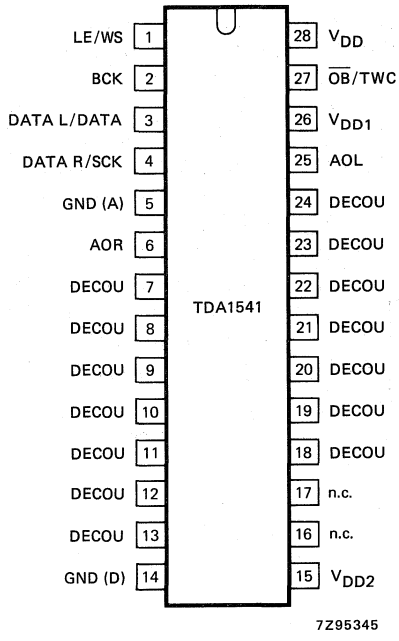


Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input / word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input / data input (selected format)
4	DATA R/SYS*	data right channel input / system clock input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	n.c.	not connected
17	n.c.	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

FUNCTIONAL DESCRIPTION

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analogue outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary.

The format of data input signals is shown in figures 3, 4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	SCK
+5 V	time MUX TWC	WS	BCK	DATA TWC	SCK

Where:

LE = latch enable
WS = word select
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 28	V_{DD}	0 to + 7	V
pin 26	V_{DD1}	0 to −7	V
pin 15	V_{DD2}	0 to −17	V
Crystal temperature range	T_{XTAL}	−55 to + 150	°C
Storage temperature range	T_{stg}	−55 to + 150	°C
Operating ambient temperature range	T_{amb}	−20 to + 70	°C
Electrostatic handling*	V_{es}	−1000 to + 1000	V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	35	K/W

* Discharging a 250 pF capacitor through a 1 kΩ series resistor.

CHARACTERISTICS

V_{DD} = + 5 V; V_{DD1} = −5 V; V_{DD2} = −12 V; T_{amb} = + 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage ranges					
pin 28	V_{DD}	4,0	5,0	6,0	V
pin 26	$-V_{DD1}$	4,5	5,0	6,0	V
pin 15	$-V_{DD2}$	14	15	16	V
Supply currents					
pin 28	I_{DD}	–	45	tbf	mA
pin 26	$-I_{DD1}$	–	45	tbf	mA
pin 15	$-I_{DD2}$	–	25	tbf	mA
Resolution	Res	–	16	–	bits
Inputs					
Input current (pin 3 and pin 4)					
digital inputs LOW (< 0,8 V)	I_{IL}	–	–	tbf	mA
digital inputs HIGH (> 2,0 V)	I_{IH}	–	–	tbf	μA
Input frequency					
at clock input (pin 4)	f_{SCK}	–	–	12	MHz
at clock input (pin 2)	f_{BCK}	–	–	6	MHz
at data inputs (pin 3 and pin 4)	f_{DAT}	–	–	6	MHz
at word select input (pin 1)	f_{WS}	–	–	200	kHz
Input capacitance of digital inputs	C_I	–	12	–	pF
Oscillator					
Oscillator frequency with internal capacitor	f_{osc}	150	200	250	kHz
Analogue outputs (AOL; AOR)					
Output voltage compliance	V_{OC}	tbf	–	tbf	mV
Full scale current	I_{FS}	3,4	4,0	4,6	mA
Zero scale current	$\pm I_{ZS}$	–	tbf	–	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 200 \times 10^{-6}$	–	K^{-1}
Linearity error integral					
at T_{amb} = 25 °C	E_1	–	0,5	–	LSB
at T_{amb} = −20 to + 70 °C	E_1	–	tbf	–	LSB
Linearity error differential					
at T_{amb} = 25 °C	E_{d1}	–	0,5	1	LSB
at T_{amb} = −20 to + 70 °C	E_{d1}	–	tbf	–	LSB

parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio + THD*	S/N	90	95	–	dB
Settling time to ± 1 LSB	t_{cs}	–	1	–	μs
Channel separation	α	80	tbf	–	dB
Unbalance between outputs	ΔI_{FS}	–	0,1	0,2	dB
Time delay between outputs	t_d	–	–	1	μs
Power supply ripple rejection**					
V_{DD} = + 5 V	RR	–	tbf	–	dB
V_{DD1} = −5 V	RR	–	tbf	–	dB
V_{DD2} = −15 V	RR	–	tbf	–	dB
Signal-to-noise ratio at bipolar zero	S/N	–	−100	–	dB
Timing (see Figs 3, 4 and 5)					
Rise time	t_r	–	–	35	ns
Fall time	t_f	–	–	35	ns
Bit clock cycle time	t_{CY}	160	–	–	ns
Bit clock HIGH time	t_{HB}	48	–	–	ns
Bit clock LOW time	t_{LB}	48	–	–	ns
Bit clock fall time to latch rise time	t_{FBRL}	0	–	–	ns
Bit clock rise time to latch fall time	t_{RBFL}	0	–	–	ns
Data set-up time to bit clock	t_{SDB}	32	–	–	ns
Data hold time to bit clock	t_{HDB}	0	–	–	ns
Data set-up time to system clock	t_{SDS}	32	–	–	ns
Word select hold time to system clock	t_{HWS}	0	–	–	ns
Word select set-up time to system clock	t_{SWS}	32	–	–	ns
Bit clock fall time to system clock rise time	t_{FBRS}	32	–	–	ns
System clock rise time to bit clock fall time	t_{RSFB}	32	–	–	ns
System clock fall time to bit clock rise time	t_{FSRB}	50	–	–	ns
Bit clock rise time to system clock fall time	t_{RBFS}	0	–	–	ns
Latch enable LOW time	t_{LLE}	20	–	–	ns
Latch enable HIGH time	t_{HLE}	32	–	–	ns

* Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.

** V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

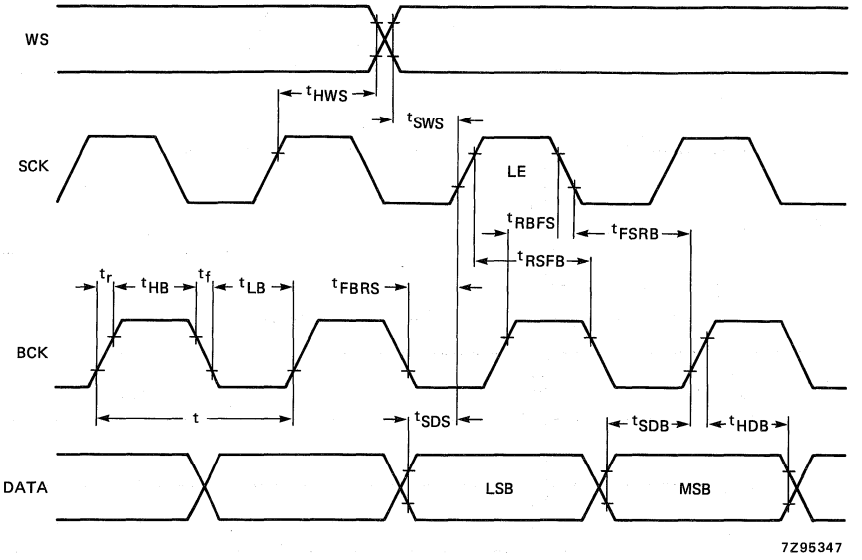


Fig. 3 Format of input signals; time multiplexed at $f_{SCK} = f_{BCK}$ (I^2S format).

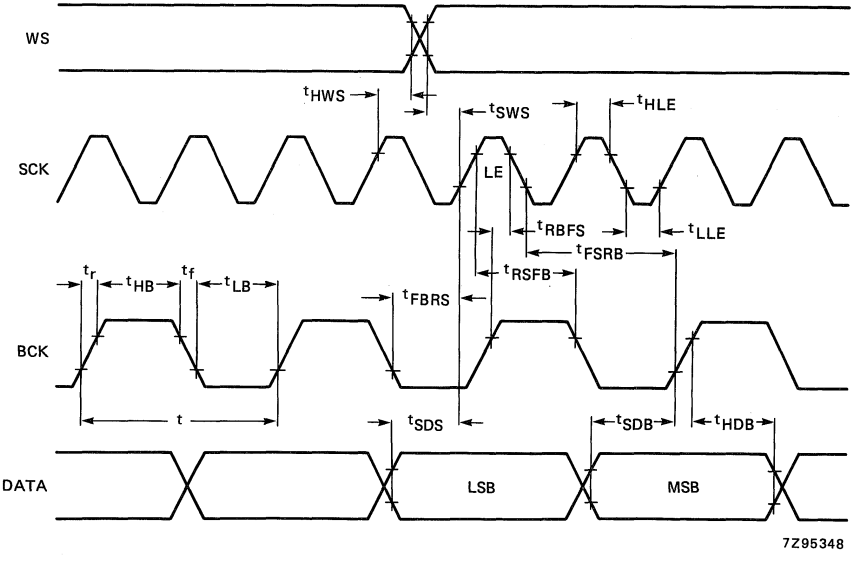


Fig. 4 Format of input signals; **time multiplexed** at $f_{SCK} = 2 \times f_{BCK}$.

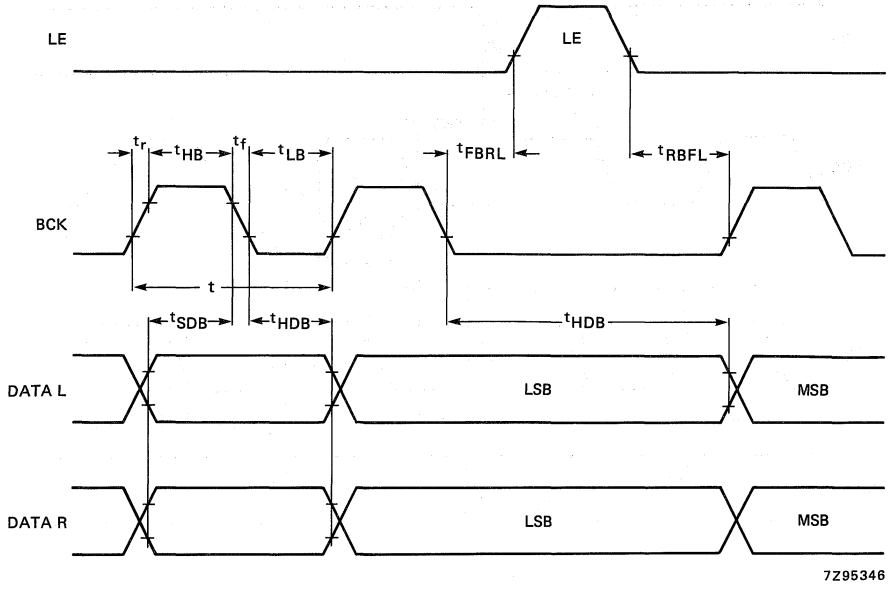


Fig. 5 Format of input signals; **simultaneous data.**

Data sheet	
status	Product specification
date of issue	February 1991

TDA1541A

Stereo high performance 16-bit DAC

FEATURES

- High sound quality
- High performance: low noise and distortion, wide dynamic range
- 4 x or 8 x oversampling possible
- Selectable two-channel input format
- TTL compatible inputs

GENERAL DESCRIPTION

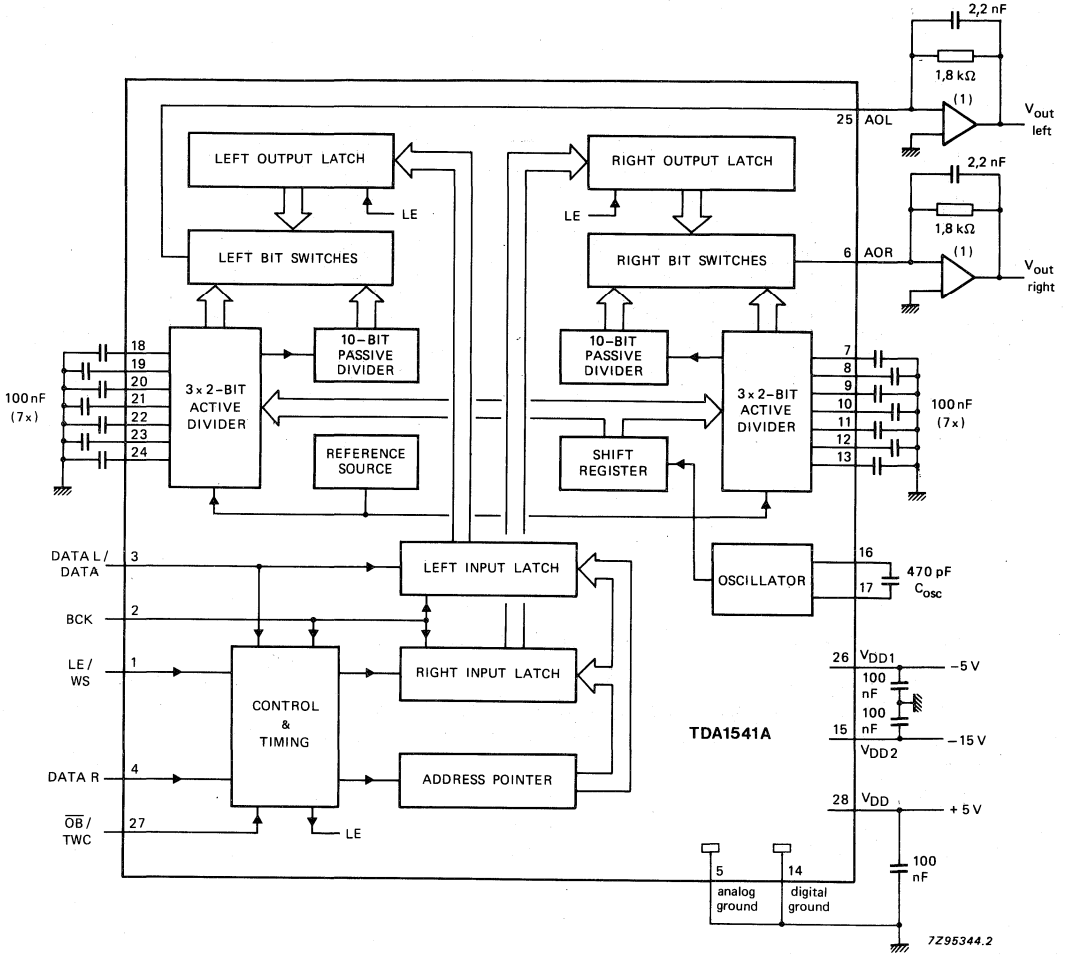
The TDA1541A is a stereo 16-bit digital-to-analog converter (DAC). The ingenious design of the electronic circuit guarantees a high performance and superior sound quality. The TDA1541A is therefore extremely suitable for use in top-end high-fi digital audio equipment such as high quality Compact Disc players or digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1541A	28	DIL	plastic	SOT117

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
THD	total harmonic distortion	including noise	-	−95	−90	dB
		at 0 dB	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise	-	−42	-	dB
		at −60 dB	-	0.79	-	%
NL	non-linearity	at T_{amb} = −20 to +85 °C	-	0.5	1.0	LSB
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input; (pin 3 and 4)		-	-	6.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	6.4	MHz
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	±200 x 10^{-6}	-	K^{-1}
T_{amb}	operating ambient temperature range		−40	-	+85	°C
P_{tot}	total power dissipation		-	700	-	mW



(1) TDA1542
(2) 2 x NE5534 or equivalent

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LE/WS*	1	latch enable input / word select input
BCK*	2	bit clock input
DATA L /DATA*	3	data left channel input / data input (selected format)
DATA R*	4	data right channel input
GND(A)	5	analog ground
AOR	6	right channel output
DECOU	7 to 13	decoupling
GND (D)	14	digital ground
V_{DD2}	15	−15 V supply voltage
COSC	16,17	oscillator
DECOU	18 to 24	decoupling
AOL	25	left channel output
V_{DD1}	26	−5 V supply voltage
$\overline{OB}$/TWC*	27	mode select input
V_{DD}	28	+5 V supply voltage

* See Table 1 data selection input.

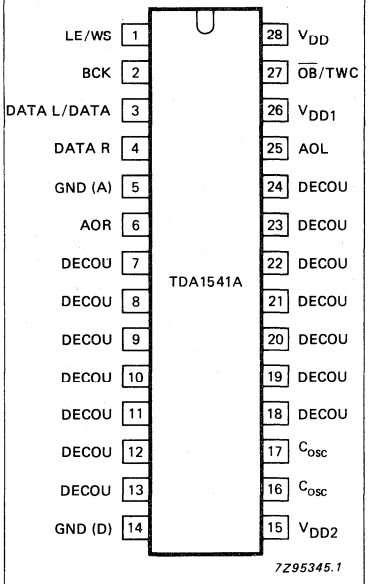


Fig.2 Pin configuration

FUNCTIONAL DESCRIPTION

The TDA1541A accepts input sample formats in time multiplexed mode or simultaneous mode up to 16-bit word length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling facilitates application in 8 x oversampling systems (44.1 kHz to 352.8 kHz or 48 kHz to 384 kHz) with the associated simple analog filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With the input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. The converted samples appear at the output, at the first positive going transition of the bit clock signal after a negative going transition of the word select signal.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but the data format must be in the two's complement.

When input $\overline{OB}$/TWC input is connected to V_{DD1} the two channels of data (L/R) are input simultaneously via DATA L and DATA R, accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary. The converted samples appear at the output at the positive going transition of the latch enable signal.

The format of the data input signals is shown in fig.4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	not used
+5 V	time MUX TWC	WS	BCK	DATA TWC	not used

Where:

LE = latch enable
WS = word select, LOW = left channel; HIGH = right channel
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = mulitplexed offset binary
MUX TWC = multiplexed two's complement = I²S-format

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage; pin 28		0	7	V
$-V_{DD1}$	supply voltage; pin 26		0	7	V
$-V_{DD2}$	supply voltage; pin 15		0	17	V
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−40	+85	°C
V_{es}	electrostatic handling*		−1000	+1000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	30	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; $-V_{DD1}$ = 5 V; $-V_{DD2}$ = 15 V; T_{amb} = +25 °C; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage; pin 28		4.5	5.0	5.5	V
$-V_{DD1}$	supply voltage; pin 26		4.5	5.0	5.5	V
$-V_{DD2}$	supply voltage; pin 15		14.0	15.0	16.0	V
$V_{GND(A)}$ $-V_{GND(D)}$	voltage difference between analog and digital ground		−0.3	0	+0.3	V
I_{DD}	supply current; pin 28		-	27	40	mA
$-I_{DD1}$	supply current; pin 26		-	37	50	mA
$-I_{DD2}$	supply current; pin 15		-	25	35	mA
Inputs						
$-I_{IL}$	input current pins (1, 2, 3 and 4) digital inputs LOW	V_I = 0.8 V	-	-	0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
$\lvert I_{\overline{OB/TWC}}\rvert$	Digital input currents (pin 27) +5 V		-	-	1	µA
$\lvert I_{\overline{OB/TWC}}\rvert$	0 V		-	-	20	µA
$\lvert I_{\overline{OB/TWC}}\rvert$	−5 V		-	-	40	µA
f_{BCK}	input frequency/bit rate clock input pin 2		-	-	6.4	MHz
BR	bit rate data input pin 3 and 4		-	-	6.4	Mbits/s
f_{WS}	word select input pin 2		-	-	200	kHz
f_{LE}	latch enable input 1		-	-	200	kHz
C_I	input capacitance of digital inputs		-	12	-	pF
Analog outputs (AOL; AOR; see note 1)						
Res	resolution		-	16	-	bits
I_{FS}	full scale current		3.4	4.0	4.6	mA
$\lvert I_{ZS}\rvert$	zero scale current		-	25	50	nA
T_{CFS}	full scale temperature coefficient	T_{amb} = −20 to +85 °C	-	±200 x 10^{-6}	-	K^{-1}
Analog outputs (V_{ref})						
E_L	integral linearity error	T_{amb} = 25 °C	-	0.5	1.0	LSB
E_L	integral linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = 20°C, note 2	-	0.5	1.0	LSB
E_{dL}	differential linearity error	T_{amb} = −20 to +85°C	-	-	1.0	LSB
THD	total harmonic distortion	at 0 dB; note 3	−100	-	dB	
			-	0.0010	-	%
THD	total harmonic distortion	including noise at 0 dB;	-	−95	−90	dB
		note 3, Fig.3	-	0.0018	0.0032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−42	-	dB
		note 3, Fig.3	-	0.79	-	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		90	98	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.1	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	-	0.2	µs
SSVR	supply voltage ripple rejection	V_{DD} = +5 V; note 4	-	−76	-	dB
SSVR	supply voltage ripple rejection	V_{DD1} = −5 V; note 4	-	−84	-	dB
SSVR	supply voltage ripple rejection	V_{DD2} = −15 V; note 4	-	−58	-	dB
S/N	signal-to-noise ratio	at bipolar zero	-	110	-	dB
S/N	signal-to-noise ratio	at full scale	98	104	-	dB
Timing (Fig.4 and 5)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		156	-	-	ns
t_{HB}	bit clock HIGH time		46	-	-	ns
t_{LB}	bit clock LOW time		46	-	-	ns
t_{FBRL}	bit clock fall time to latch enable rise time		0	-	-	ns
t_{RBFL}	bit clock rise time to latch enable fall time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		0	-	-	ns
$t_{HD;WS}$	word select hold time		0	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. To ensure no performance losses, permitted output voltage compliance is ±25 mV maximum.

2. Selections have been made with respect to the maximum differential linearity error (E_{dL}):

   TDA1541A/N2 bit 1-16 $E_{dL} < 1$ LSB

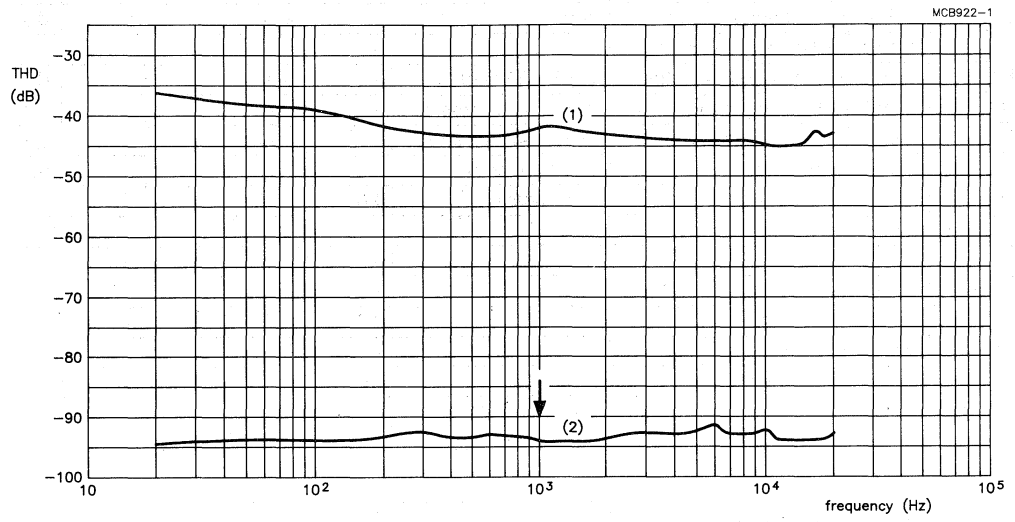
   TDA1541A/N2/R1 bit 1-16 $E_{dL} < 2$ LSB

   TDA1541A/N2/S1 bit 1-7 $E_{dL} < 0.5$ LSB
   bit 8-15 $E_{dL} < 1$ LSB
   bit 16 $E_{dL} < 0.75$ LSB

   The S1 version has been specially selected to achieve extremely good performance even for small signals.

3. Measured using a 1 kHz sinewave generated at a sampling rate of 176.4 kHz.

4. V_{ripple} = 100 mV and f_{ripple} = 100 Hz.

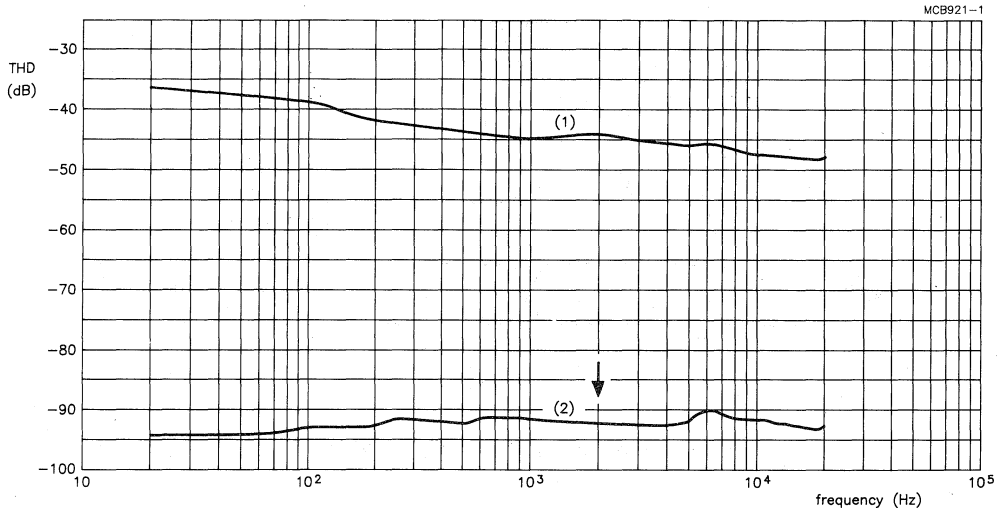


(1) Measured including all distortion plus noise at a signal level of −60 dB
(2) Measured including all distortion plus noise at a signal level of −0 dB

Fig.3a Distortion as a function of frequency (4FS)

Notes to Fig.3a

- The sample frequency 4FS: 176.4 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.



(1) Measured including all distortion plus noise at a signal level of –60 dB
(2) Measured including all distortion plus noise at a signal level of –0 dB

Fig.3b Distortion as a function of frequency (8FS)

Notes to Fig.3b

- The sample frequency 8FS: 352.8 kHz.
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.

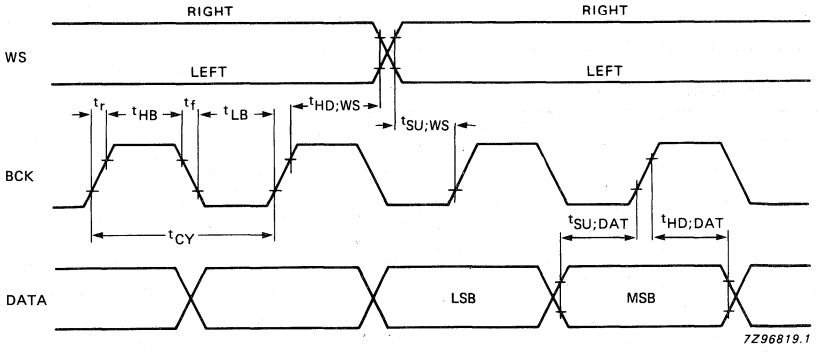


Fig.4 Format of input signals; time multiplexed (I^2S format).

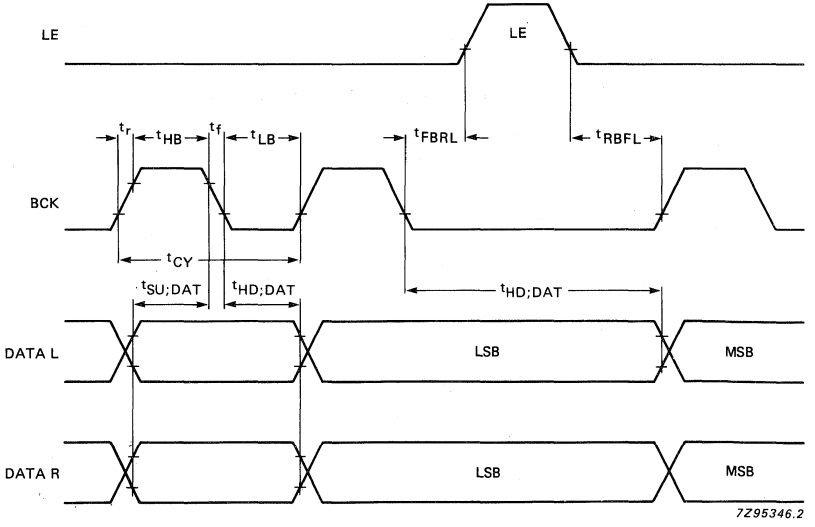


Fig.5 Format of input signals; simultaneous data.

ACTIVE ELEMENT FOR POST FILTERING

GENERAL DESCRIPTION

The TDA1542 is a dual channel monolithic integrated circuit encapsulated in a 28 pin DIL plastic package. Each channel incorporates five high performance amplifiers and is designed for use in hi-fi digital audio equipment such as a compact disc player.

Features

- Mute function for click and plop free switching (on and off)
- Switch function for activating a de-emphasis circuit
- Two separate output amplifiers per channel
- Flexible use of filtering
- Extremely low distortion
- High slew-rate input amplifier

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Input amplifier (A)						
Slew-rate		$\Delta V/\Delta t$	–	30	–	V/μs
Line amplifier (D)						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 1 kΩ	THD	–	–110	–100	dB
Channel separation		α	95	100	–	dB
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)		$V_{O(rms)}$	–	6	–	V
Signal to noise ratio		S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	–110	–100	dB
Channel separation		α	95	100	–	dB
Filter amplifiers (A, B and C)						
Amplifiers conform to line amplifier D, without mute function						

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT117).

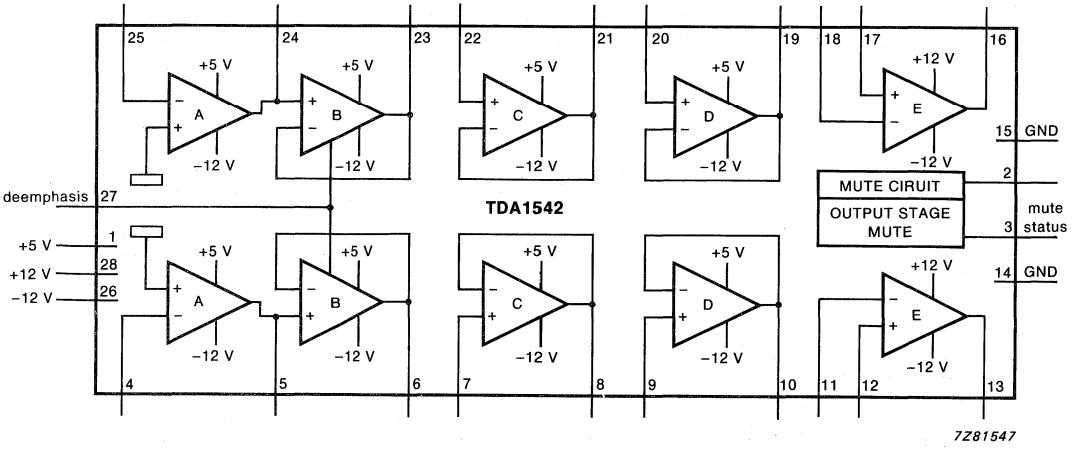


Fig. 1 Block diagram.

PINNING

1	+5 V supply voltage (V_{DD2})	15	Ground left
2	Mute timing capacitor	16	Amplifier E left output
3	Mute status	17	Amplifier E left non-inverting input
4	Amplifier A right input	18	Amplifier E left inverting input
5	Amplifier A right output/Amplifier B input	19	Amplifier D left output
6	Amplifier B right output	20	Amplifier D left input
7	Amplifier C right input	21	Amplifier C left output
8	Amplifier C right output	22	Amplifier C left input
9	Amplifier D right input	23	Amplifier B left output
10	Amplifier D right output	24	Amplifier A left output/Amplifier B input
11	Amplifier E right inverting input	25	Amplifier A left input
12	Amplifier E right non-inverting input	26	−12 V supply voltage (V_{DD3})
13	Amplifier E right output	27	De-emphasis on/off function
14	Ground right	28	+12 V supply voltage (V_{DD1})

FUNCTIONAL DESCRIPTION

The TDA1542 is a high performance, dual channel device designed to perform post filtering in a compact disc player. Since only the active part of the filter is integrated, the user has the option of selecting the desired filter type e.g. Bessel or Cauer etc. Each channel contains two separate output amplifiers, one with fixed gain for line output and the other with variable gain for driving low/high impedance headphones.

A switchable buffer amplifier is incorporated to enable the deemphasis function without producing clicks.

A mute circuit is incorporated to prevent spurious signals appearing at the output.

Both amplifiers are muted, for a preset period of time, when the 5 V supply is switched on or off. An external capacitor determines the mute time. When the mute time has elapsed the signal path is switched directly to the output, without clicks. The mute circuit status is available externally.

The TDA1542 is designed to operate over a wide supply voltage range.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage ranges					
pin 28		V_{DD1}	0	18	V
pin 1		V_{DD2}	0	7	V
pin 26		$-V_{DD3}$	0	18	V
Storage temperature range		T_{stg}	−65	150	°C
Operating ambient temperature range		T_{amb}	−30	85	°C
Electrostatic handling *		V_{es}	−	600	V

THERMAL RESISTANCE

From junction to ambient $R_{th\ j\text{-}a}$ 30 K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

DC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage						
pin 28		V_{DD1}	4.75	12.0	13.0	V
pin 1		V_{DD2}	4.5	5.0	5.5	V
pin 26		$-V_{DD3}$	4.75	12.0	13.0	V
Supply current						
pin 28		I_{DD1}	–	12	18	mA
pin 1		I_{DD2}	–	34	51	mA
pin 26		$-I_{DD3}$	–	46	69	mA
Input current						
Amplifier A (pins 4 and 25)		I_{IA}	–	1	2	μA
Amplifier C (pins 7 and 22)		I_{IC}	–	320	600	nA
Amplifier D (pins 9 and 20)		I_{ID}	–	50	150	nA
Amplifier E (pins 11 and 18)		I_{IE}	–	300	600	nA
Amplifier E (pins 12 and 17)		I_{IE}	–	30	150	nA
Offset voltage						
Amplifier A (pins 4 and 25)		$\lvert V_{IAos}\rvert$	–	1.2	7.0	mV
Amplifier B (pins 6 and 23)		$\lvert V_{IBos}\rvert$	–	0.5	7.0	mV
Amplifier C (pins 8 and 21)		$\lvert V_{ICos}\rvert$	–	0.6	7.0	mV
Amplifier D (pins 10 and 19)		$\lvert V_{IDos}\rvert$	–	1.0	3.0	mV
Amplifier E (pins 11 and 18)		$\lvert V_{IEos}\rvert$	–	0.7	3.0	mV
Mute timing capacitor (pin 2)						
Switch-on voltage		V_{sw}	–	3.5	4.1	V
Loading current		$-I_L$	0.1	0.5	2.0	mA

AC CHARACTERISTICS

V_{DD1} = + 12 V; V_{DD2} = + 5 V; V_{DD3} = −12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 2

parameter	conditions	symbol	min.	typ.	max.	unit
Amplifier A to Amplifier E						
Open loop gain		G_{ol}	–	90	–	dB
Overall distortion without de-emphasis		THD	–	−110	−100	dB
Slew rate (Amplifier A)		$\Delta V/\Delta t$	–	30	–	V/μs
Supply voltage ripple rejection						
V_{DD1}	note 1	SVRR	50	60	–	dB
V_{DD2}	note 2	SVRR	50	60	–	dB
V_{DD3}	note 2	SVRR	55	70	–	dB
Line amplifier D						
Output voltage (pins 10 and 19) (r.m.s. value)		$V_{O(rms)}$	1.9	2.0	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion		THD	–	−110	−100	dB
Channel separation		α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and mute OFF output voltage (pins 10 and 19)		V_O	–	–	4	mV
Headphone amplifier (E)						
Output voltage (pins 13 and 16) (r.m.s. value)	R_L = 600 Ω	$V_{O(rms)}$	–	6	–	V
	R_L = 132 Ω	$V_{O(rms)}$	–	5.5	–	V
Signal to noise ratio	B = 20 Hz to 20 kHz	S/N	110	115	–	dB
Total harmonic distortion	R_L = 600 Ω	THD	–	−110	−100	dB
Total harmonic distortion	R_L = 132 Ω	THD	–	−88	−80	dB
Channel separation	20 Hz to 20 kHz; R_L = 600 Ω	α	95	100	–	dB
Output impedance		Z_O	–	–	0.5	Ω
Difference between mute ON and OFF output voltage (pins 13 and 16)		V_O	–	–	6	mV

AC CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Mute status (pin 3)	open collector output					
Output voltage LOW (mute ON)	$-I_{OL}$ = 3 mA	–	–	–	0.4	V
Output voltage HIGH (mute OFF)	$I_{OL} \leqslant 1\ \mu A$		2.4	–	V_{DD1}	V
Mute timing	note 3					
De-emphasis switch						
Input voltage HIGH	De-emphasis ON	V_{IH}	2.4	–	V_{DD1}	V
Input voltage LOW	De-emphasis OFF	V_{IL}	0	–	1	V
Input current HIGH	De-emphasis ON	I_{IH}	–	–	5.0	μA
Input current LOW	De-emphasis OFF	$-I_{IL}$	–	–	25	μA

Notes to the characteristics

1. The ripple rejection is measured at the output of the line amplifier; amplitude = 0.5 V_{tt}; f = 100 Hz to 10 kHz.
2. The ripple rejection is measured at the output of the line amplifier; amplitude = 1 V_{tt}; f = 100 Hz to 10 kHz.
3. The mute timing is provided by an external capacitor connected to pin 2.

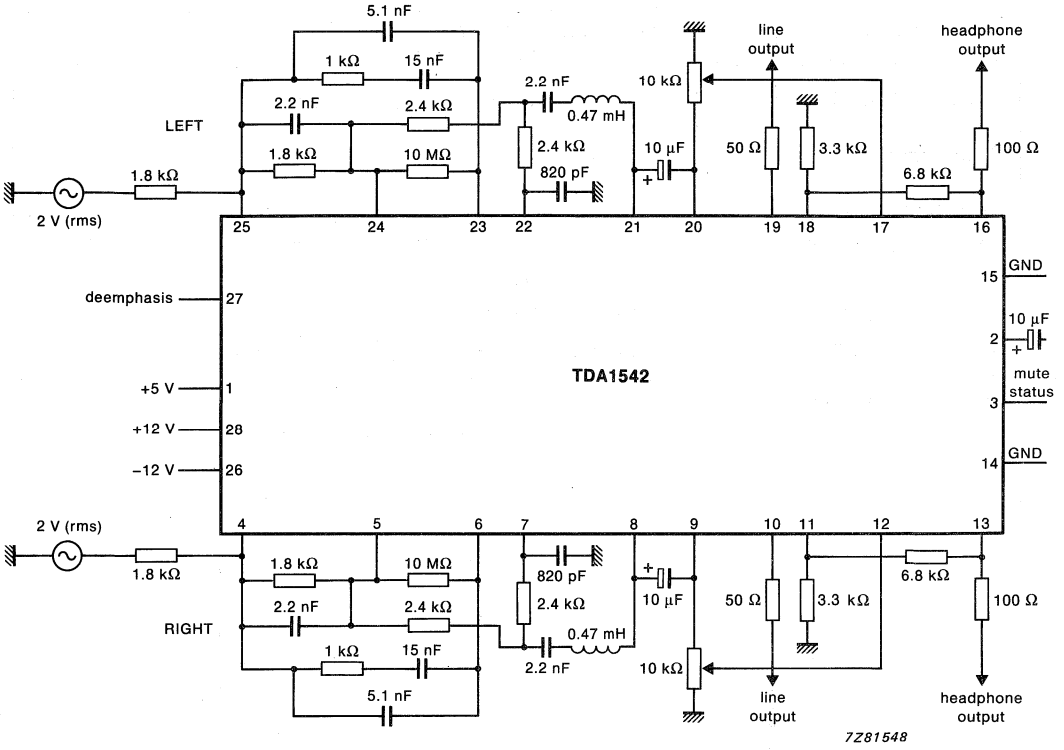


Fig. 2 Test and application circuit.

Philips Semiconductors

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543

Dual 16-bit DAC (economy version) (I^2S input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

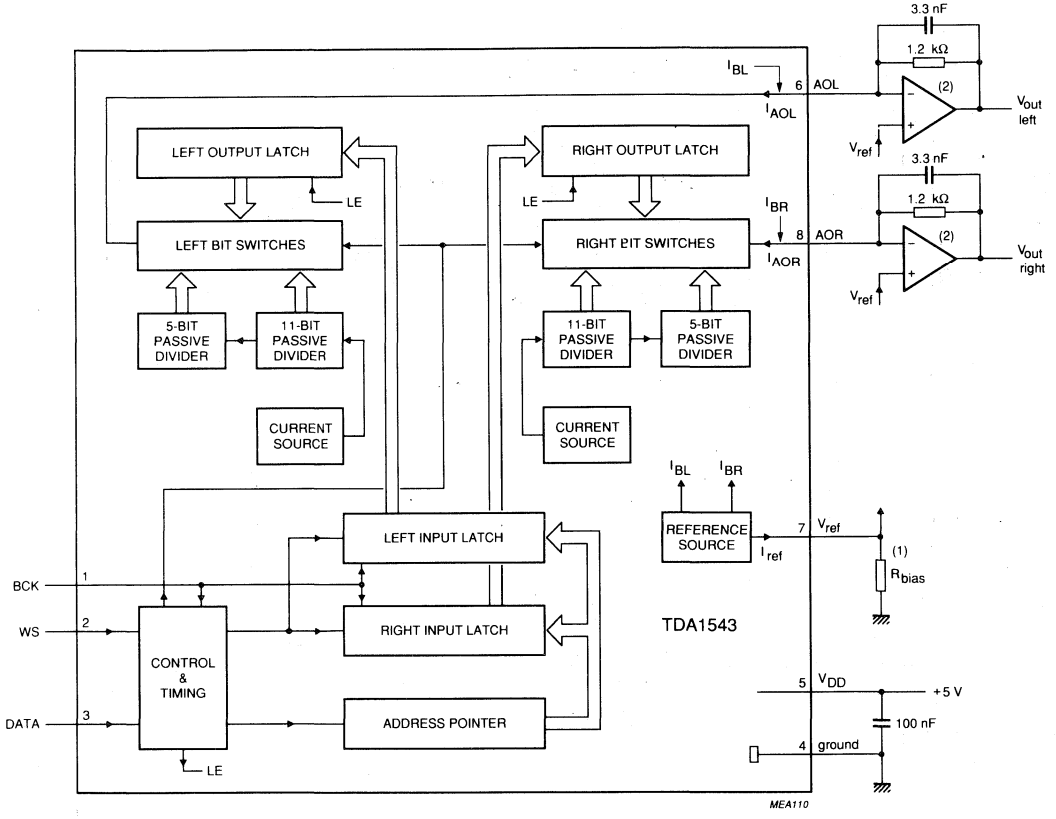
The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543	8	DIL	plastic	SOT97
TDA1543T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

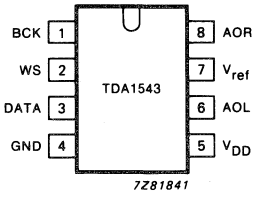


Fig.2(a) Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

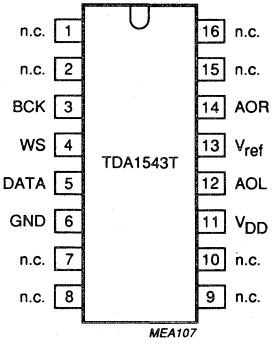
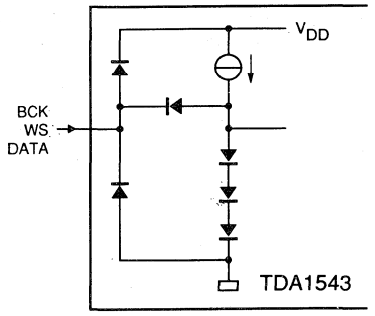
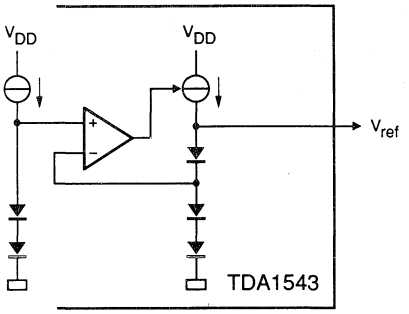


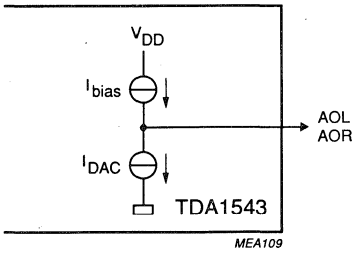
Fig.2(b) Pin configuration TDA1543T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

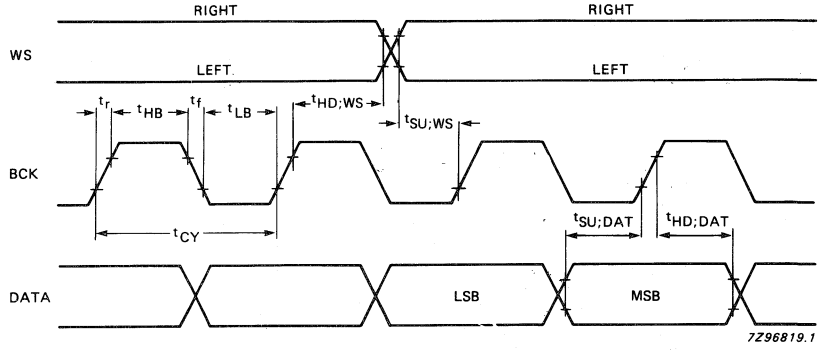


Fig.4 Format of input signals (I²S format).

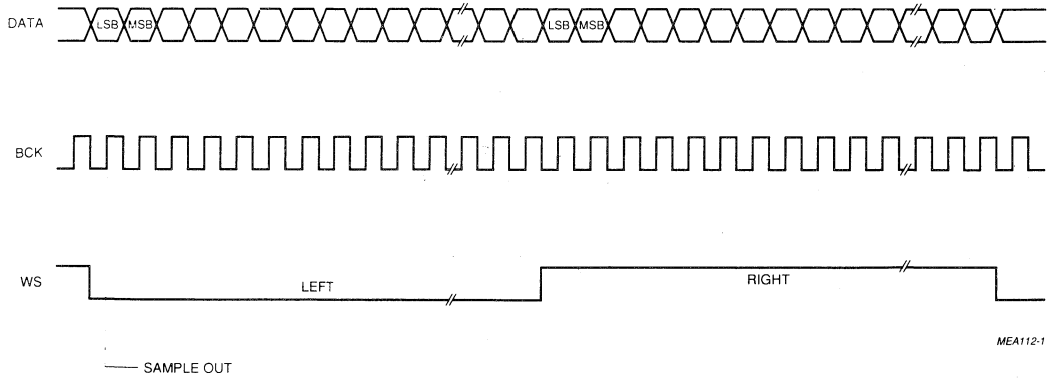
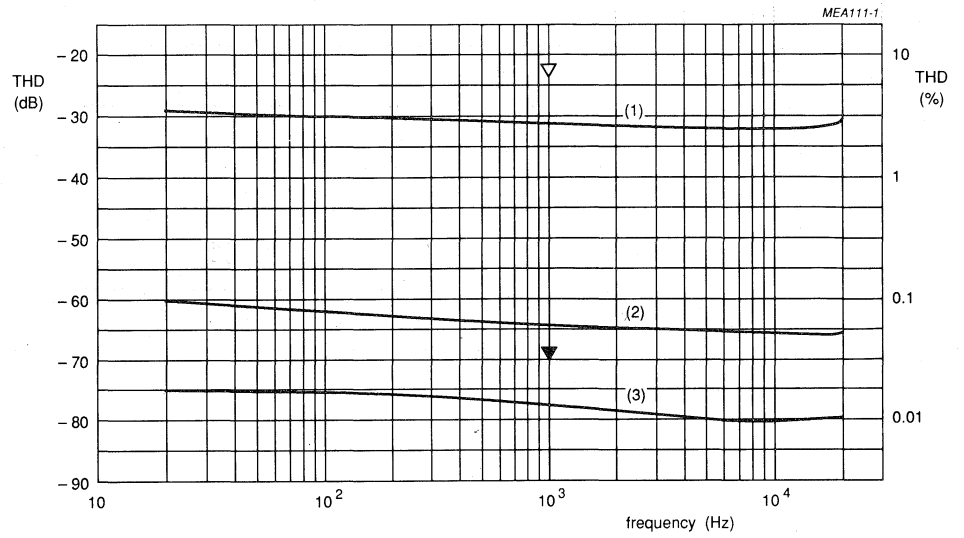


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543A

Dual 16-bit DAC (economy version) (Japanese input format)

FEATURES

- Low distortion
- 16-bit dynamic range
- 4 x oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- Japanese input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1543A is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders and in digital amplifiers.

ORDERING INFORMATION

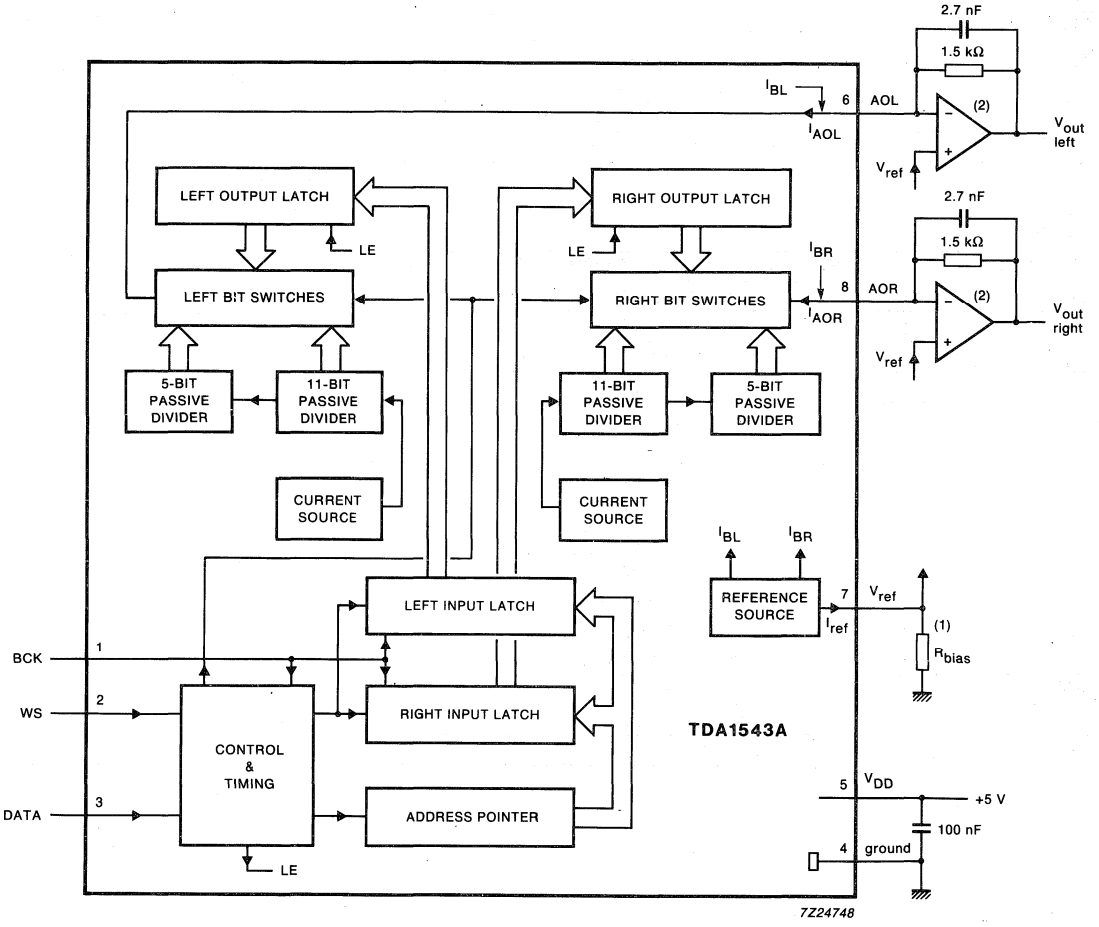
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543A	8	DIL	plastic	SOT97
TDA1543AT	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−30	−23	dB
		at −60 dB	-	3.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A



(1) Optional
(2) 2 x 1/2 NE5532

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (Japanese input format)

TDA1543A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

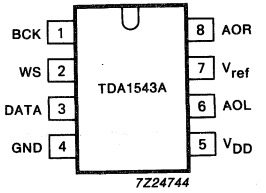


Fig.2(a) Pin configuration TDA1543A.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

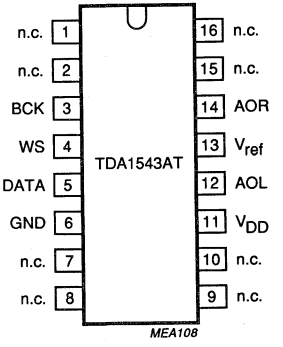
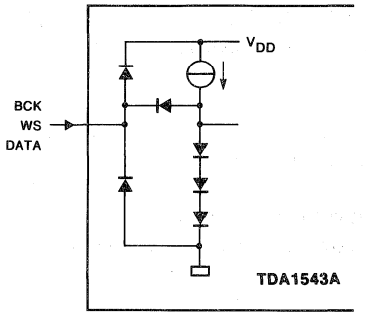
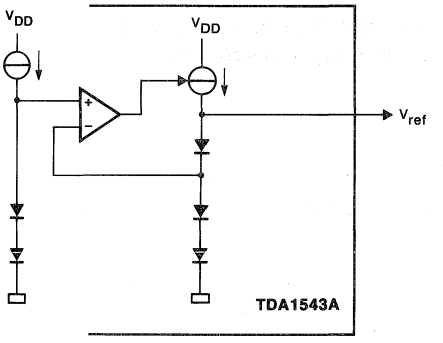


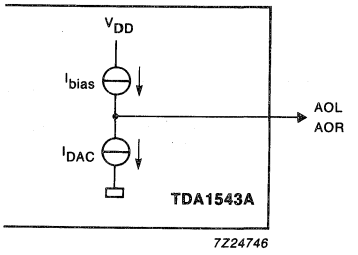
Fig.2(b) Pin configuration TDA1543AT.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543A accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

This flexible input data format (Japanese) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	µA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		−0.3	-	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		−75	−70	dB
		note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise at −60 dB;	-	−30	−23	dB
		note 3, Fig.6	-	3.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	µs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

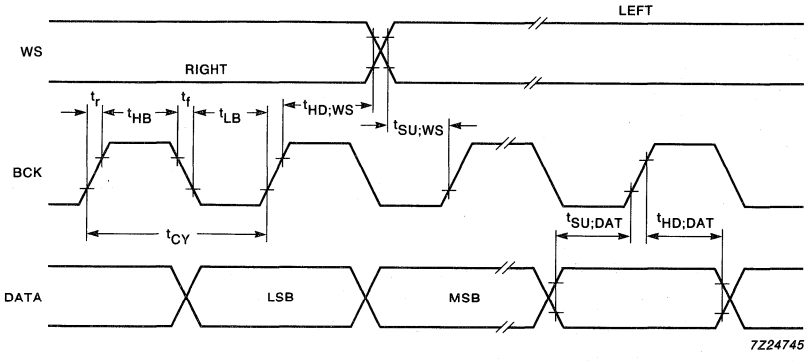


Fig.4 Format of input signals (Japanese format).

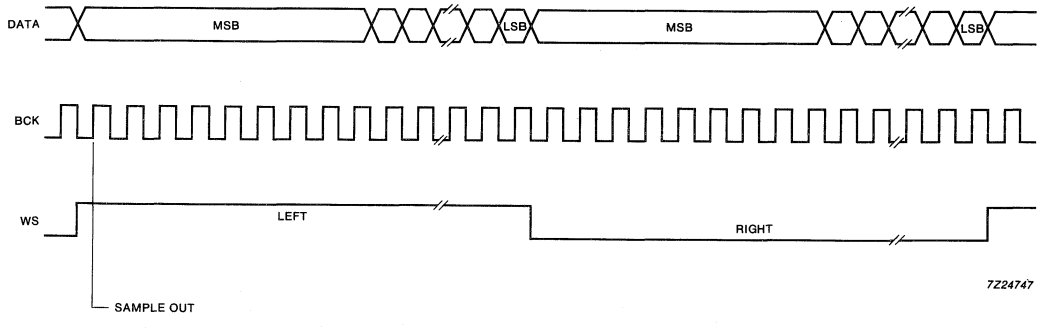
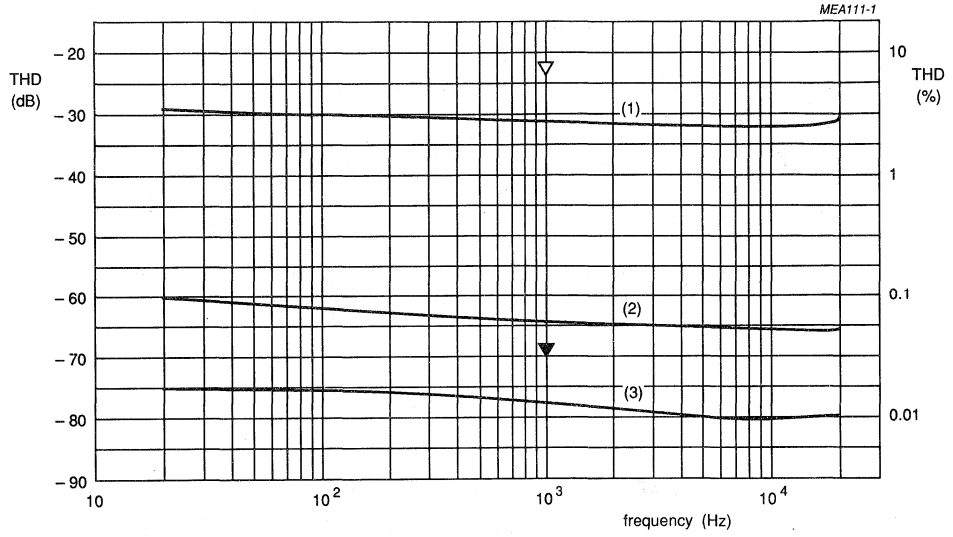


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

Data sheet	
status	Product specification
date of issue	February 1991

TDA1543(A)/S6

Dual 16-bit low-cost economy DAC (relaxed version of TDA1543A)

GENERAL DESCRIPTION

The TDA1543(A)/S6 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as a low-cost economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassete recorders, digital sound in television systems and digital amplifiers.

The S6 version is a relaxed version of the TDA1543(A). The differences in performance between the S6 selection and the standard version are limited to only three parameters:

QUICK REFERENCE VALUES STANDARD VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	−70	dB
T_{amb}	operating ambient temperature range		−30	+85	°C
AI_{bias}	bias current gain		1.9	2.1	

QUICK REFERENCE VALUES S6 VERSION

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
THD	total harmonic distortion	including noise at 0 dB	-	−60	dB
T_{amb}	operating ambient temperature range		−20	+75	°C
AI_{bias}	bias current gain		1.85	2.1	

The other characteristics of the S6 version can be found in the data sheets of the TDA1543 and the TDA1543A.

Data sheet	
status	Objective specification
date of issue	February 1991

TDA1544
Dual 16-bit low-noise DAC

FEATURES

- 16-bit resolution and 4 x oversampling
- High performance: low distortion, wide dynamic range and high signal-to-noise ratio
- Single 5 V power supply
- No external components required
- Adjustable bias current
- Japanese-input format: time multiplexed, two's complement, TTL

GENERAL DESCRIPTION

The TDA1544 is a dual 16-bit digital-to-analog converter (DAC) and is designed for use in hi-fi digital audio equipment.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1544	8	DIL	plastic	SOT97
TDA1544T	16	mini-pack	plastic	SO16L;SOT162A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		-	50	60	mA
I_{FS}	full scale output current		2.7	3.0	3.3	mA
THD	total harmonic distortion	including noise	-	−75	−70	dB
		at 0 dB	-	0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB	-	2.2	7.9	%
t_{cs}	current settling time to ±1 LSB		-	0.5	-	µs
BR	input bit rate at data input		-	-	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	9.2	MHz
S/N	signal-to-noise ratio		99	101	-	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	-	$\pm 500 \times 10^{-6}$	-	K^{-1}
T_{amb}	operating ambient temperature range		−30	-	+85	°C
P_{tot}	total power dissipation		-	250	-	mW
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA

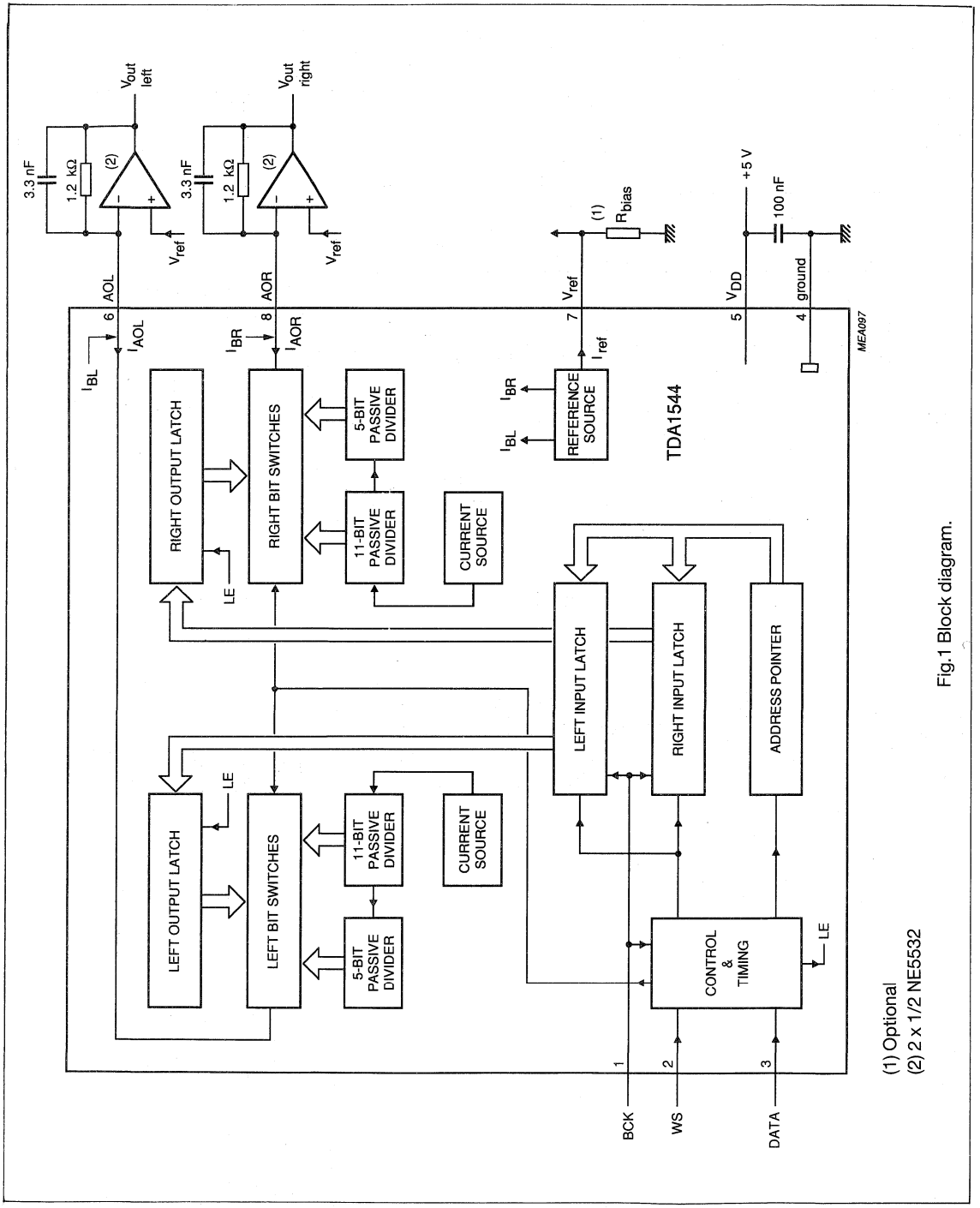


Fig.1 Block diagram.

(1) Optional
(2) 2 x 1/2 NE5532

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel output
V_{ref}	7	reference voltage output
AOR	8	right channel output

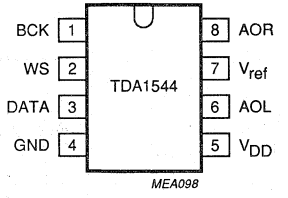


Fig.2(a) Pin configuration TDA1544.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

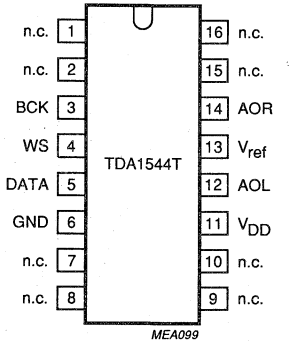
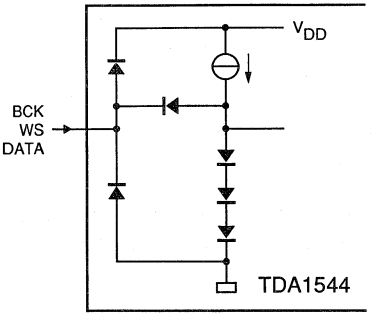
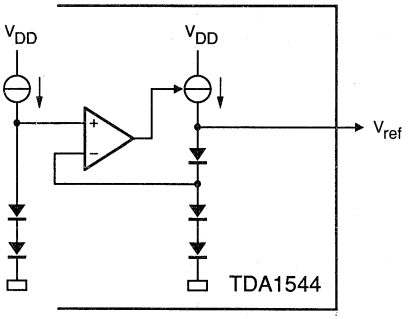


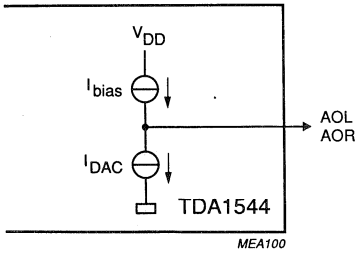
Fig.2(b) Pin configuration TDA1544T.



(a) input pins BCK, WS and DATA.



(b) output pin V_{ref}.



(c) output pins AOL and AOR.

Fig.3 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1544 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5.

The high maximum input bit-rate and fast settling current facilitates application in 4 x oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		-	+150	°C
T_{stg}	storage temperature range		−55	+150	°C
T_{amb}	operating ambient temperature range		−30	+85	°C
V_{es}	electrostatic handling*		−2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	-	50	60	mA
RR	ripple rejection	note 2	-	50	-	dB
Digital inputs						
I_{IL}	input current pins (1, 2 and 3) digital inputs LOW	V_I = 0.8 V	-	-	−0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	-	-	20	μA
f_{BCK}	input frequency/bit rate clock input pin 1		-	-	9.2	MHz
BR	bit rate data input pin 3		-	-	9.2	Mbits/s
f_{WS}	word select input pin 2		-	-	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		-	-	16	bits
$V_{OC(AC)}$	output voltage compliance AC		-	±25	-	mV
$V_{OC(DC)}$	DC		1.8	-	V_{DD}−1.2	V
I_{FS}	full scale current		2.7	3.0	3.3	mA
T_{CFS}	full scale temperature coefficient		-	±500 x 10^{-6}	-	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA $V_{AO} = V_{ref}$	−0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		−0.6	-	5.0	mA
AI_{bias}	bias current gain		0.95	1.00	1.05	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.05	2.20	2.35	V
I_{ref}	reference current output		−0.6	-	5.0	mA
THD	total harmonic distortion	including noise		−75	−70	dB
		at 0 dB; note 3, Fig.6		0.018	0.032	%
THD	total harmonic distortion	including noise	-	−33	−23	dB
		at −60 dB; note 3, Fig.6	-	2.2	7.9	%
t_{cs}	settling time ±1 LSB		-	0.5	-	μs
α	channel separation		85	90	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	-	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	< 0.2	-	μs
S/N	signal-to-noise ratio at bipolar zero	note 5	99	101	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.4)						
t_r	rise time		-	-	32	ns
t_f	fall time		-	-	32	ns
t_{CY}	bit clock cycle time		108	-	-	ns
t_{HB}	bit clock HIGH time		22	-	-	ns
t_{LB}	bit clock LOW time		22	-	-	ns
$t_{SU;DAT}$	data set-up time		32	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	-	-	ns
$t_{HD;WS}$	word select hold time	note 6	2	-	-	ns
$t_{SU;WS}$	word select set-up time		32	-	-	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point t_{HD} = 0 ns, this value has been fixed on 2 ns due to tolerances.

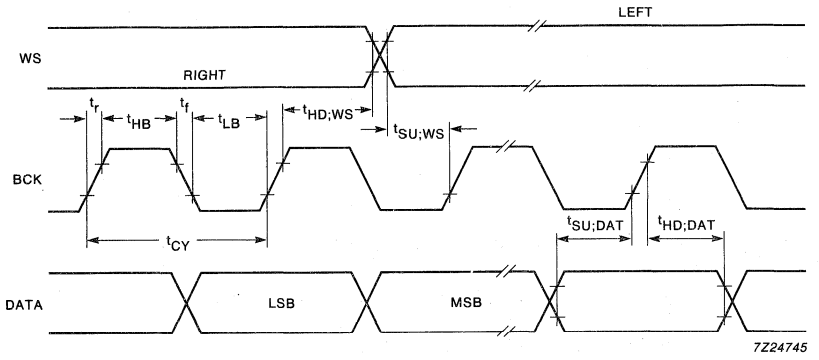


Fig.4 Format of input signals (Japanese format).

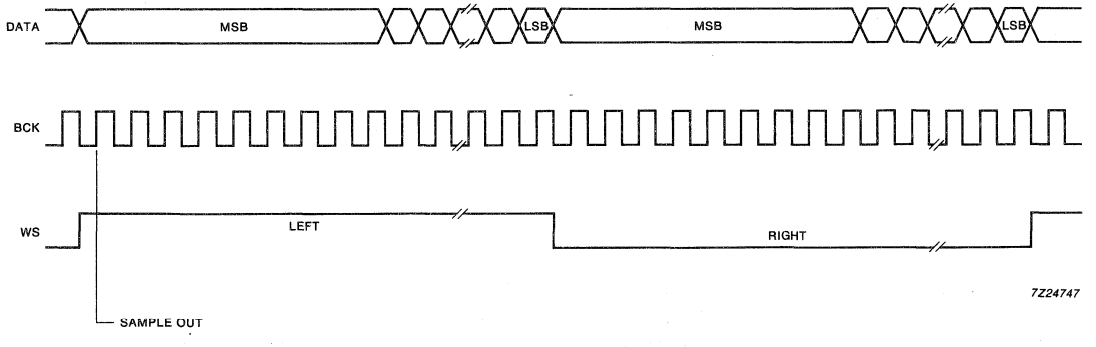
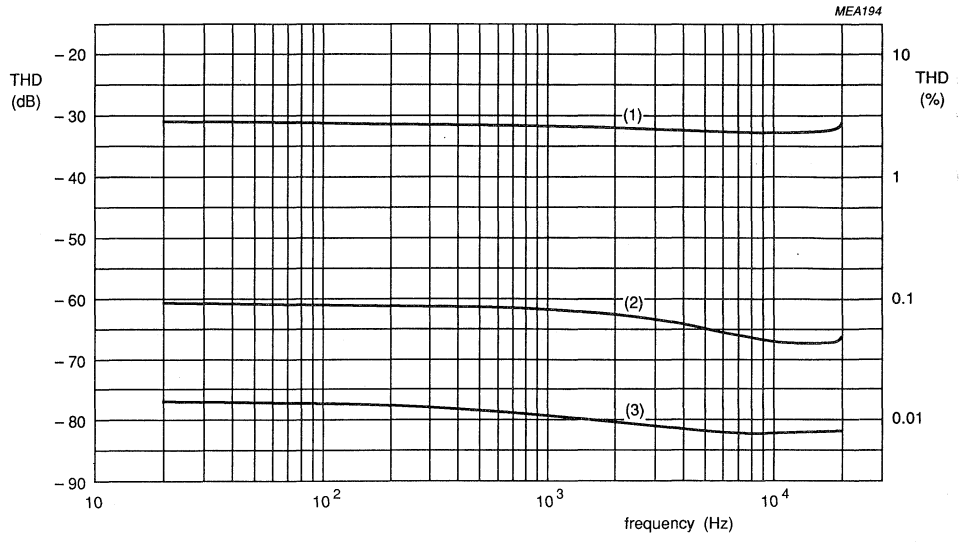


Fig.5 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –60 dB

(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –24 dB

(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of –0 dB

Fig.6 Distortion as a function of frequency (4FS)

Notes to Fig.6

- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.

GENERAL DESCRIPTION

The TDA1545 is the first device of a new generation of the digital-to-analog convertors which embodies the innovative technique of continuous calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature, matching and process variations. The TDA1545 is fabricated in a 1.0 µm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the high coarse current combined with the implemented symmetrical offset decoding method preclude zero-crossing distortion and ensures high quality audio reproduction. Therefore, the continuous calibration digital-to-analog convertor is eminently suitable for use in (portable) digital audio equipment.

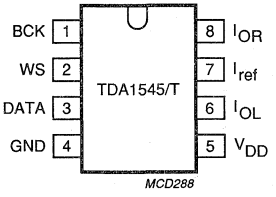


Fig.1 Pinning diagram.

FEATURES

- Space saving package (SO8 or DIL8)
- Low power consumption
- Low total harmonic distortion
- Wide dynamic range (16-bit resolution)
- Continuous calibration concept
- Easy application: single 3 to 5.5 V rail power supply and output- and bias current are proportional to the supply voltage
- Fast settling time permits 2 x, 4 x and 8 x oversampling (serial input) or double speed operation at 4 x oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range of −40 °C to 85 °C
- Internal timing and control circuits
- Compatible with most of the Japanese input formats: time multiplexed, two's complement, TTL
- No zero crossing distortion

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1545	8	DIL	plastic	SOT97
TDA1545T	8	mini-pack	plastic	SO8; SOT96A

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	positive supply voltage
I_{OL}	6	left channel output
V_{ref}	7	reference voltage output
I_{OR}	8	right channel output

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction-to-ambient		
	DIL8	100	K/W
	SO8	210	K/W

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5	5.5	V
I_{DD}	supply current	V_{DD} = 5 V, at code 0000H	-	3.0	4.0	mA
I_{FS}	full scale output current	V_{DD} = 5 V	0.9	1.0	1.1	mA
I_{FS}	full scale output current	V_{DD} = 3 V	-	0.6	-	mA
THD	total harmonic distortion	including noise at 0 dB	- -	–85 0.005	–78 0.01	dB %
THD	total harmonic distortion	including noise at –60 dB	- -	–30 3	–24 6	dB %
THD	total harmonic distortion	including noise at –60 dB, A-weigthing	- -	–33 2	- -	dB %
		R3 = R4 = 11 kΩ see Fig.2; I_{FS} = 2 mA	-	1	-	%
S/N	signal-to-noise ratio at bipolar zero	A-weighting, at code 0000H	86	92	-	dB
S/N	signal-to-noise ratio at bipolar zero	R3 = R4 = 11 kΩ see Fig.1; I_{FS} = 2 mA	-	95	-	dB
t_{cs}	current settling time to ±1 LSB		-	0.2	-	µs
BR	input bit rate at data input		-	-	18.4	Mbits/s
f_{BCK}	clock frequency at clock input		-	-	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL}; I_{OR})		-	±400	-	10^{-6}
P_{tot}	total power dissipation	V_{DD} = 5 V, at code 0000H	-	15	20	mW
P_{tot}	total power dissipation	V_{DD} = 3 V, at code 0000H	-	6.0	-	mW
T_{amb}	operating ambient temperature range		–40	-	+85	°C

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage		-	-	6	V
T_{stg}	storage temperature range		–55	-	+150	°C
T_{XTAL}	maximum crystal temperature		-	-	+150	°C
T_{amb}	operating ambient temperature range		–40	-	+85	°C
V_{es}	electrostatic handling	see note 1	–2000	-	+2000	V

Note to the limiting values

1 Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

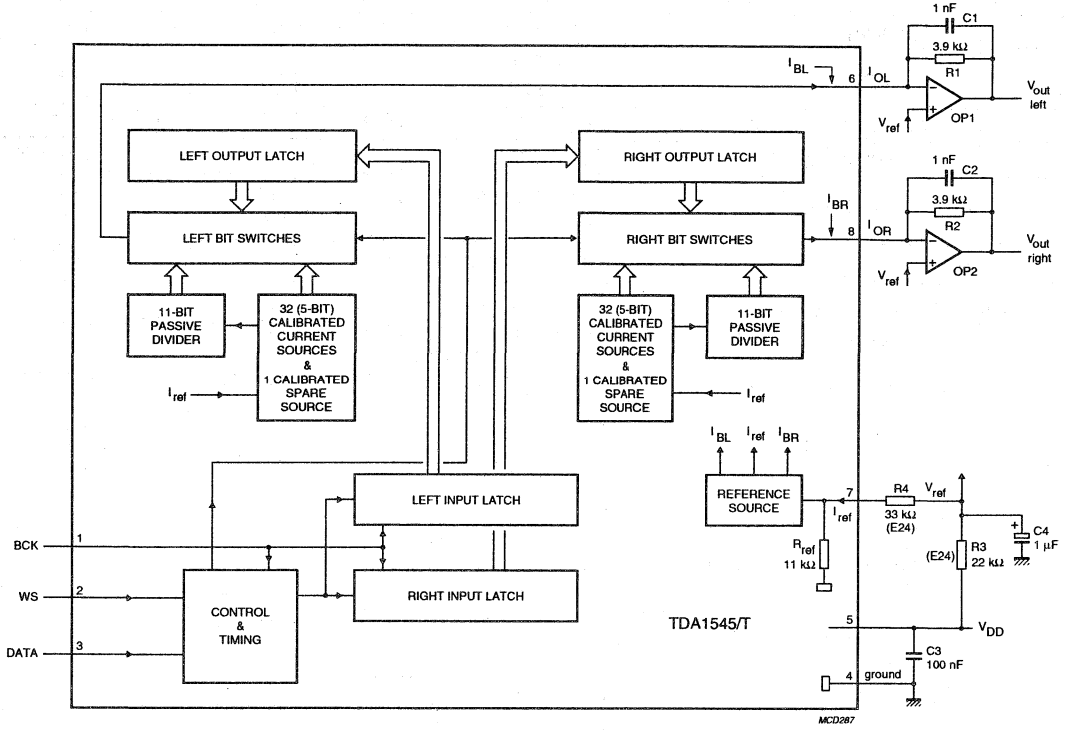


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig. 3. The figure shows the calibration principle (Fig.3a) and operation principle (Fig.3b). During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore the drain current of M1 will still be equal to I_{ref} and this exact duplicate of I_{ref} is now available at the I_{out} terminal. The 32 current sources and the spare current source of the TDA1545 are continuously calibrated (see Fig.2). The spare current is included to allow for continuous convertor operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by the LSB currents. The TDA1545 accepts input serial data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.4 and Fig.5. With a LOW level on the word select input (WS) input data is placed in the right input register and with a HIGH level on the WS input data is placed in the left input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches. An internal bias current I_{bias} (see I_{BL} and I_{BR} in Fig.2) is added to the full scale output current I_{FS} in order to achieve the maximum dynamic range at the outputs of OP1 and OP2 (see Fig.2). The reference input current I_{ref} controls with gain A_{FS} the current I_{FS} which is a sink current and with gain A_{bias} the I_{bias} which is a source current (note 1). The current I_{ref} is proportional to V_{DD} so the I_{FS} and I_{bias} will be proportional to V_{DD} as well (note 2) because A_{FS} and A_{bias} are constant. The reference output voltage V_{ref} in Fig.2 is 2/3 V_{DD}. In this way the maximum dynamic range is achieved over the entire power supply range. The tolerance of the reference input current in Fig.2 depends on the tolerance of the resistors R3, R4 and R_{ref} (note 3).

Note 1: $I_{FS} = A_{FS} \cdot I_{ref}$ and $I_{bias} = A_{bias} \cdot I_{ref}$

Note 2: $$\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$$

Note 3: $$dI_{ref} = I_{ref} - \frac{V_{DD}}{R3+dR3+R4+dR4+R_{ref}+dR_{ref}}$$

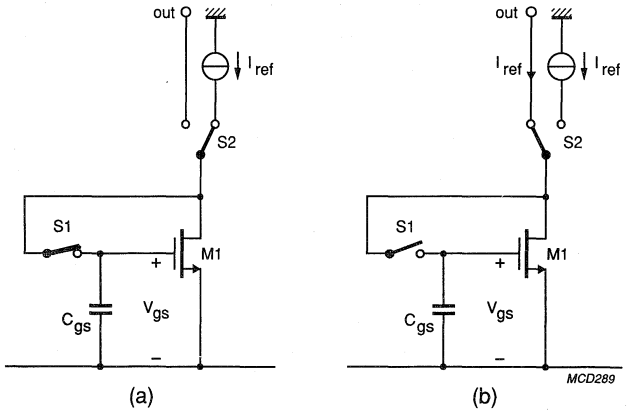


Fig.3 Calibration principle: (a) calibration, (b) operation.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = +25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage range		3.0	5.0	5.5	V
I_{DD}	supply current	note 1	-	3.0	4.0	mA
RR	ripple rejection	note 2	-	30	-	dB
Digital inputs (WS; BCK; DATA)						
$\lvert I_{IL} \rvert$	input leakage current LOW	V_I = 0.8 V	-	-	10	µA
$\lvert I_{IH} \rvert$	input leakage current HIGH	V_I = 2.4 V	-	-	10	µA
f_{BCK}	clock input pin 1		-	-	18.4	MHz
BR	bit rate data input pin 3		-	-	18.4	Mbits/s
f_{WS}	word select input pin 2		-	-	384	kHz
Timing (Fig.4)						
t_r	rise time		-	-	12	ns
t_f	fall time		-	-	12	ns
t_{CY}	bit clock cycle time		54	-	-	ns
t_{HB}	bit clock HIGH time		15	-	-	ns
t_{LB}	bit clock LOW time		15	-	-	ns
$t_{SU;DAT}$	data set-up time		12	-	-	ns
$t_{HD;DAT}$	data hold time to bit clock		2	-	-	ns
$t_{HD;WS}$	word select hold time		2	-	-	ns
$t_{SU;WS}$	word select set-up time		12	-	-	ns
Analog input (I_{ref})						
R_{ref}	reference resistor (see Fig.2)		7.4	11.0	14.6	kΩ
Analog outputs (I_{OL}; I_{OR})						
Res	resolution		-	-	16	bits
V_{DCC}	DC output voltage compliance		2.0	-	V_{DD}–1	V
I_{FS}	full scale current		0.9	1.0	1.1	mA
T_{CFS}	full scale temperature coefficient		-	±400	-	10^{-6}
I_{bias}	bias current (adjustable)		643	714	785	µA
A_{FS}	reference input current to full scale output current gain		12.8	13.2	13.6	
A_{bias}	reference input current to bias current gain		9.14	9.42	9.7	
THD	total harmonic distortion	including noise at 0 dB; note 3, Fig.6	- -	–85 0.005	–78 0.01	dB %
THD	total harmonic distortion	including noise at –60 dB; note 3, Fig.6	- -	–30 3	–24 6	dB %

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	including noise at −60 dB, A-weigthing	-	−33	-	dB
			-	2	-	%
		R3 = R4 = 11 kΩ see Fig.2; I_{FS} = 2 mA	-	1	-	%
THD	total harmonic distortion	including noise at 0 dB; note 4	-	−81	−70	dB
			-	0.009	0.03	%
t_{cs}	settling time ±1 LSB		-	0.2	-	µs
α	channel separation		86	95	-	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 3	-	0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		-	±0.2	-	µs
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 1	86	92	-	dB
S/N	signal-to-noise ratio (A-weighting)	at bipolar zero; note 5	-	95	-	dB

Notes to the characteristics

1 At code 0000H

2 V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

3 Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.

4 Measured with 1 kHz sinewave over a 20 Hz to 20 kHz bandwidth generated at a sampling rate of 192 kHz.

5 R3 = R4 = 11 kΩ; see Fig.2; I_{FS} = 2 mA

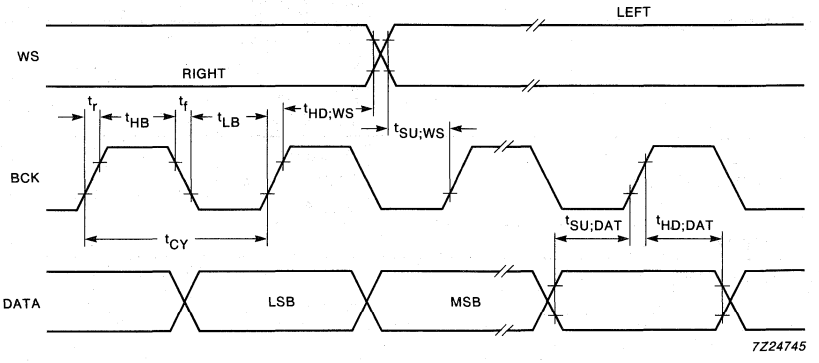


Fig.4 Format of input signals (Japanese format).

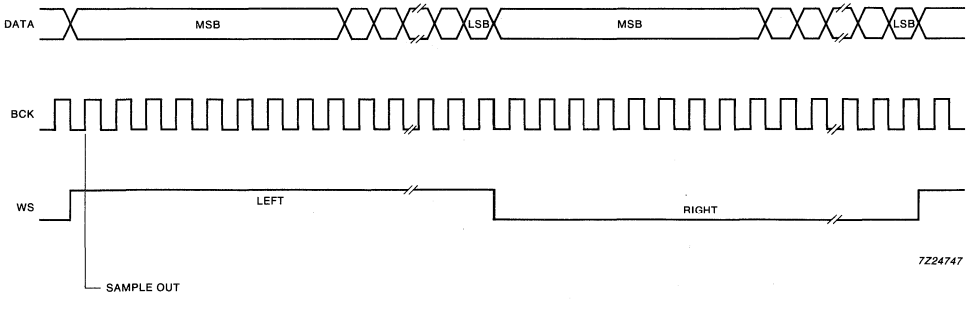
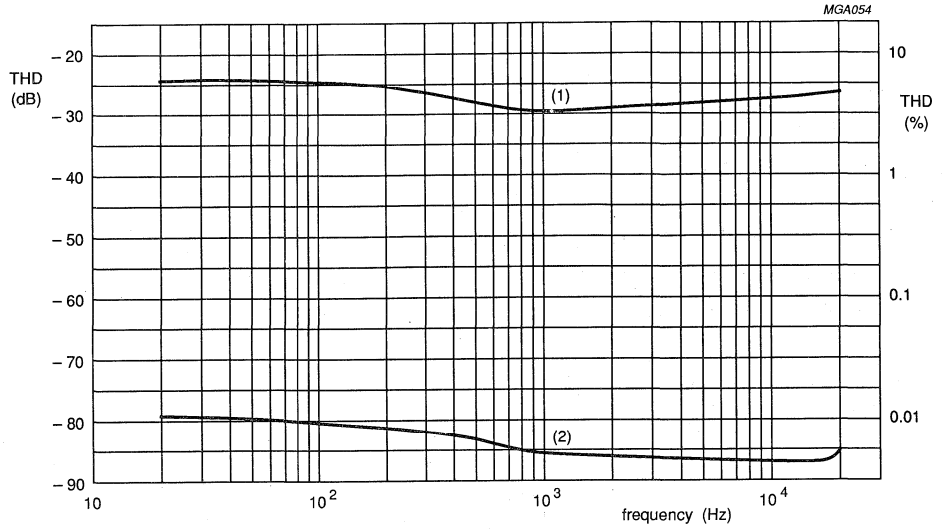


Fig.5 Format of input signals.



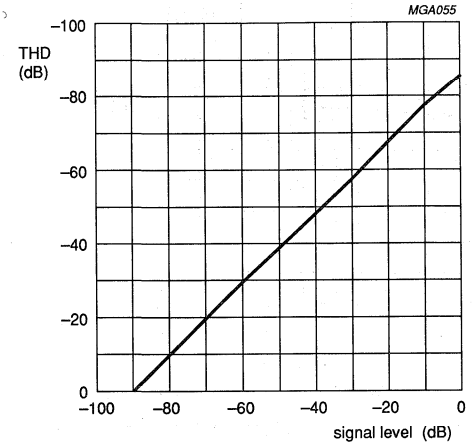
(1) Measured including all distortion plus noise at a level of –60 dB

(2) Measured including all distortion plus noise at a level of –0 dB

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

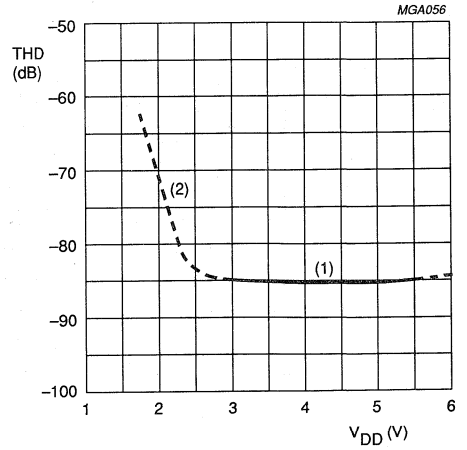
Fig.6 Distortion as a function of frequency (4FS).



The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.7 Distortion as a function of signal level (4FS).



(1) Measured within the specified operating supply voltage range

(2) Measured outside the specified operating supply voltage range

The sample frequency 4FS: 176.4 kHz

The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied

Fig.8 Distortion as a function of supply voltage V_{DD} (4FS).

Dual top-performance bitstream DAC

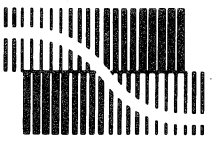
TDA1547

FEATURES

- Top-grade audio performance
  - very low harmonic distortion
  - high signal-to-noise ratio
  - wide dynamic range of approximately 108 dB (not A-weighted)
- High crosstalk immunity
- Bitstream concept
  - high over-sampling rate up to 192 f_s
  - pulse-density modulation
  - inherently monotonic
  - no zero-crossing distortion

GENERAL DESCRIPTION

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems. The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's, thereby reducing the crosstalk between the digital and analog parts. The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity. The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.



ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1547	32	SDIL	plastic	SOT232A

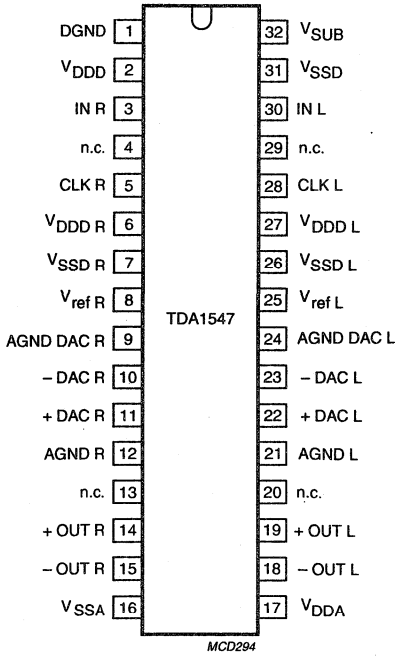


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DGND	1	0 V digital supply
V_{DDD}	2	5 V digital supply for both channels
IN R	3	serial one-bit data input for the right channel
n.c.	4	pin not connected; should preferably be connected to digital ground
CLK R	5	clock input for the right channel
$V_{DDD\ R}$	6	5 V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel
$V_{SSD\ R}$	7	−3.5 V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel
$V_{ref\ R}$	8	−4 V reference voltage for the right channel switched capacitor DAC
AGND DAC R	9	0 V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground
−DAC R	10	output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier
+DAC R	11	output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier
AGND R	12	0 V reference voltage for both right channel operational amplifiers
n.c.	13	pin not connected; should preferably be connected to analog ground
+OUT R	14	+ output of the switched capacitor operational amplifier
−OUT R	15	− output of the switched capacitor operational amplifier
V_{SSA}	16	−5 V analog supply
V_{DDA}	17	5 V analog supply
−OUT L	18	− output of the switched capacitor operational amplifier
+OUT L	19	+ output of the switched capacitor operational amplifier
n.c.	20	pin not connected; should preferably be connected to analog ground
AGND L	21	0 V reference voltage for both left channel operational amplifiers
+DAC L	22	output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier
−DAC L	23	output from the left negative switched capacitor DAC; feedback connection for the left negative operational amplifier
AGND DAC L	24	0 V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground
$V_{ref\ L}$	25	−4 V reference voltage for the left channel switched capacitor DAC
$V_{SSD\ L}$	26	−3.5 V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel
$V_{DDD\ L}$	27	5 V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel

SYMBOL	PIN	DESCRIPTION
CLK L	28	clock input for the left channel
n.c.	29	pin not connected; should preferably be connected to digital ground
IN L	30	serial one-bit data input for the left channel
V_{SSD}	31	–5 V digital supply for both channels
V_{SUB}	32	–5 V substrate voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply voltages						
$V_{DDD\ L,\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage for one channel; pins 26 and 7		–4.0	–3.5	–3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		–5.5	–5.0	–4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6	V
V_{SSA}	negative analog supply voltage ; pin 16		–6.0	–5.0	–4.5	V
Supply current						
$I_{DDD\ L,\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2		-	29.0	-	mA
$I_{SSD\ L,\ R}$	negative digital supply current for one channel; pins 26 and 7		-	–0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		-	–28.0	-	mA
I_{DDA}	positive analog supply current; pin 17		-	51.0	-	mA
I_{SSA}	negative analog supply current; pin 16		-	–51.0	-	mA
P_{tot}	total power dissipation		-	800	-	mW
$V_{OUT(RMS)}$	output voltage (RMS value)	f_{CLK} = 8.46 MHz; notes 1 and 2	0.85	1.0	1.15	V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Supply current						
(THD + N)/S	THD + Noise; 0 dB	1 kHz; notes 2 and 3	-	−101	−96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	f = 20 Hz to 20 kHz; notes 2 and 4	-	−101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; −20 dB	f = 1 kHz; notes 2 and 3	-	−88	−84	dB
(THD + N)/S	THD + Noise; −60 dB	f = 1 kHz; notes 2 and 3	-	−48	−44	dB
S/N	signal-to-noise ratio	pattern 0101..; notes 2 and 5	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101..; notes 2 and 5	-	113	-	dB
f_{CLK}	maximum clock frequency		-	-	10	MHz
α	channel separation	f = 1 kHz	101	115	-	dB
T_{amb}	operating ambient temperature		−20	-	70	°C

Notes to the quick reference data

1. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$)
2. Device measured in differential mode with external components as shown in Fig.5.
3. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

FUNCTIONAL DESCRIPTION

Both channels are completely separated to reach the desired high crosstalk suppression level.
Each channel consists of the following functional parts:

- One-bit input, which latches the incoming data to the system clock.
- Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
- Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
- Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	60	K/W

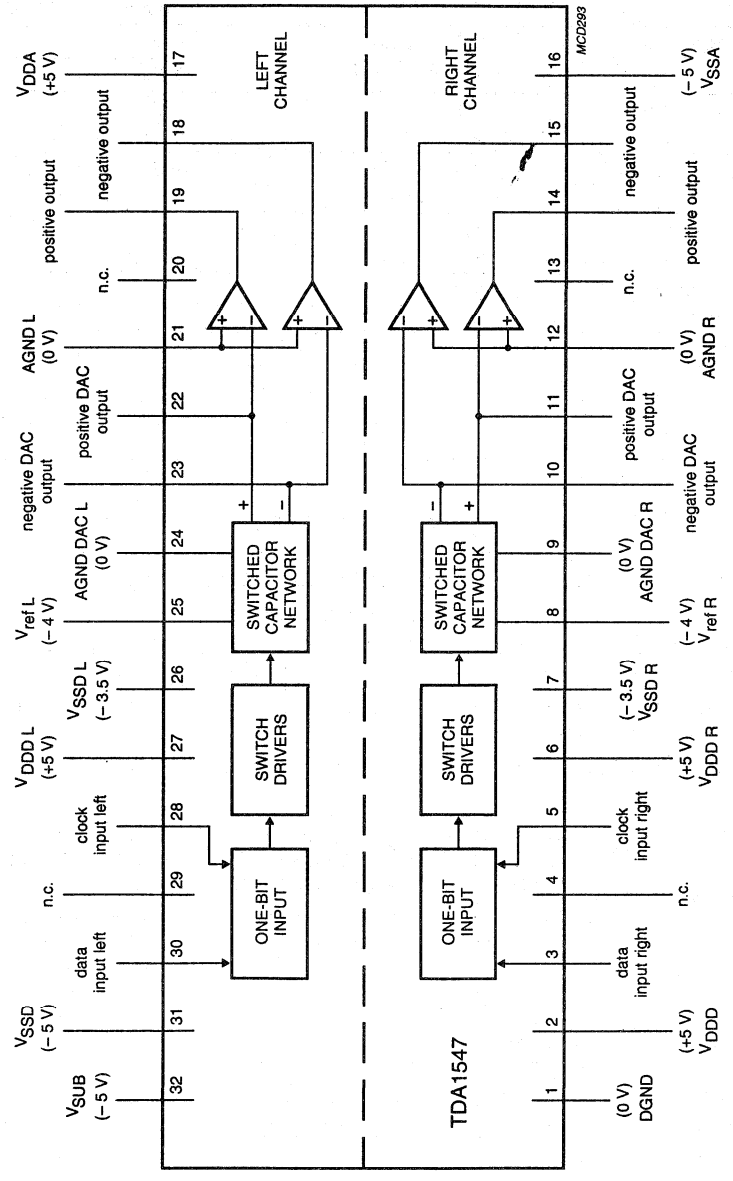


Fig.2 Block diagram.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX.	UNIT
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	V
$V_{DDD\ L,\ R}$	positive digital supply voltage; pins 27 and 6		-	5.5	V
V_{DDD}	positive digital supply voltage; pin 2		-	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage; pins 26 and 7		−4.0	-	V
V_{SSD}	negative digital supply voltage; pin 31		−5.5	-	V
V_{DDA}	positive analog supply voltage; pin 17		-	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	-	V
$V_{DDD\ L,\ R}$ - $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	9.0	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	-	1300	mW
$V_{ref\ L,\ R}$	input reference voltage; pins 25 and 8		−6.0		V
$V_{CLK\ L,\ R}$	input voltage clock; pins 28 and 5		−0.5	V_{DDD}+0.5	V
$V_{I\ L}$	input voltage channel; pin 30		−0.5	V_{DDD}+0.5	V
$V_{I\ R}$	input voltage channel; pin 3		−0.5	V_{DDD}+0.5	V
T_{amb}	operating ambient temperature		−20	70	°C
T_{stg}	storage temperature		−40	150	°C
T_{XTAL}	maximum crystal temperature		-	150	°C
V_{ES}	electrostatic handling	note 2	-	2000	V

Notes to the limiting values

1. The substrate voltage must be lower than or equal to the lowest supply voltage.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DDD}, $V_{DDD\ L,\ R}$, V_{DDA} = +5 V; V_{SSD}, V_{SSA} = −5 V, $V_{SSD\ L,\ R}$ = −3.5 V; $V_{ref\ L,\ R}$ = −4 V; T_{amb} = 25°C; f_{CLK} = 8.46 MHz; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{SUB}	negative substrate voltage; pin 32	note 1	−7.0	-	−4.5	V
$V_{DDD\ L,\ R}$	positive digital supply voltage for one channel; pins 27 and 6		4.5	5.0	5.5	V
V_{DDD}	digital supply voltage for both channels; pin 2		4.5	5.0	5.5	V
$V_{SSD\ L,\ R}$	negative digital supply voltage for one channel; pins 26 and 7		−4.0	−3.5	−3.0	V
V_{SSD}	negative digital supply voltage for both channels; pin 31		−5.5	−5.0	−4.5	V
V_{DDA}	positive analog supply voltage; pin 17		4.5	5.0	6.0	V
V_{SSA}	negative analog supply voltage; pin 16		−6.0	−5.0	−4.5	V
$V_{DDD\ L,\ R}$ - $V_{SSD\ L,\ R}$	supply voltage difference between pins 27, 6 and pins 26, 7		-	-	9.0	V
$V_{SSD\ L,\ R}$ - V_{SSD}	supply voltage difference between pins 26, 7 and pin 31		1.3	-	-	V
$I_{DDD\ L,\ R}$	positive digital supply current for one channel; pins 27 and 6		-	0.1	-	mA
I_{DDD}	digital supply current for both channels; pin 2			29.0	46	mA
$I_{SSD\ L,\ R}$	negative digital supply current for one channel; pins 26 and 7		-	−0.1	-	mA
I_{SSD}	negative supply current for both channels; pin 31		−45	−28.0	-	mA
$-I_{DDA}$	positive analog supply current; pin 17		-	51.0	63	mA
I_{SSA}	negative analog supply current; pin 16		−63.0	−51.0	-	mA
P_{SSR1}	power supply rejection ratio	$V_{DDD\ L,\ R}$; note 6	50	-	-	dB
P_{SSR2}	power supply rejection ratio	V_{DDD}; note 6	50	-	-	dB
P_{SSR3}	power supply rejection ratio	$V_{SSD\ L,\ R}$; note 6	60	-	-	dB
P_{SSR4}	power supply rejection ratio	V_{SSD}; note 6	50	-	-	dB
P_{SSR5}	power supply rejection ratio	V_{DDA}; note 6	60	-	-	dB
P_{SSR6}	power supply rejection ratio	V_{SSA}; note 6	60	-	-	dB
P_{tot}	total power dissipation		-	800	-	mW
Clock - Input						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		4.5	-	-	V
I_{IL}	input current LOW	V_i = 0.5 V	−10	-	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Clock - input						
I_{IH}	input current HIGH	V_i = 4.5 V	–10	-	10	µA
C_i	clock input capacitance		-	5	-	pF
f_{CLK}	clock input frequency		-	-	10	MHz
Channel left/right inputs						
V_{IL}	input voltage LOW		-	-	0.5	V
V_{IH}	input voltage HIGH		-	4.5	-	V
I_{IL}	input current LOW	V_i = 0.5 V	–10	-	10	µA
I_{IH}	input current HIGH	V_i = 4.5 V	–10	-	10	µA
C_i	channel input capacitance; pins 3, 30		-	5	-	pF
V_{ref}	reference input voltage; pins 8, 25	note 2	-	–4 ±0.4	-	V
Audio outputs						
$V_{OUT(RMS)}$	output voltage (RMS value); pins 14, 19; pins 15, 18	notes 2 and 3	0.85	1.0	1.15	V
(THD + N)/S	THD + Noise; 0 dB	f = 1 kHz; notes 3 and 4	-	–101	–96	dB
			-	0.0009	0.0016	%
(THD + N)/S	THD + Noise; 0 dB	20 Hz - 20 kHz; notes 3 and 5	-	–101	-	dB
			-	0.0009	-	%
(THD + N)/S	THD + Noise; –20 dB	f = 1 kHz; notes 3 and 4	-	–88	–84	dB
(THD + N)/S	THD + Noise; –60 dB	f = 1 kHz; notes 3 and 4	-	–48	–44	dB
S/N	signal-to-noise ratio	pattern 0101; notes 3 and 7	109	111	-	dB
S/N	signal-to-noise ratio; "A"-weighting	pattern 0101; notes 3 and 7	-	113	-	dB
α	channel separation	f = 1 kHz	101	115	-	dB
Timing						
t_r	rise time clock input	C_L = 20 pF	-	5	10	ns
t_f	fall time clock input	C_L = 20 pF	-	5	10	ns
$t_{CLK\ L}$	clock input LOW time		45	-	-	ns
$t_{CLK\ H}$	clock input HIGH time		45	-	-	ns
t_r	channel input rise time	C_L = 20 pF	-	10	15	ns
t_f	channel input fall time	C_L = 20 pF	-	10	15	ns
t_{HD}	channel input hold time		25	-	-	ns
t_{SU}	channel input set-up time		0	-	-	ns

Notes to the characteristics

1. The substrate voltage must be lower than or to equal than the lowest supply voltage.
2. Output level tracks linearly with both the clock frequency and the reference voltage ($V_{ref\ L}$ or $V_{ref\ R}$).
3. Device measured in differential mode with external components as shown in Fig.5.
4. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 1 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
5. Measured with a one-bit data signal generated by the SAA7350 from an 8 f_s (352.8 kHz), 20-bit, 20 Hz to 20 kHz digital sinewave. Measured over a 20 Hz to 20 kHz bandwidth.
6. Power supply rejection ratio measured with f_{ripple} = 1 kHz and v_{ripple} = 100 mV.
7. The specified signal-to-noise ratio includes noise introduced by the application components as shown in Fig.5.

TIMING

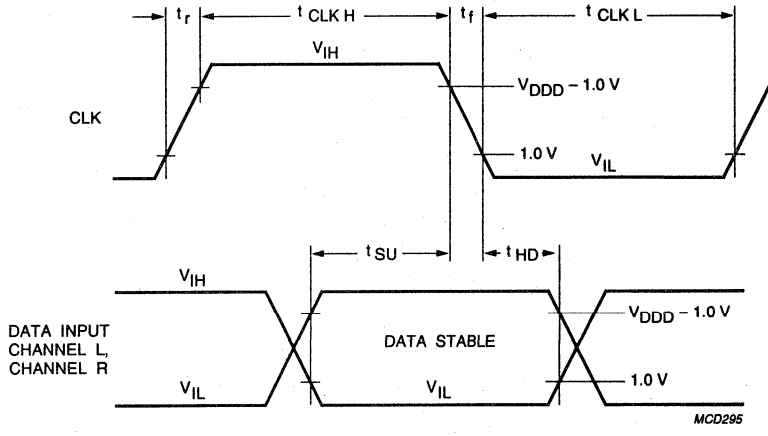


Fig.3 Timing waveform.

APPLICATION INFORMATION

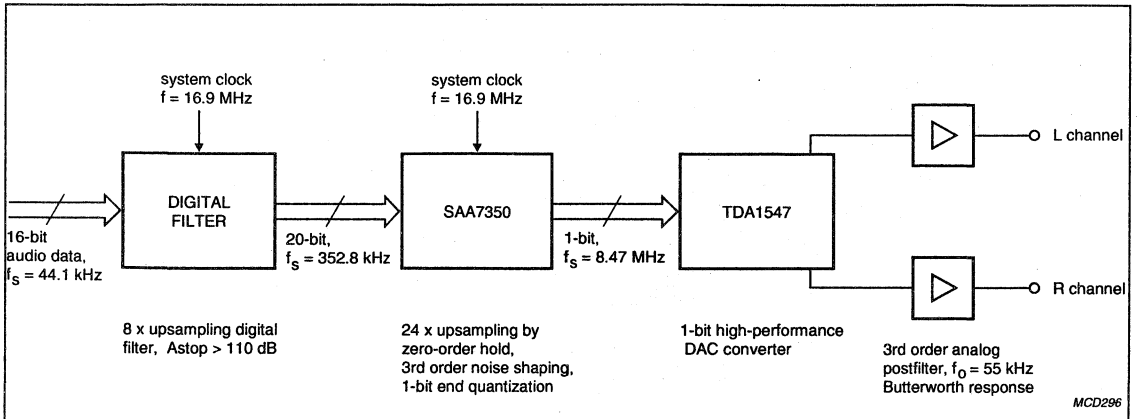


Fig.4 CD-range bitstream reconstruction system (192 f_s over-sampling).

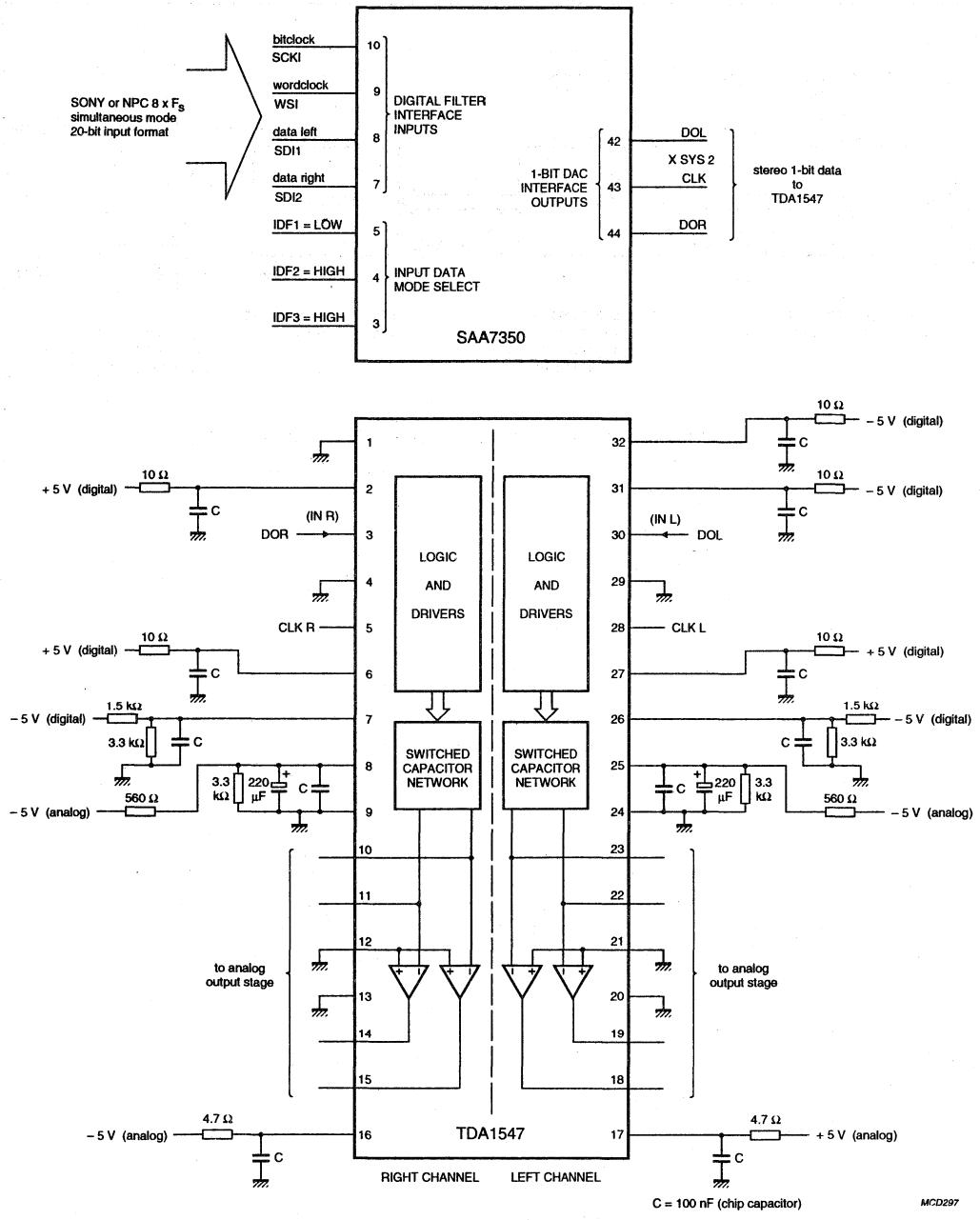


Fig.5 Application diagram.

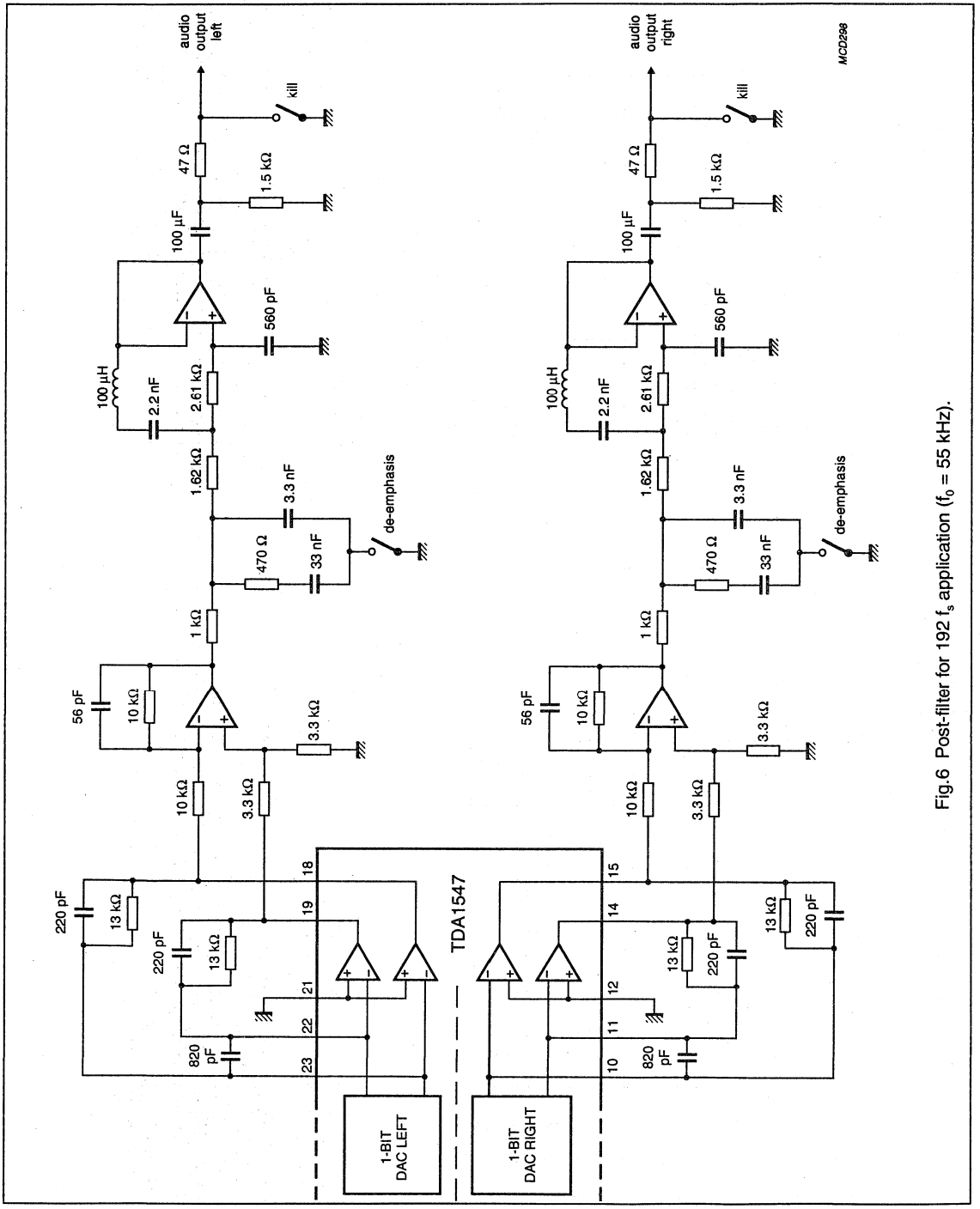


Fig.6 Post-filter for 192 f_s application (f_0 = 55 kHz).

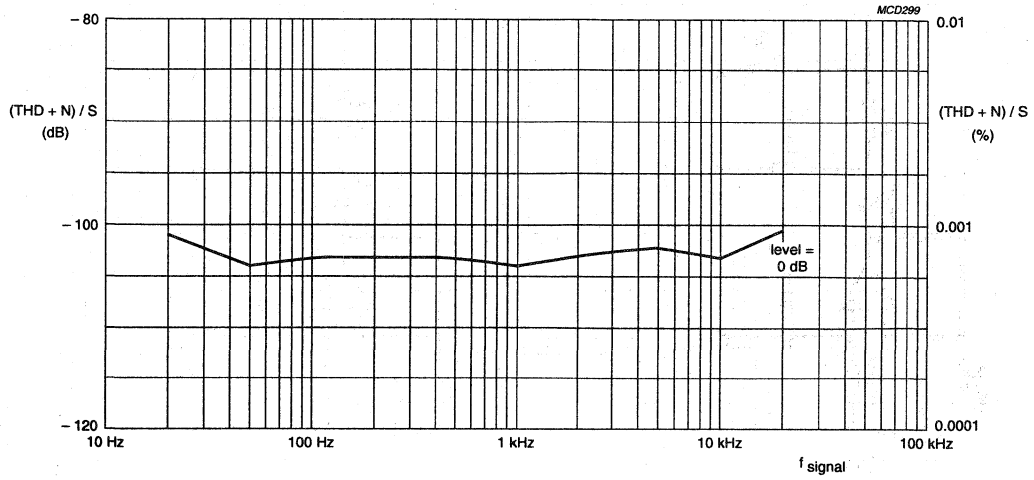


Fig.7 (THD + N)/S as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

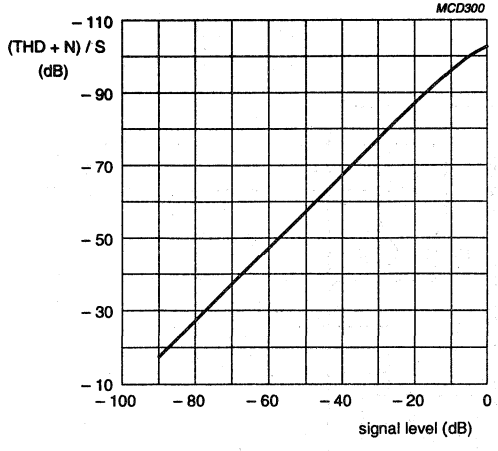


Fig.8 (THD + N)/S as a function of test signal level.

Note : Graph constructed from average measurement values of a small amount of engineering samples. No guarantee for typical values is implied.

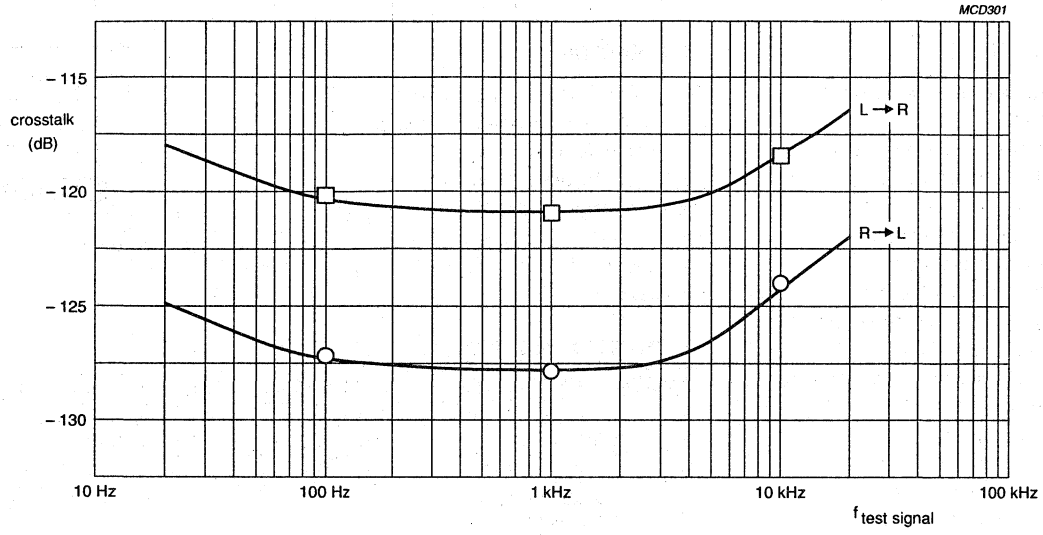


Fig.9 Inter-channel crosstalk as a function of signal frequency.

Note : Graph constructed from average measurements values of a small amount of engineering samples. No guarantee for typical values is implied.

Philips Semiconductors

Data sheet	
status	Preliminary specification
date of issue	May 1992

TDA1551Q

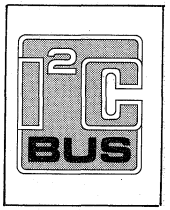
2 x 22 W BTL car radio power amplifier with diagnostic facility

FEATURES

- Requires very few external components
- Flexible in use – quad, single ended or stereo BTL
- I²C-bus control
- Dynamic distortion detector
- Thermal protection
- Output status information
- Power supply dip detection
- High output power
- MUTE/sleep mode by writing to I²C-bus
- Stand-by mode
- Fixed gain
- Good ripple rejection
- Load dump protection
- AC/DC short circuit safe to ground and V_P
- Reverse polarity safe
- Low offset voltage at output
- Capable of handling high energy at outputs (V_P = 0 V)
- Electrostatic discharge protection
- No switch-ON/switch-OFF plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

DESCRIPTION

The TDA1551Q is an integrated class-B output amplifier encased in a 17-lead single-in-line plastic power package. The device contains 4 x 11 W single-ended (SE) or 2 x 22 W BTL amplifiers and is intended for use in car radio applications.



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range	operating	6	14.4	18	V
V_P	supply voltage	non-operating	-	-	30	V
I_P	total quiescent current		-	80	160	mA
Quad single-ended application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	6	-	W
		R_L = 2 Ω; THD = 10 %	-	11	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	50	-	μV
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10 %	-	22	-	W
V_{no}	output voltage noise	R_S = 0 Ω	-	70	-	μV
ΔV_o	DC output offset voltage		-	-	100	mV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1551Q	17	SIL bent to DIL	plastic	SOT243R

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

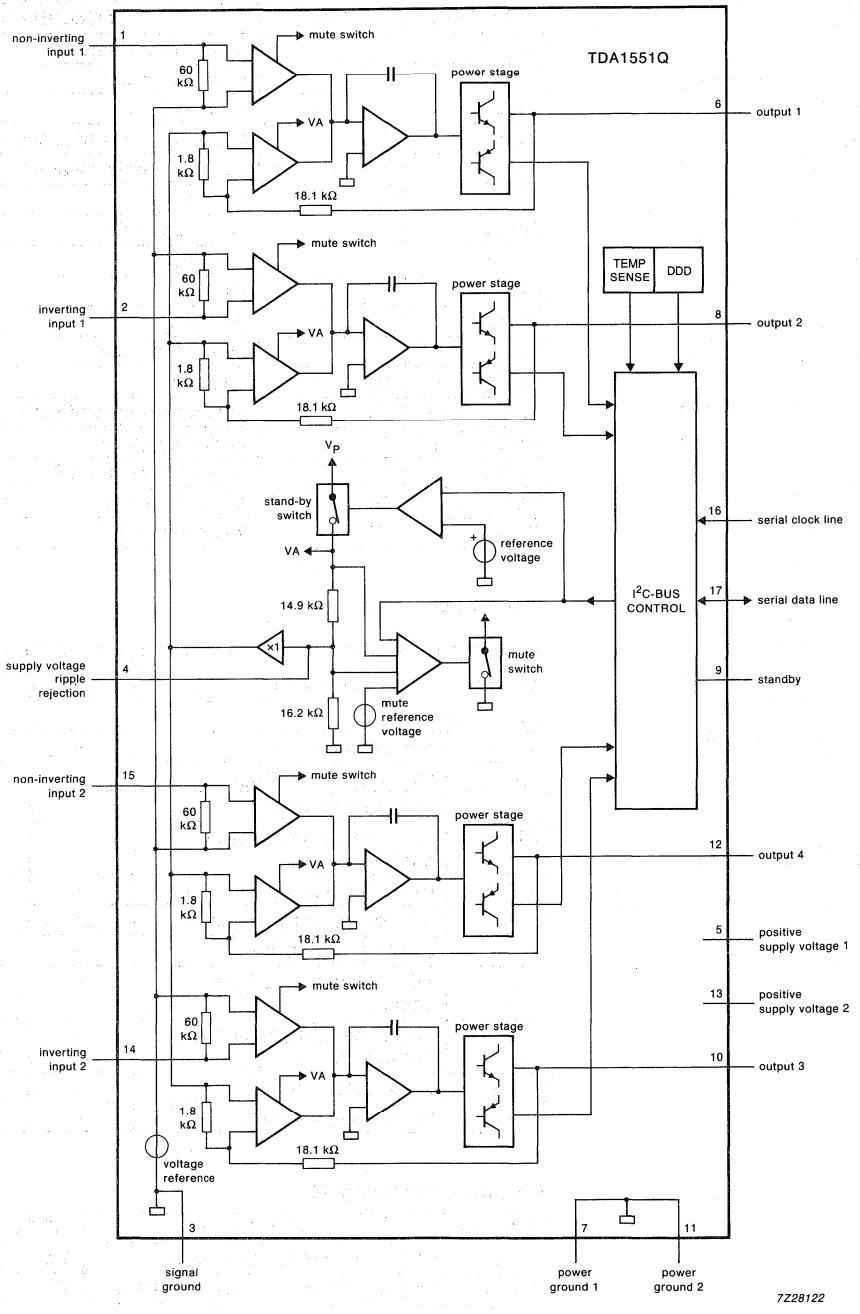


Fig.1 Block diagram.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

PIN CONFIGURATION

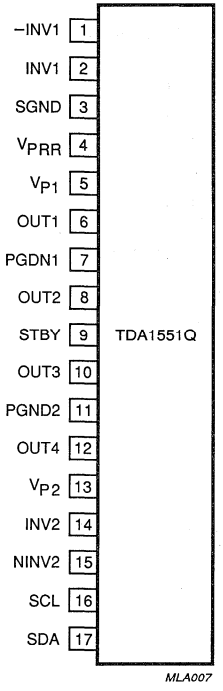


Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
−INV1	1	non-inverting input 1
INV1	2	inverting input 1
GND	3	signal ground
V_{PRR}	4	supply voltage ripple rejection
V_{p1}	5	positive supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
SB	9	standby
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{p2}	13	positive supply voltage 2
INV2	14	inverting input 2
−INV2	15	non-inverting input 2
SCL	16	serial clock line
SDA	17	serial data line

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Supply voltage				
V_P	operating voltage	–	18	V
V_P	non-operating voltage	–	30	V
	load dump protect	–	45	V
IOSM	non-repetitive peak output current	–	6	A
IORM	repetitive peak output current	–	4	A
T_{stg}	storage temperature range	−65	150	°C
T_c	crystal temperature	–	150	°C
V_{Psc}	AC/DC short-circuit safe voltage	–	18	V
	energy handling capability at outputs (V_P = 0)	–	200	mJ
V_{Pr}	reverse polarity	–	6	V
P_{tot}	total power dissipation	–	60	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}c}$	from junction to case (Fig.3)	1.5	–	K/W
$R_{th\ j\text{-}a}$	from junction to ambient in free air	40	–	K/W

FUNCTIONAL DESCRIPTION

The TDA1551Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) which can be used in SE or BTL applications. The gain of each amplifier is fixed at 20 dB for SE and 26 dB for BTL. The device also contains an I²C-bus facility which operates in the read or write mode.

In the **write** mode the device can be switched to either the sleep condition (low sleep current of 0.6 mA typ.), the MUTE condition or the ON condition.

In the **read** mode an 8-bit status word is available. Data bits D0 to D3 contain status information of each of the 4 outputs. If the device is switched to the ON or MUTE condition and there is a short-circuit at one or more outputs, the power transistors will be outside their safe operating area consequently one or more bits of D0 to D3 will be HIGH. Bits D0 to D3 are LOW when in the normal safe operating area. Bit D4 is normally LOW, if one or more channels reaches the clipping level D4 will go HIGH. Bit D5 is normally LOW, if the crystal temperature reaches 150 °C D5 will go HIGH. After a power-on reset bit 7 will go HIGH and a dip in the power supply will be noticed. Bit 7 will go LOW after the I²C-bus is read. When pin 9 is LOW the device will switch OFF and the supply current will be reduced to 0.1 mA (max.).

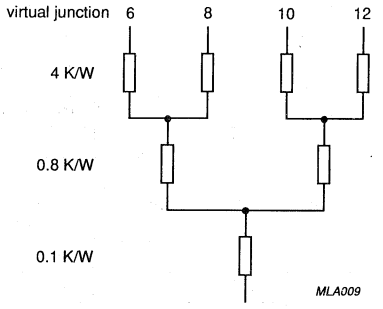


Fig.3 Thermal equivalent resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25°C; measurements in accordance with Fig.6 unless otherwise stated.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	100	mV
MUTE/sleep/standby						
V_O	output signal in MUTE position	$V_{I(max)}$ = 1 V; f = 20 Hz to 10 kHz	–	–	2	mV
I_P	DC current in sleep condition	V9 > 3 V	–	0.7	1	mA
I_P	DC current in standby condition	V9 < 2 V	–	–	0.1	mA
$\lvert\Delta V_o\rvert$	DC output offset voltage		–	–	100	mV

AC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25°C; f = 1 kHz; R_L = 4 Ω; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (Fig.7)						
P_O	output power	THD = 0.5% THD = 10%	15 20	17 22	- -	W W
P_O	output power	V_P = 13.2 V THD = 0.5% THD = 10%	 - -	 12 17	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
B	power bandwidth	THD = 0.5%; P_O = –1 dB with respect to 15 W	-	20 - 15000	-	Hz
f_{LOW}	low frequency roll-off	at –3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at –1 dB	20	-	-	kHz
G_v	closed loop voltage gain		25	26	27	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 standby; note 4	48 48 80	- - -	- - -	dB dB dB
$\lvert Z_i\rvert$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	70 100 60	- 200 -	μV μV μV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%

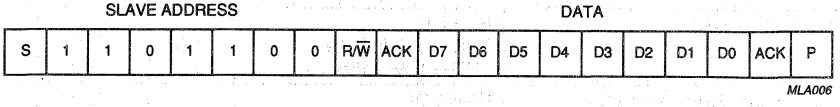
AC CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad single-ended application (Fig.6)						
P_O	output power	THD = 0.5%; note 7 THD = 10%; note 7	4 5.5	5 6	- -	W W
P_O	output power	R_L = 2 Ω THD = 0.5%; note 7 THD = 10%; note 7	 7.5 10	 8.5 11	 - -	 W W
THD	total harmonic distortion	P_O = 1 W	-	0.05	-	%
f_{LOW}	low frequency roll-off	at −3 dB; note 3	-	25	-	Hz
f_{HIGH}	high frequency roll-off	at −1 dB	20	-	-	kHz
G_v	closed loop voltage gain		19	20	21	dB
V_{PRR}	supply voltage ripple rejection	ON; note 4 MUTE; note 4 stand-by; note 4	48 48 80	- - -	- - -	dB dB dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage	ON; R_S = 0; note 5 ON; R_S = 10 kΩ; note 5 MUTE; notes 5 and 6	- - -	50 70 60	- 100 -	μV μV μV
α	channel separation	R_S = 10 kΩ	40	-	-	dB
$\|\Delta G_v\|$	channel unbalance		-	-	1	dB
	dynamic distortion detector switch level		-	3.5	-	%
I²C-bus (see I²C-bus protocol)						
V_{IH}	input voltage HIGH		3	-	5.5	V
V_{IL}	input voltage LOW		− 0.3	-	1.5	V
I_{IH}	input current HIGH	V = 5.5 V	−10	-	10	μA
I_{IL}	input current LOW	V = GND	−10	-	10	μA
V_{OL}	output voltage LOW	I_L = 3 mA	-	-	0.4	V
Power-on reset (increasing supply voltage)						
V_P	start of reset end of reset		0.5 -	- -	- 5	V V
Standby (pin 9)						
V_9	input voltage HIGH input voltage LOW		3 -	- -	V_P 2	V V

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V and AC operating at V_P = 8 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage < V_P/2.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω and at a frequency of 100 Hz to 10 kHz (amplitude = 2 V(p-p)).
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

I²C-bus protocol



S start condition
R/$\overline{W}$ read/write bit; LOW = write, HIGH = read
ACK acknowledge, generated by the receiving device
DATA see Tables 1 and 2
P stop condition

Fig.4 I²C-bus protocol.

Table 1: WRITE definition (R/$\overline{W}$ = LOW)

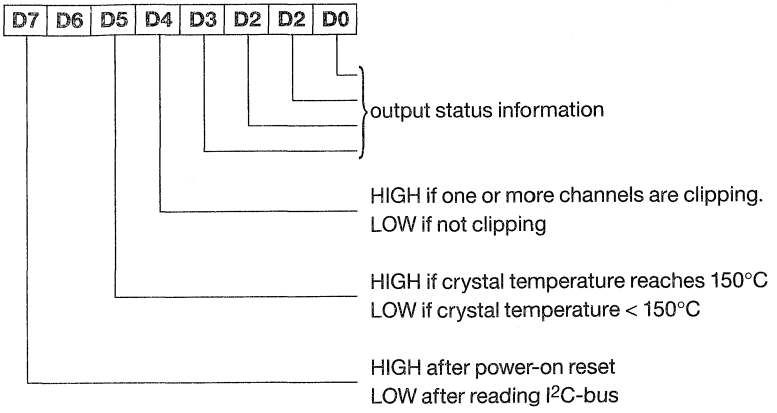
MSB			DATA				LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	SLEEP condition
0	0	0	0	0	0	0	1	MUTE condition
0	0	0	0	0	0	1	0	not allowed (1)
0	0	0	0	0	0	1	1	ON condition (2)

Bit D0 switches from SLEEP to the ON condition
Bit D1 switches the MUTE condition

(1) For test purposes only; I²C-bus is in the ON condition, amplifier is in the stand-by condition.

(2) To get into the ON condition without switch-on plops, the device should be switched from the SLEEP condition to the MUTE condition and then, after a period of 150 ms, to the ON condition.

Table 2: READ definition (R/$\overline{W}$ = HIGH)



If the device is sinewave driven bit D4 will be HIGH if the THD in one or more channels exceeds 3.5%.

Table 3: Fault conditions

DATA MSB				
D3	D2	D1	D0	FUNCTION
0	0	0	0	all output power transistors in the normal safe operating condition
-	-	-	1	fault condition pin 6
-	-	1	-	fault condition pin 8
-	1	-	-	fault condition pin 10
1	-	-	-	fault condition pin 12

If more outputs are in a fault condition (e.g. short-circuit) then more bits, D3 to D0, will be HIGH.

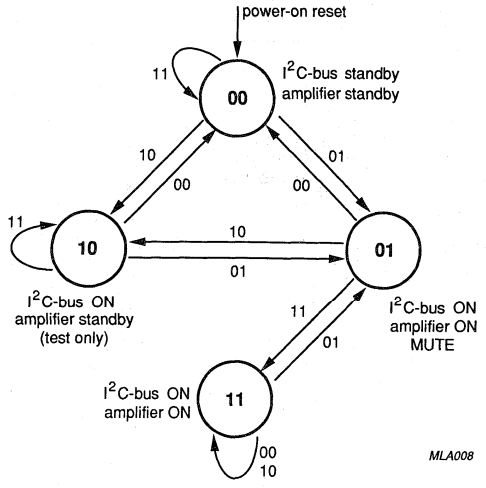


Fig.5 State diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

2 x 22 W BTL car radio power amplifier with diagnostic facility

TDA1551Q

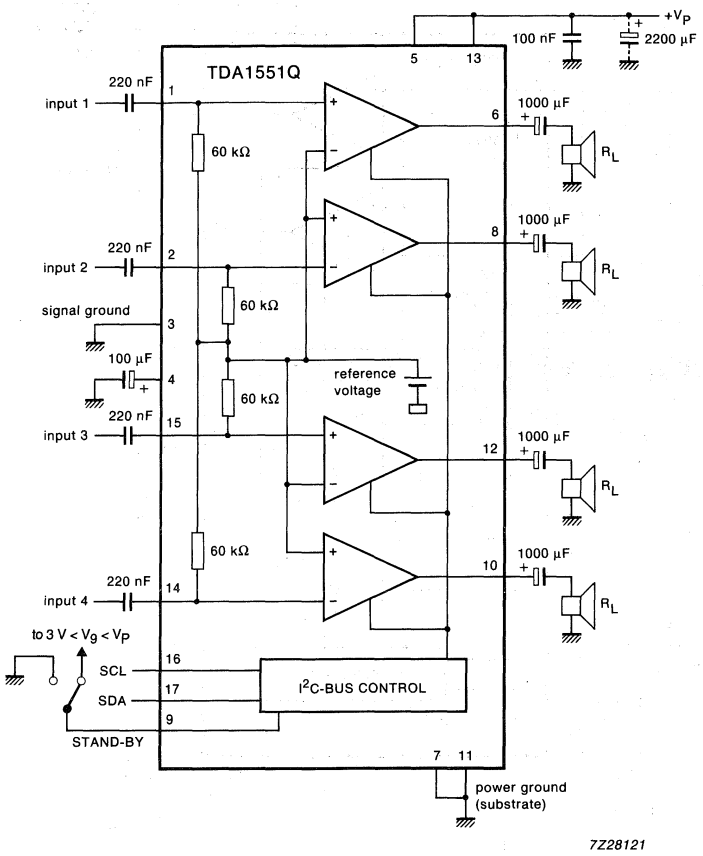


Fig.6 Test circuit quad single-ended.

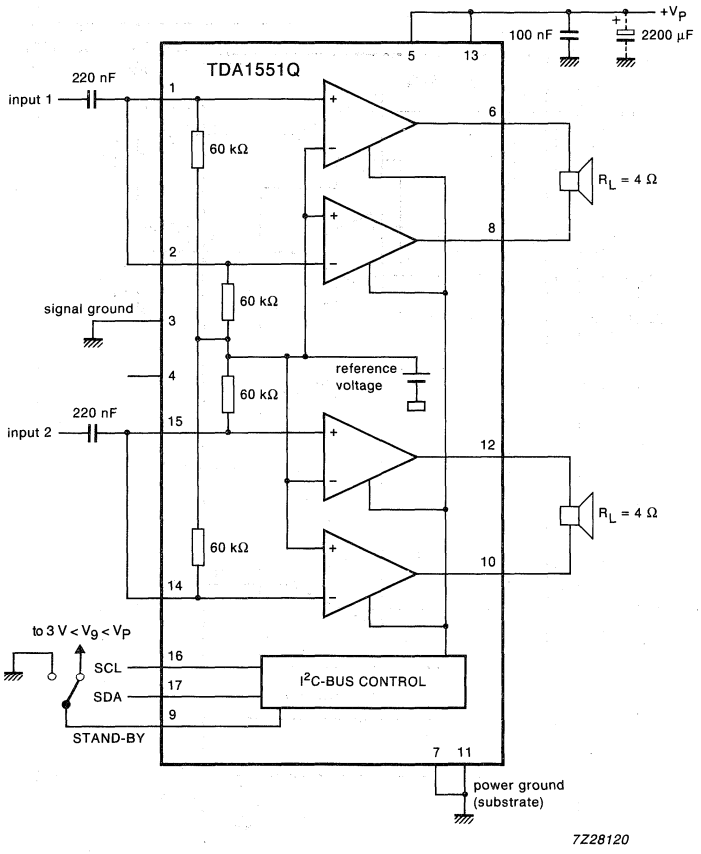


Fig.7 Test circuit stereo BTL.

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1552Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω; f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

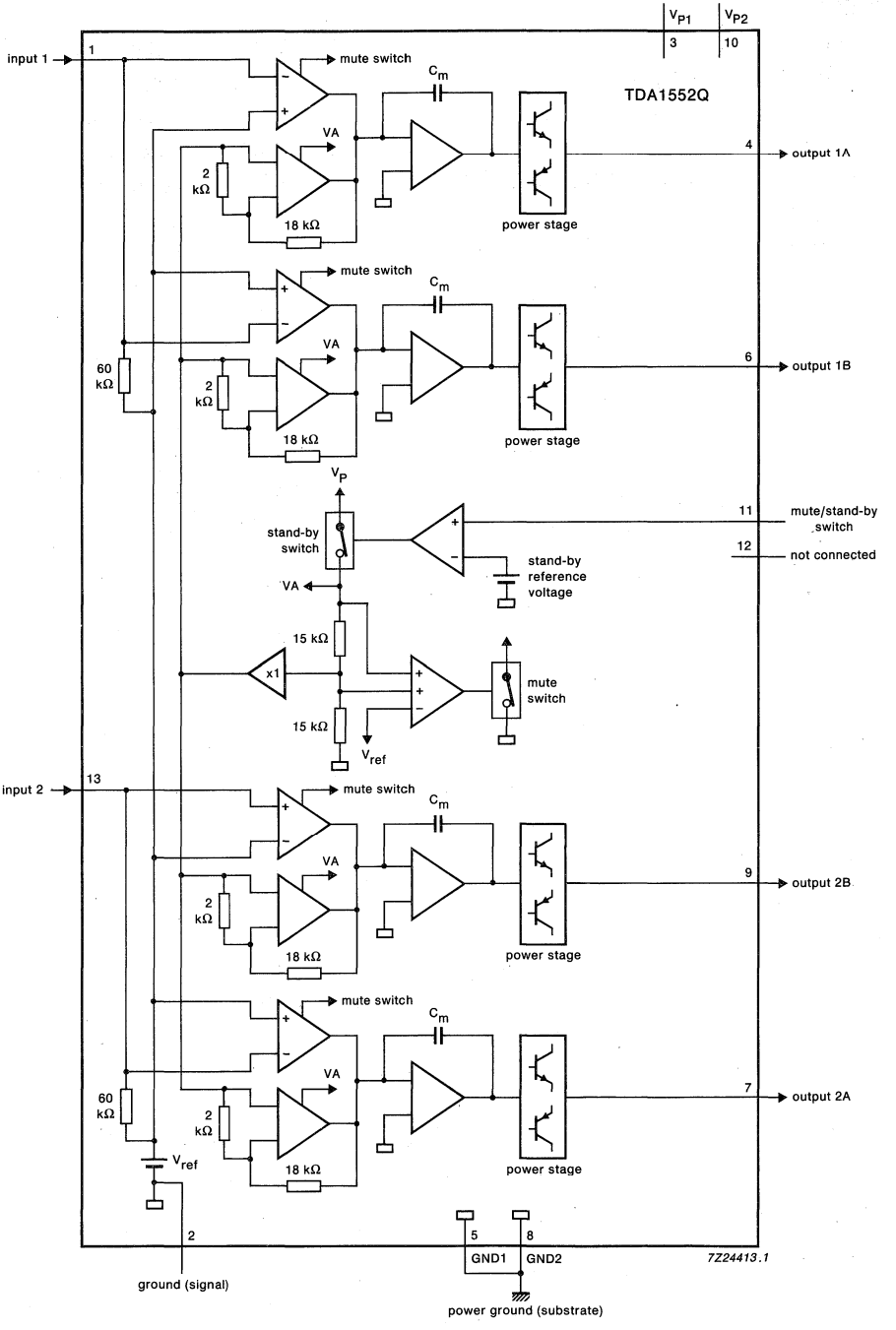


Fig.1 Block diagram.

PINNING

1	IP1	input 1	8	GND2	power ground 2 (substrate)
2	GND	ground (signal)	9	OUT2B	output 2B
3	V_{P1}	positive supply voltage 1	10	V_{P2}	positive supply voltage 2
4	OUT1A	output 1A	11	M/SS	mute/stand-by switch
5	GND1	power ground 1 (substrate)	12	n.c.	not connected
6	OUT1B	output 1B	13	IP2	input 2
7	OUT2A	output 2A			

FUNCTIONAL DESCRIPTION

The TDA1552Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

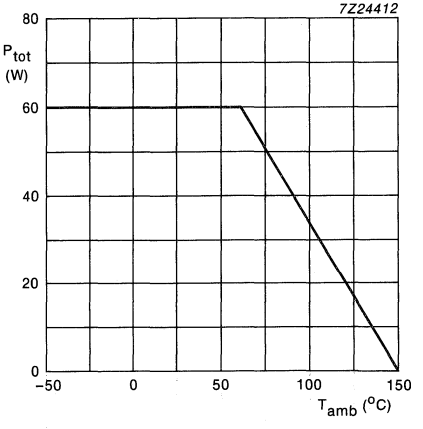


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_I < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \text{ V} \leqslant V_I < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to GND note 3	I_P	–	5.5	–	mA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4; −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ V_P/2.
3. Conditions: 1. V_{11} = 0 V
   2. short-circuit to GND
   3. switch V_{11} to MUTE or ON condition (rise time ⩾ 10 μs).
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

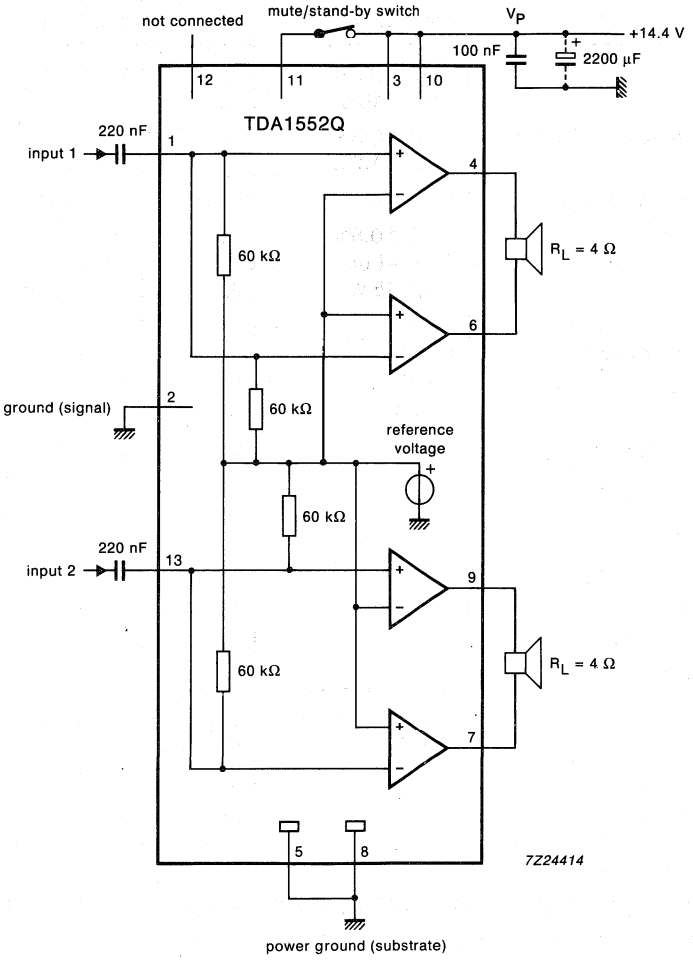


Fig.3 Application circuit diagram.

2 X 22 W BTL STEREO CAR RADIO POWER AMPLIFIER WITH LOUDSPEAKER PROTECTION

GENERAL DESCRIPTION

The TDA1553Q is an integrated class-B output amplifier in a 13-lead single-in-line (SIL) plastic power package. The circuit contains 2 x 22 W amplifiers in Bridge Tied Load (BTL) configuration. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- High output power
- Low offset voltage at outputs
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Loudspeaker protection (LSP)
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_P	6.0	14.4	18.0	V
non-operating		V_P	–	–	30	V
load dump protected		V_P	–	–	45	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Switch-on current		I_{sw}	–	–	60	μA
Input impedance		$\|Z_I\|$	50	60	75	kΩ
Junction temperature		T_j	–	–	150	°C
Stereo application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection	R_S = 0 Ω f = 100 Hz to 10 kHz	RR	48	–	–	dB
DC output offset voltage		$\|\Delta V_O\|$	–	–	150	mV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_V\|$	–	–	1	dB

PACKAGE OUTLINE

13-lead SIL-bent-to-DIL; plastic power (SOT141R).

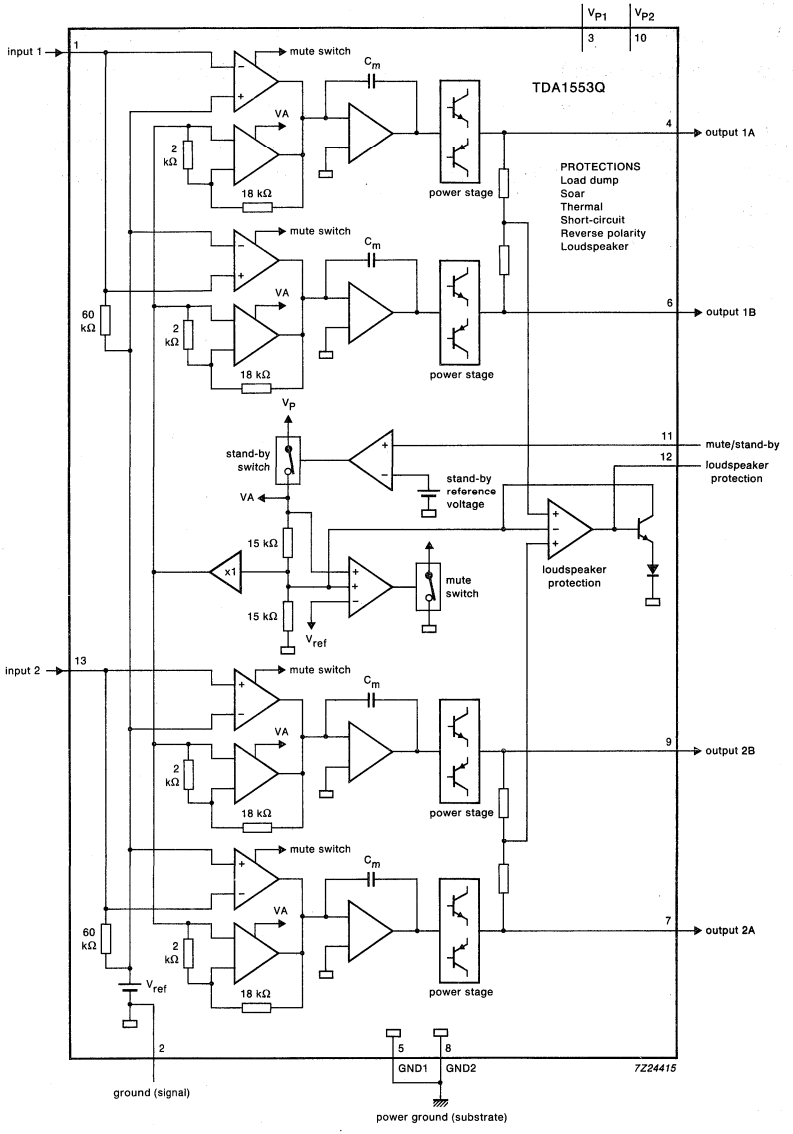


Fig.1 Block diagram.

PINNING

1	IP1	input 1
2	GND	ground (signal)
3	V_{P1}	positive supply voltage 1
4	OUT1A	output 1A
5	GND1	power ground 1 (substrate)
6	OUT1B	output 1B
7	OUT2A	output 2A
8	GND2	power ground 2 (substrate)
9	OUT2B	output 2B
10	V_{P2}	positive supply voltage 2
11	M/SS	mute/stand-by switch
12	LSP	loudspeaker protection
13	IP2	input 2

FUNCTIONAL DESCRIPTION

The TDA1553Q contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

Loudspeaker protection

When a short-circuit to ground is made, which forces a DC voltage across the loudspeaker of $\geqslant 1$ V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to $\leqslant 1$ V. The delay time of the protection circuit can be controlled by an external capacitor connected to pin 12.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	−55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	V_P = 0 V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

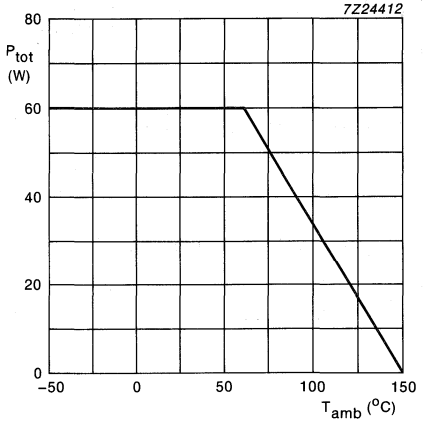


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	150	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max.); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 4 to 6 and 7 to 9)		$\lvert\Delta V_O\rvert$	–	–	150	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition	$V_{I1} < 0.5$ V	I_{sb}	–	–	100	μA
	$0.5 \leqslant V_{I1} < 2$ V	I_{sb}	–	–	500	μA
Switch-on current		I_{sw}	–	25	60	μA
Supply current	short-circuit to ground note 3	I_p	–	5.5	–	mA
Loudspeaker protection						
DC voltage across R_L pin 4 to pin 6		ΔV_{4-6}	–	–	1	V
pin 7 to pin 9		ΔV_{7-9}	–	–	1	V
Delay time		t_d	–	0.5	–	s
Protection active	$\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert \geqslant 1.0$ V					
Current information		I_{12}	–	25	–	μA
Voltage information		V_{12}	2	–	–	V
Protection not active	$\lvert\Delta V_{4-6}\rvert$ and $\lvert\Delta V_{7-9}\rvert \leqslant 0.1$ V					
Voltage information		V_{12}	–	–	0.3	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5%; P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 4; −1 dB	f_L	–	25	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	notes 5, 6	RR	42	–	–	dB
ON	notes 5, 7	RR	48	–	–	dB
mute	notes 5, 6, 7	RR	48	–	–	dB
stand-by	notes 5, 6, 7	RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 8	$V_{no(rms)}$	–	70	120	μV
ON	R_S = 10 kΩ; note 8	$V_{no(rms)}$	–	100	–	μV
mute	notes 8, 9	$V_{no(rms)}$	–	60	–	μV
Channel separation		α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Conditions: 1. V_{11} = 0 V
   2. short-circuit to GND
   3. switch V_{11} to MUTE or ON condition (rise time ⩾ 10 μs).
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V).
6. Frequency f = 100 Hz.
7. Frequency between 1 kHz and 10 kHz.
8. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
9. Noise output voltage independent of R_S (V_I = 0 V).

APPLICATION INFORMATION

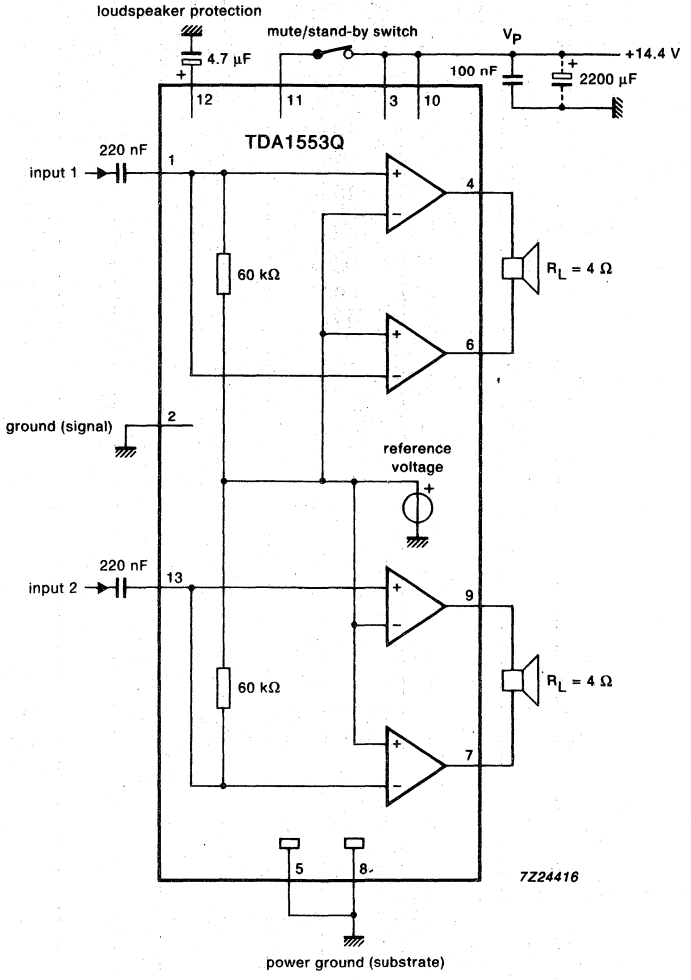


Fig.3 Application circuit diagram.

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

FEATURES

- Few peripheral components
- High output power
- Low output offset voltage
- Fixed gain
- Loudspeaker protection
- Good ripple rejection
- 3-state mode switch (operating, mute, stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Thermally protected
- Reverse polarity safe
- High energy handling capability at the outputs ($V_P = 0$)
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance

GENERAL DESCRIPTION

The TDA1553CQ is a monolithic integrated class-B output amplifier in a 13-lead single-in-line (SIL) power package. It contains 2 x 22 W amplifiers in BTL configuration.
The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage					
	operating		6	14.4	18	V
	non-operating		–	–	30	V
	load dump		–	–	45	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	40	100	μA
$\|Z_I\|$	input impedance		50	–	–	kΩ
T_{vj}	virtual junction temperature		–	–	150	°C
Stereo application						
P_O	output power	at 4 Ω; THD = 10%	–	22	–	W
RR	supply voltage ripple rejection	R_s = 0 Ω; f = 100 Hz to 10 kHz	48	–	–	dB
$\|\Delta V_O\|$	DC output offset voltage		–	–	150	mV
α	channel separation		40	–	–	dB
$\|\Delta G_V\|$	channel unbalance		–	–	1	dB

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1553CQ	13	SIL	plastic	SOT141R

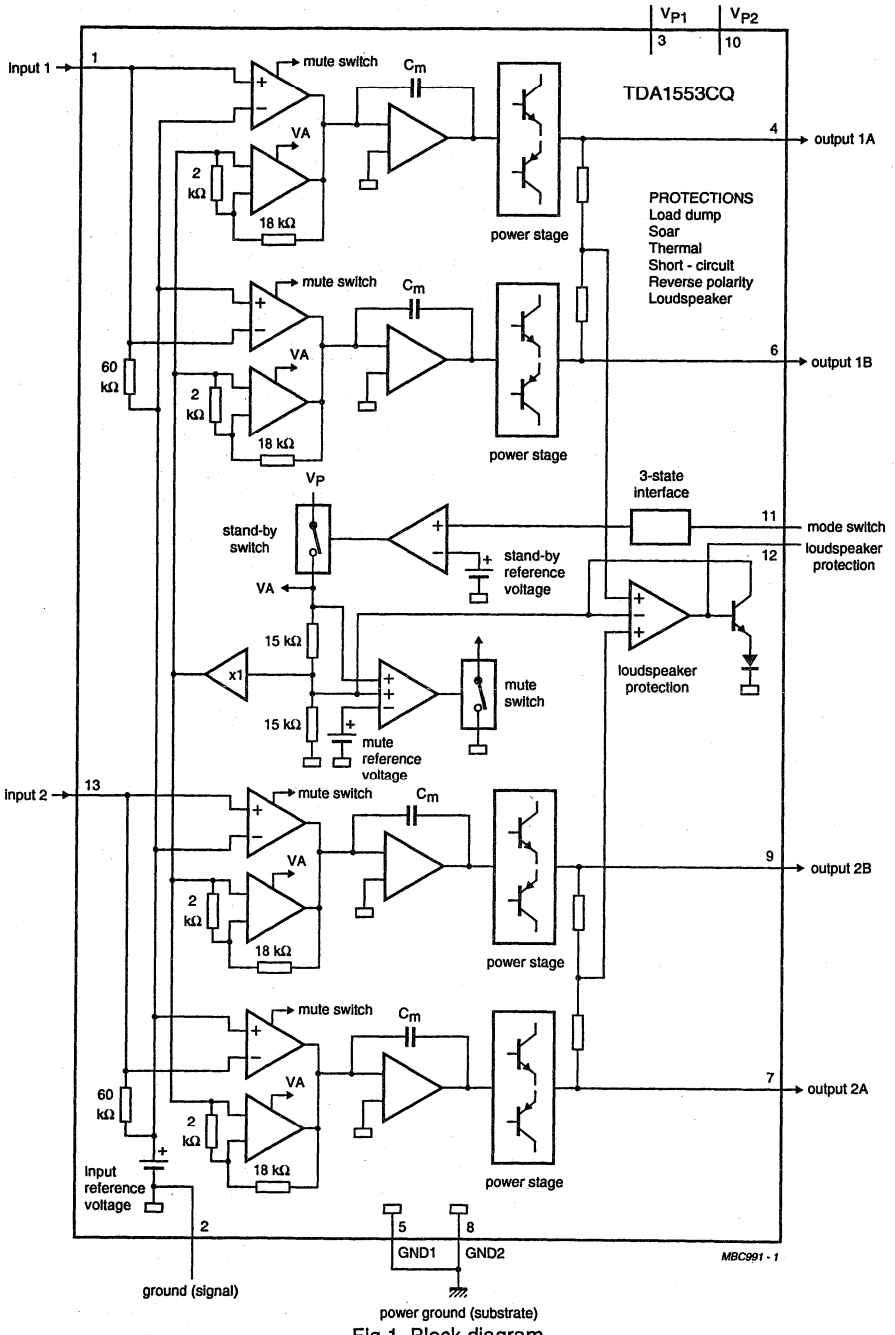


Fig.1 Block diagram.

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

PINNING

SYMBOL	PIN	DESCRIPTION
IN 1	1	input 1
GND(S)	2	signal ground
V_{P1}	3	supply voltage
OUT 1A	4	output 1A
GND1	5	power ground 1
OUT 1B	6	output 1B
OUT 2A	7	output 2A
GND2	8	power ground 2
OUT 2B	9	output 2B
V_{P2}	10	supply voltage
MODE	11	mode switch input
LSP	12	loudspeaker protection
IN 2	13	input 2

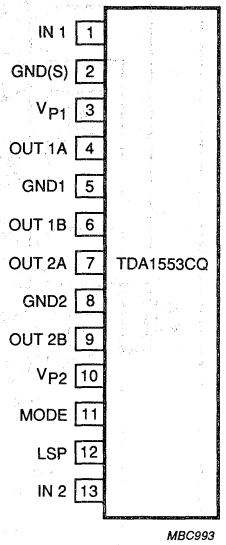


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1553CQ contains two identical amplifiers with differential input stages and can be used for bridge applications. The gain of each amplifier is fixed at 26 dB. Special features of the device are:

3-state mode switch

- standby : low supply current (< 100 μA)
- mute : input signal suppressed
- operating: normal on condition

Loudspeaker protection

When a short-circuit to ground occurs, which forces a DC voltage across the loudspeaker of ≥ 1 V, a built-in protection circuit becomes active and limits the DC voltage across the loudspeaker to ≤ 1 V.
Pin 12 detects the status of the protection circuit, (e.g. for diagnostic purposes).

Short-circuit protection

If any output is short-circuited to ground during the stand-by mode, it becomes impossible to switch the circuit to the mute or operating condition. In this event the supply current will be limited to a few milliamps.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
V_P	positive supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature range		–55	150	°C
T_{amb}	operating ambient temperature range		–40	85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
	energy handling capability at outputs	$V_P = 0$	–	200	mJ
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL RESISTANCE

In accordance with IEC 747-1

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air		40 K/W
$R_{th\ j\text{-}c}$	from junction to case	see Fig.3	1.5 K/W

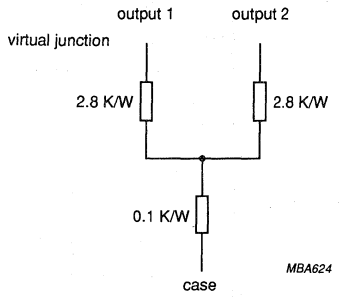


Fig.3 Equivalent thermal resistance network.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.4; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	quiescent current					
		$R_L = \infty$	–	80	160	mA
		note 2	–	5.5	–	mA
Operating condition						
V_{11}	mode switch voltage level		2.2	–	7	V
I_{11}	mode switch current	V_{11} = 2.2 V	–	50	100	µA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Mute condition						
V_{11}	mode switch voltage level		0	–	0.6	V
$-I_{11}$	mode switch current	V_{11} = 0.6 V	–	50	100	µA
V_O	DC output voltage	note 3	–	6.9	–	V
$\lvert\Delta V_O\rvert$	DC output offset voltage		–	–	150	mV
Stand-by condition						
$\lvert I_{11}\rvert$	mode switch 3-state leakage current		–	–	10	µA
I_{sb}	stand-by current	I_{11} = 0 µA	–	40	100	µA
Loudspeaker protection						
$\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert$	DC voltage across R_L		–	–	1	V
Protection active ($\lvert\Delta V_{4-6}\rvert$ or $\lvert\Delta V_{7-9}\rvert \geq$ 1.0 V)						
I_{12}	current information		–	25	–	µA
V_{12}	voltage information		3.6	–	–	V
Protection not active ($\lvert\Delta V_{4-6}\rvert$ and $\lvert\Delta V_{7-9}\rvert \leq$ 0.15 V)						
V_{12}	voltage information		–	–	0.3	V

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.4; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_O	output power	V_P = 14.4 V				
		THD = 0.5%	15	17	–	W
		THD = 10%	20	22	–	W
THD	total harmonic distortion	P_O = 1 W	–	0.1	–	%
P_O	output power	V_P = 13.2 V				
		THD = 0.5%	–	12	–	W
		THD = 10%	–	17	–	W
B	power bandwidth	THD = 0.5%; P_O = −1 dB; with respect to 15 W	–	20 - 15000	–	Hz
f_l	low frequency roll-off	at −1 dB; note 4	–	25	–	Hz
f_h	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
RR	supply voltage ripple rejection	note 5				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$\|Z_I\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage	note 6				
	on	R_S = 0 Ω	–	70	120	μV
	on	R_S = 10 kΩ	–	100	–	μV
V_{no}	noise output voltage	notes 6 and 7				
	mute		–	60	–	μV
α	channel separation	R_S = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
V_O	output voltage in mute	note 8	–	–	2	mV

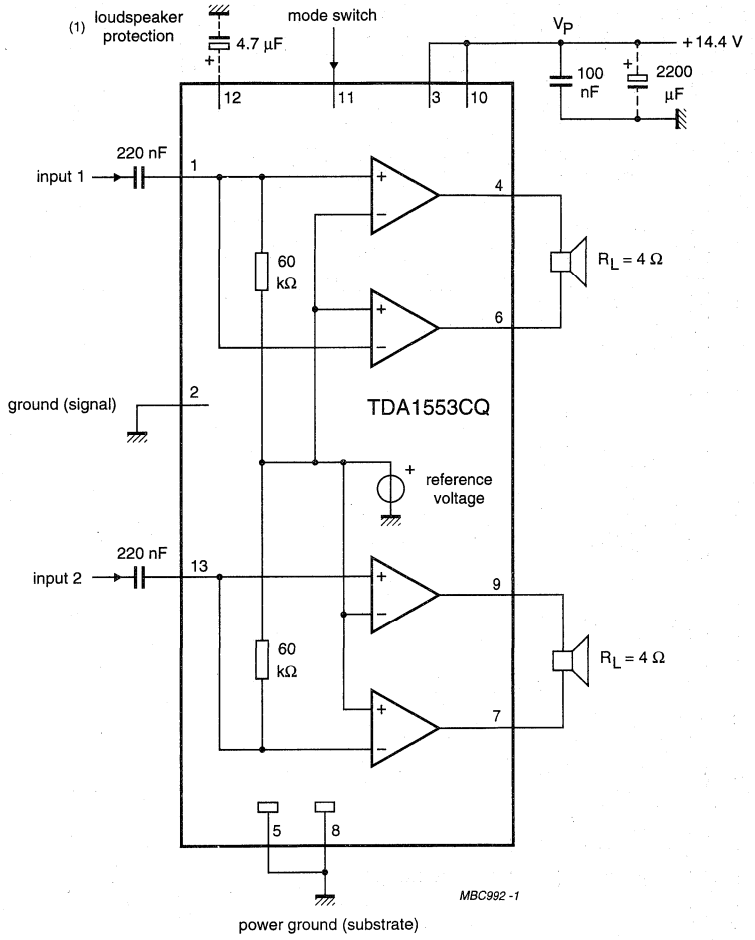
Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 9 to 18 V.
2. If any output is short-circuited to ground during the stand-by mode and in this condition the circuit is switched to mute or operating.
3. At 18 V < V_P < 30 V the DC output voltage ≤ V_P/2.
4. Frequency response externally fixed.
5. Ripple rejection measured at the output with a source-impedance of 0 Ω, maximum ripple amplitude of 2 V p-p and at a frequency between 100 Hz and 10 kHz.
6. Noise measured in a bandwidth of 20 Hz to 20 kHz.
7. Noise output voltage independent of R_S (V_I = 0 V).
8. $V_I = V_{Imax}$ = 1 V RMS.

2 x 22 W stereo BTL car radio power amplifier with loudspeaker protection and 3-state mode switch

TDA1553CQ

TEST/APPLICATION INFORMATION



(1) With C = 4.7 µF the delay time of the loudspeaker protection is typically 0.5 s.

Fig.4 Stereo BTL application diagram.

4 X 11 W SINGLE-ENDED OR 2 X 22 W POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1554Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) plastic power package. The circuit contains 4 x 11 W single-ended or 2 x 22 W bridge amplifiers. The device is primarily developed for car radio applications.

Features

- Requires very few external components
- Flexibility in use – Quad single-ended or stereo BTL
- High output power
- Low offset voltage at outputs (important for BTL)
- Fixed gain
- Good ripple rejection
- Mute/stand-by switch
- Load dump protection
- AC and DC short-circuit-safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Low thermal resistance
- Identical inputs (inverting and non-inverting)
- Flexible leads

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range operating		V_P	6.0	14.4	18.0	V
Repetitive peak output current		I_{ORM}	–	–	4	A
Total quiescent current		I_{tot}	–	80	160	mA
Stand-by current		I_{sb}	–	0.1	100	μA
Stereo BTL application						
Output power	R_L = 4 Ω; THD = 10%	P_o	20	22	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	70	–	μV
Input impedance		$\|Z_I\|$	25	30	38	kΩ
DC output offset voltage		$\|\Delta V_O\|$	–	–	100	mV
Quad single-ended application						
Output power	THD = 10%					
	R_L = 4 Ω	P_o	–	6	–	W
	R_L = 2 Ω	P_o	–	11	–	W
Supply voltage ripple rejection		RR	48	–	–	dB
Noise output voltage (RMS value)	R_S = 0 Ω	$V_{no(rms)}$	–	50	–	μV
Input impedance		$\|Z_I\|$	50	60	75	kΩ

PACKAGE OUTLINE

17-lead SIL-bent-to-DIL; plastic power (SOT243R).

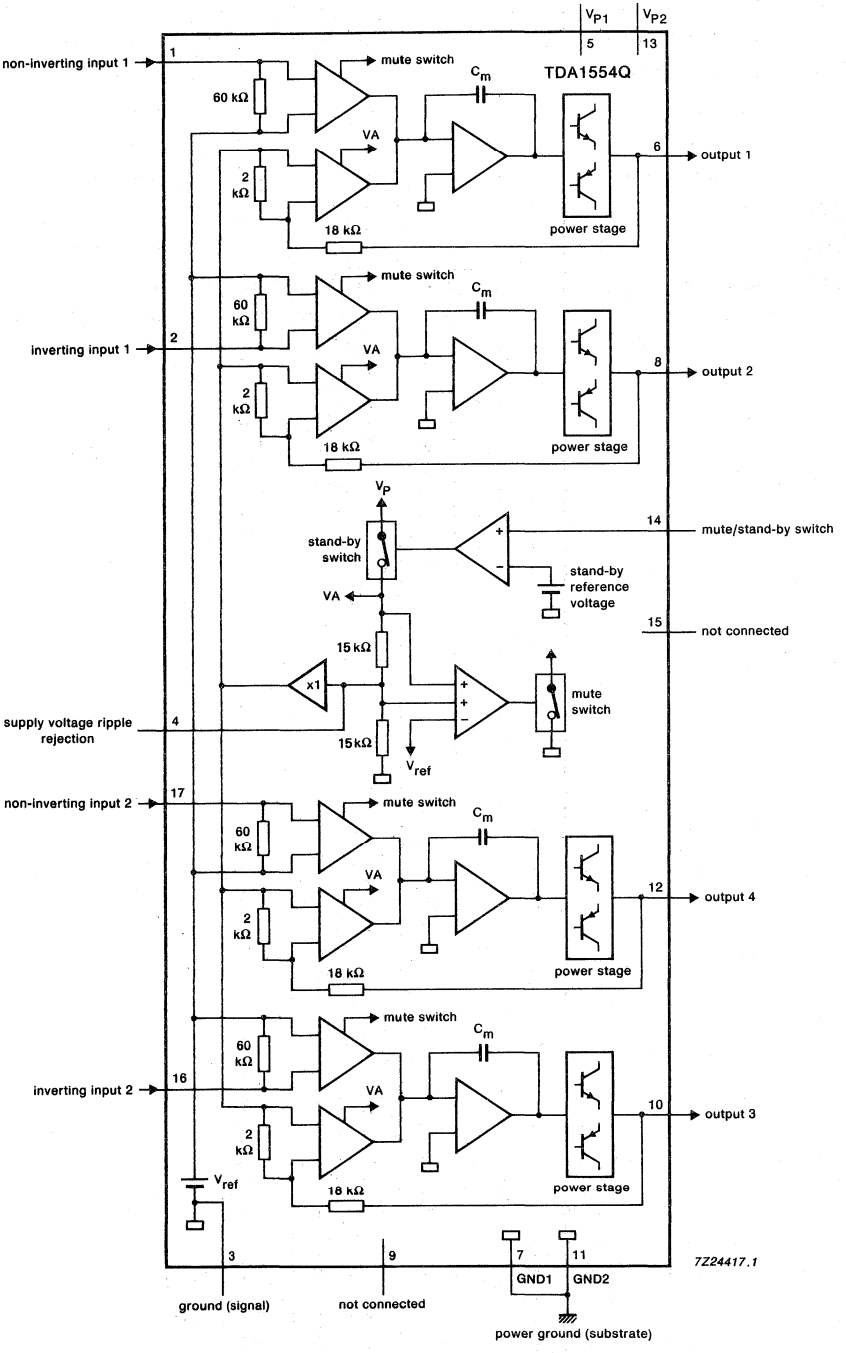


Fig.1 Block diagram.

PINNING

1	NINV1	non-inverting input 1	9	n.c.	not connected
2	INV1	inverting input 1	10	OUT3	output 3
3	GND	ground (signal)	11	GND2	power ground 2 (substrate)
4	RR	supply voltage ripple rejection	12	OUT4	output 4
5	V_{P1}	positive supply voltage 1	13	V_{P2}	positive supply voltage 2
6	OUT1	output 1	14	M/SS	mute/stand-by switch
7	GND1	power ground 1 (substrate)	15	n.c.	not connected
8	OUT2	output 2	16	INV2	inverting input 2
			17	NINV2	non-inverting input 2

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION

The TDA1554Q contains four identical amplifiers with differential input stages (two inverting and two non-inverting) and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). A special feature of this device is:

Mute/stand-by switch

- low stand-by current ($< 100\ \mu A$)
- low mute/stand-by switching current (low cost supply switch)
- mute facility

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage					
operating		V_P	–	18	V
non-operating		V_P	–	30	V
load dump protected	during 50 ms; $t_r \geqslant 2.5$ ms	V_P	–	45	V
Non-repetitive peak output current		I_{OSM}	–	6	A
Repetitive peak output current		I_{ORM}	–	4	A
Storage temperature range		T_{stg}	–55	+ 150	°C
Junction temperature		T_j	–	150	°C
AC and DC short-circuit-safe voltage		V_{PSC}	–	18	V
Energy handling capability at outputs	$V_P = 0$ V		–	200	mJ
Reverse polarity		V_{PR}	–	6	V
Total power dissipation	see Fig.2	P_{tot}	–	60	W

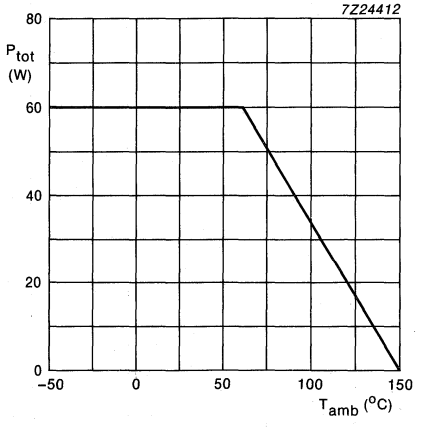


Fig.2 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measurements taken using Fig.4; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range	note 1	V_P	6.0	14.4	18.0	V
Total quiescent current		I_{tot}	–	80	160	mA
DC output voltage	note 2	V_O	–	6.9	–	V
DC output offset voltage		$\lvert\Delta V_O\rvert$	–	–	100	mV
Mute/stand-by switch						
Switch-on voltage level		V_{ON}	8.5	–	–	V
Mute condition		V_{mute}	3.3	–	6.4	V
Output signal in mute position	V_I = 1 V (max); f = 1 kHz	V_O	–	–	2	mV
DC output offset voltage (between pins 6 to 8 and 10 to 12)		$\lvert\Delta V_O\rvert$	–	–	100	mV
Stand-by condition		V_{sb}	0	–	2	V
DC current in stand-by condition		I_{sb}	–	–	100	μA
Switch-on current		I_{sw}	–	12	40	μA

DEVELOPMENT DATA

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measurements taken using Fig.3 for stereo BTL application and Fig.4 for quad single-ended application unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo BTL application						
Output power	THD = 0.5%	P_o	15	17	–	W
	THD = 10%	P_o	20	22	–	W
Output power at V_P = 13.2 V	THD = 0.5%	P_o	–	12	–	W
	THD = 10%	P_o	–	17	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Power bandwidth	THD = 0.5% P_o = −1 dB w.r.t. 15 W	B_w	–	20 to 15 000	–	Hz
Low frequency roll-off	note 3 −1 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	25	26	27	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	25	30	38	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	70	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	100	200	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	60	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Quad single-ended application						
Output power	note 7					
	THD = 0.5%	P_o	4	5	–	W
	THD = 10%	P_o	5.5	6	–	W
Output power at R_L = 2 Ω	note 7					
	THD = 0.5%	P_o	7.5	8.5	–	W
	THD = 10%	P_o	10	11	–	W
Total harmonic distortion	P_o = 1 W	THD	–	0.1	–	%
Low frequency roll-off	note 3					
	−3 dB	f_L	–	45	–	Hz
High frequency roll-off	−1 dB	f_H	20	–	–	kHz
Closed loop voltage gain		G_v	19	20	21	dB
Supply voltage ripple rejection	note 4					
ON		RR	48	–	–	dB
mute		RR	48	–	–	dB
stand-by		RR	80	–	–	dB
Input impedance		$\|Z_i\|$	50	60	75	kΩ
Noise output voltage (RMS value)						
ON	R_S = 0 Ω; note 5	$V_{no(rms)}$	–	50	–	μV
ON	R_S = 10 kΩ; note 5	$V_{no(rms)}$	–	70	100	μV
mute	notes 5 and 6	$V_{no(rms)}$	–	50	–	μV
Channel separation	R_S = 10 kΩ	α	40	–	–	dB
Channel unbalance		$\|\Delta G_v\|$	–	–	1	dB

Notes to the characteristics

1. The circuit is DC adjusted at V_P = 6 V to 18 V and AC operating at V_P = 8.5 V to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage ⩽ $V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0 Ω (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S (V_I = 0 V).
7. Output power is measured directly at the output pins of the IC.

APPLICATION INFORMATION

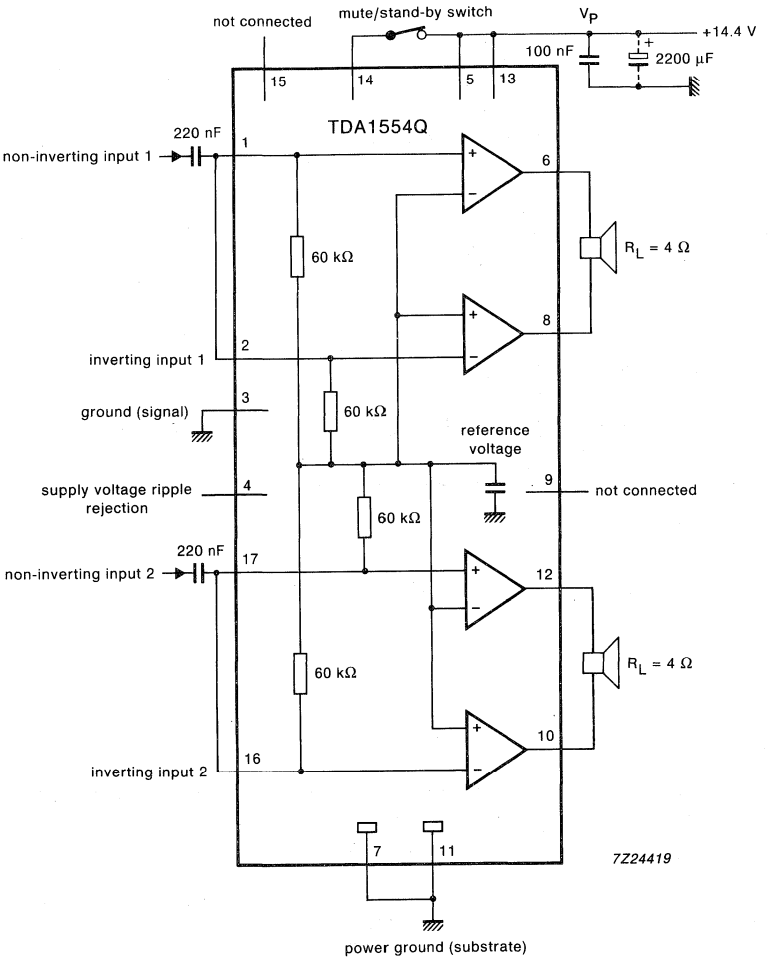


Fig.3 Stereo BTL application circuit diagram.

DEVELOPMENT DATA

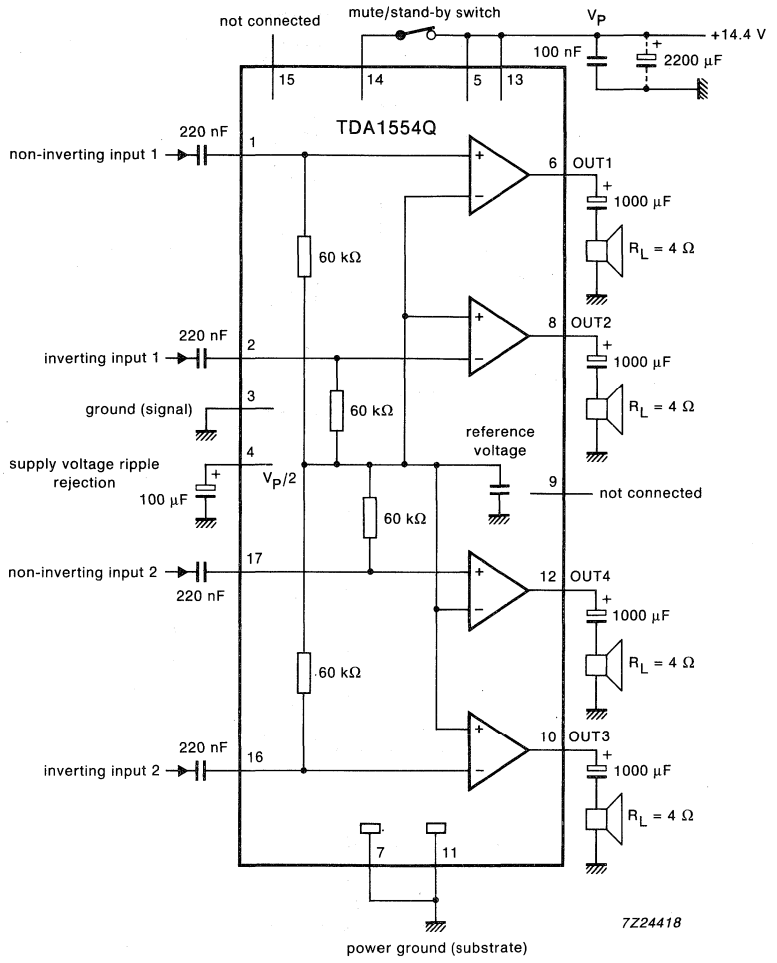


Fig.4 Quad single-ended application circuit diagram.

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